

MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultra-Low Power Consumption
 - Active Mode (AM)
All System Clocks Active
 - 195 μ A/MHz at 8 MHz, 3 V, Flash Program Execution (Typical)
 - 115 μ A/MHz at 8 MHz, 3 V, RAM Program Execution (Typical)
 - Standby Mode (LPM3)
 - Real-Time Clock With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up:
1.9 μ A at 2.2 V, 2.1 μ A at 3 V (Typical)
 - Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up:
1.4 μ A at 3 V (Typical)
 - Off Mode (LPM4)
Full RAM Retention, Supply Supervisor Operational, Fast Wake-Up:
1.1 μ A at 3 V (Typical)
 - Shutdown Mode (LPM4.5)
0.18 μ A at 3 V (Typical)
- Wake-Up From Standby in Less Than 5 μ s
- 16-Bit RISC Architecture, Extended Memory, Up to 25-MHz System Clock
- Flexible Power Management System
 - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
 - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
 - FLL Control Loop for Frequency Stabilization
 - Low-Power Low-Frequency Internal Clock Source (VLO)
 - Low-Frequency Trimmed Internal Reference Source (REFO)
 - 32-kHz Watch Crystals (XT1)
- High-Frequency Crystals up to 32 MHz (XT2)
- 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
- 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TA2, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer_B With Seven Capture/Compare Shadow Registers
- Two Universal Serial Communication Interfaces
 - USCI_A0 and USCI_A1 Each Support:
 - Enhanced UART Supports Auto-Baudrate Detection
 - IrDA Encoder and Decoder
 - Synchronous SPI
 - USCI_B0 and USCI_B1 Each Support:
 - I²C™
 - Synchronous SPI
- Full-Speed Universal Serial Bus (USB)
 - Integrated USB-PHY
 - Integrated 3.3-V and 1.8-V USB Power System
 - Integrated USB-PLL
 - Eight Input, Eight Output Endpoints
- 10-Bit Analog-to-Digital (A/D) Converter With Window Comparator
- Comparator
- Hardware Multiplier Supporting 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Three Channel Internal DMA
- Basic Timer With Real-Time Clock Feature
- Family Members are Summarized in [Table 1](#)
- For Complete Module Descriptions, See the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#))



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DESCRIPTION

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 5 μ s.

The MSP430F5510, MSP430F5509, and MSP430F5508 devices are microcontroller configurations with integrated USB and PHY supporting USB 2.0, four 16-bit timers, a high-performance 10-bit analog-to-digital converter (ADC), two universal serial communication interfaces (USCI), hardware multiplier, DMA, real-time clock module with alarm capabilities, and 31 or 47 I/O pins.

The MSP430F5507, MSP430F5506, MSP430F5505, and MSP430F5504 devices are microcontroller configurations with integrated USB and PHY supporting USB 2.0, four 16-bit timers, a high-performance 10-bit analog-to-digital converter (ADC), two universal serial communication interfaces (USCI), hardware multiplier, DMA, real-time clock module with alarm capabilities, and 31 I/O pins.

The MSP430F5503, MSP430F5502, and MSP430F5500 include all of these peripherals but have a comparator instead of the 10-bit ADC.

Typical applications include analog and digital sensor systems and data loggers that require connectivity to various USB hosts.

Family members available are summarized in [Table 1](#).

Table 1. Family Members

DEVICE	PROGRAM MEMORY (KB)	SRAM (KB) ⁽¹⁾	Timer_A ⁽²⁾	Timer_B ⁽³⁾	USCI		ADC10_A (CH)	Comp_B (CH)	I/O	PACKAGE TYPE
					CHANNEL A: UART, LIN, IrDA, SPI	CHANNEL B: SPI, I ² C				
MSP430F5510	32	4 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					1	1	6 ext, 2 int	4	31	48 PT, 48 RGZ
MSP430F5509	24	4 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					1	1	6 ext, 2 int	4	31	48 PT, 48 RGZ
MSP430F5508	16	4 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					1	1	6 ext, 2 int	4	31	48 PT, 48 RGZ
MSP430F5507	32	4 + 2	5, 3, 3	7	1	1	6 ext, 2 int	-	31	48 RGZ
MSP430F5506	24	4 + 2	5, 3, 3	7	1	1	6 ext, 2 int	-	31	48 RGZ
MSP430F5505	16	4 + 2	5, 3, 3	7	1	1	6 ext, 2 int	-	31	48 RGZ
MSP430F5504	8	4 + 2	5, 3, 3	7	1	1	6 ext, 2 int	-	31	48 PT, 48 RGZ
MSP430F5503	32	4 + 2	5, 3, 3	7	1	1	-	4	31	48 RGZ
MSP430F5502	24	4 + 2	5, 3, 3	7	1	1	-	4	31	48 RGZ
MSP430F5501	16	4 + 2	5, 3, 3	7	1	1	-	4	31	48 RGZ
MSP430F5500	8	4 + 2	5, 3, 3	7	1	1	-	4	31	48 RGZ

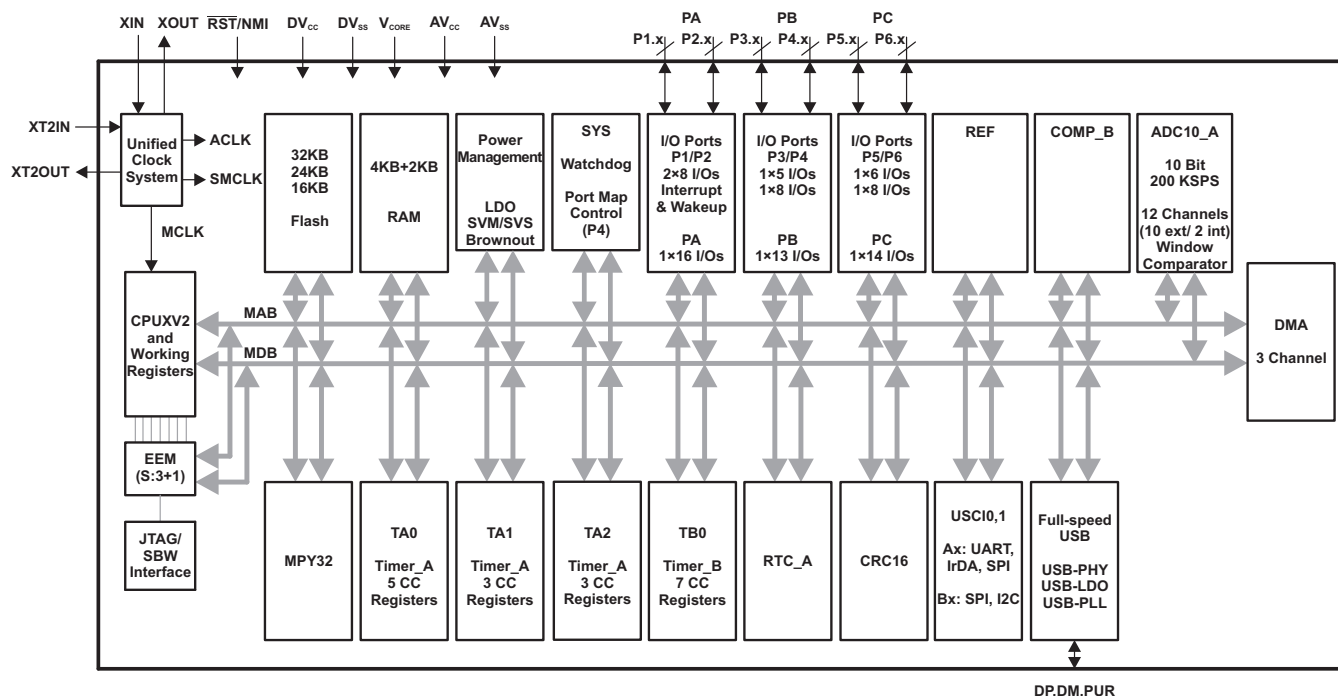
- (1) The additional 2-KB USB SRAM that is listed can be used as general purpose SRAM when USB is not in use.
- (2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (3) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

Table 2. Ordering Information⁽¹⁾

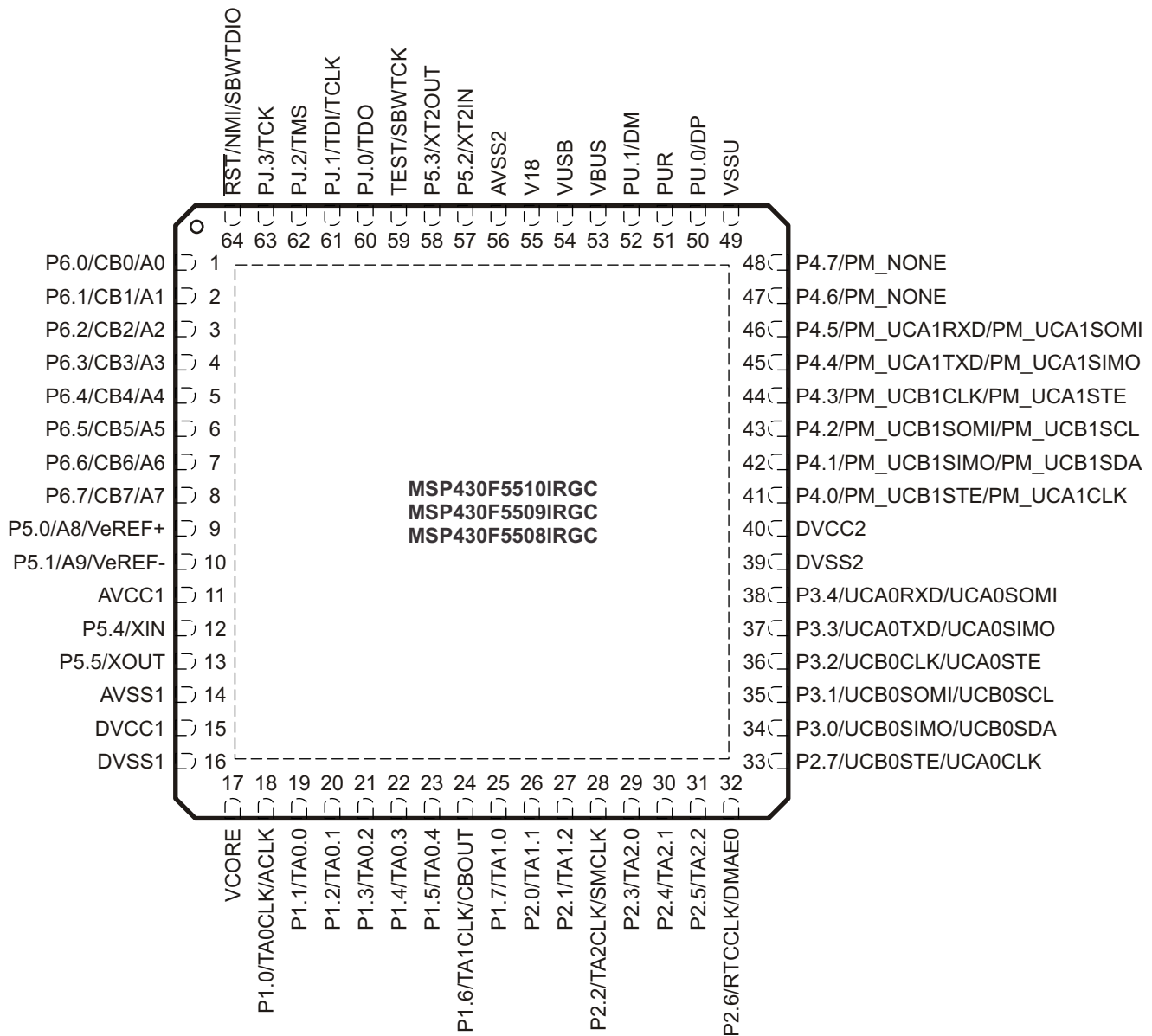
T _A	PACKAGED DEVICES ⁽²⁾			
	PLASTIC 64-PIN VQFN (RGC)	PLASTIC 80-BALL BGA (ZQE)	PLASTIC 48-PIN VQFN (RGZ)	PLASTIC 48-PIN LQFP (PT)
–40°C to 85°C	MSP430F5510IRGC	MSP430F5510IZQE	MSP430F5510IRGZ	MSP430F5510IPT
	MSP430F5509IRGC	MSP430F5509IZQE	MSP430F5509IRGZ	MSP430F5509IPT
	MSP430F5508IRGC	MSP430F5508IZQE	MSP430F5508IRGZ	MSP430F5508IPT
			MSP430F5507IRGZ	MSP430F5504IPT
			MSP430F5506IRGZ	
			MSP430F5505IRGZ	
			MSP430F5504IRGZ	
			MSP430F5503IRGZ	
			MSP430F5502IRGZ	
			MSP430F5501IRGZ	
			MSP430F5500IRGZ	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

**Functional Block Diagram – MSP430F5510IRGC, MSP430F5509IRGC, MSP430F5508IRGC,
MSP430F5510IZQE, MSP430F5509IZQE, MSP430F5508IZQE**


Pin Designation – MSP430F5510IRGC, MSP430F5509IRGC, MSP430F5508IRGC

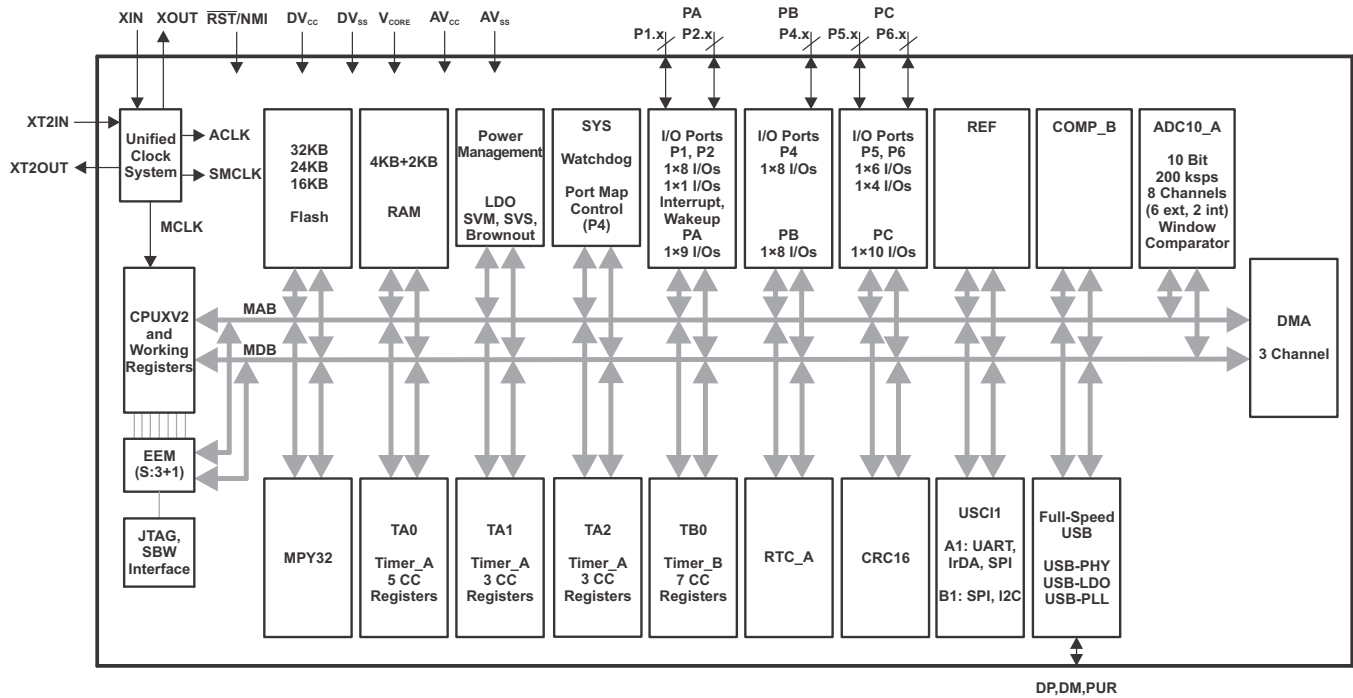


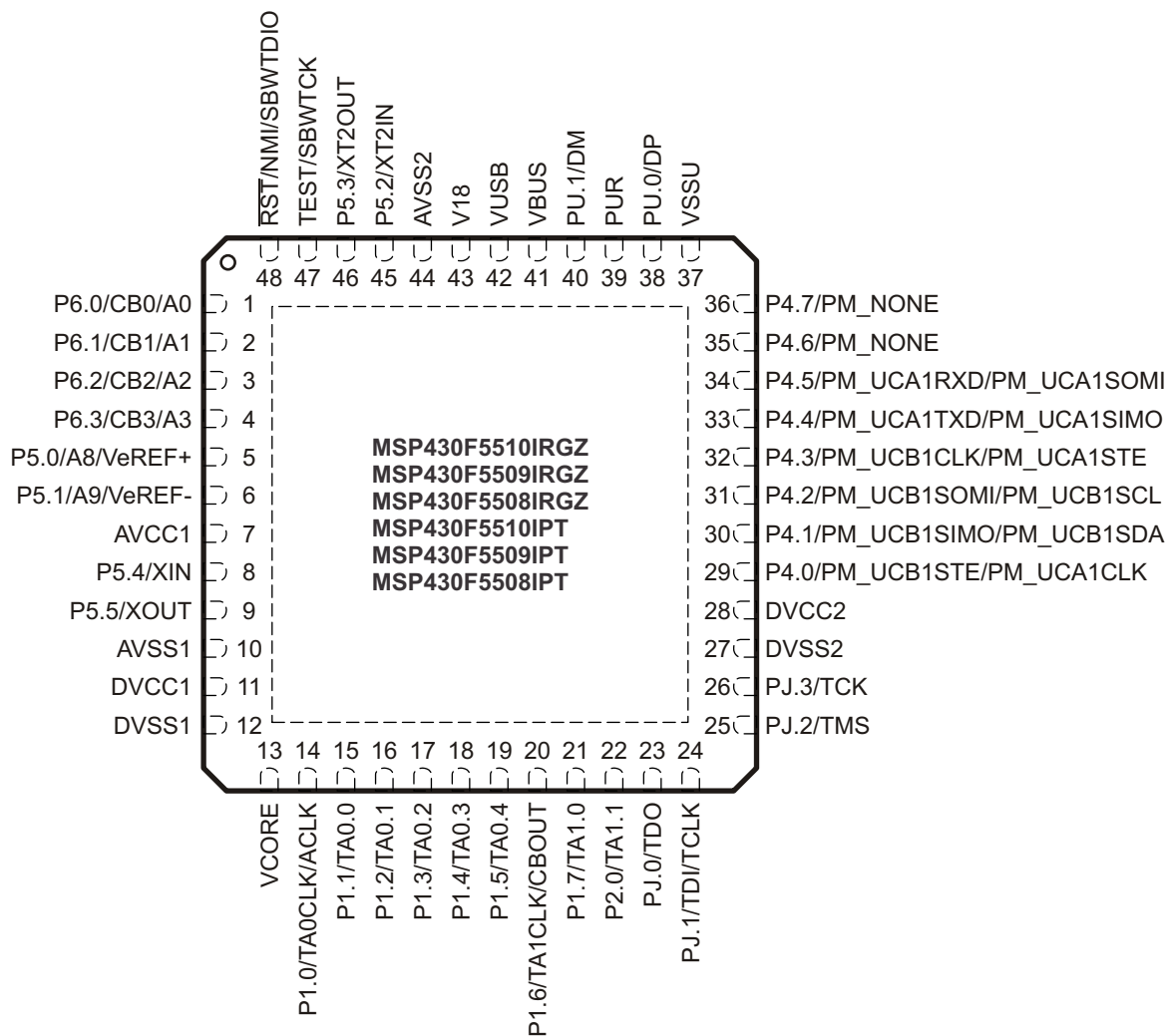
NOTE: TI recommends connection of the exposed thermal pad to V_{SS}.

Pin Designation – MSP430F5510IZQE, MSP430F5509IZQE, MSP430F5508IZQE**ZQE PACKAGE
(TOP VIEW)**

(A1)	(A2)	(A3)	(A4)	(A5)	(A6)	(A7)	(A8)	(A9)
(B1)	(B2)	(B3)	(B4)	(B5)	(B6)	(B7)	(B8)	(B9)
(C1)	(C2)		(C4)	(C5)	(C6)	(C7)	(C8)	(C9)
(D1)	(D2)	(D3)	(D4)	(D5)	(D6)	(D7)	(D8)	(D9)
(E1)	(E2)	(E3)	(E4)	(E5)	(E6)	(E7)	(E8)	(E9)
(F1)	(F2)	(F3)	(F4)	(F5)	(F6)	(F7)	(F8)	(F9)
(G1)	(G2)	(G3)	(G4)	(G5)	(G6)	(G7)	(G8)	(G9)
(H1)	(H2)	(H3)	(H4)	(H5)	(H6)	(H7)	(H8)	(H9)
(J1)	(J2)	(J3)	(J4)	(J5)	(J6)	(J7)	(J8)	(J9)

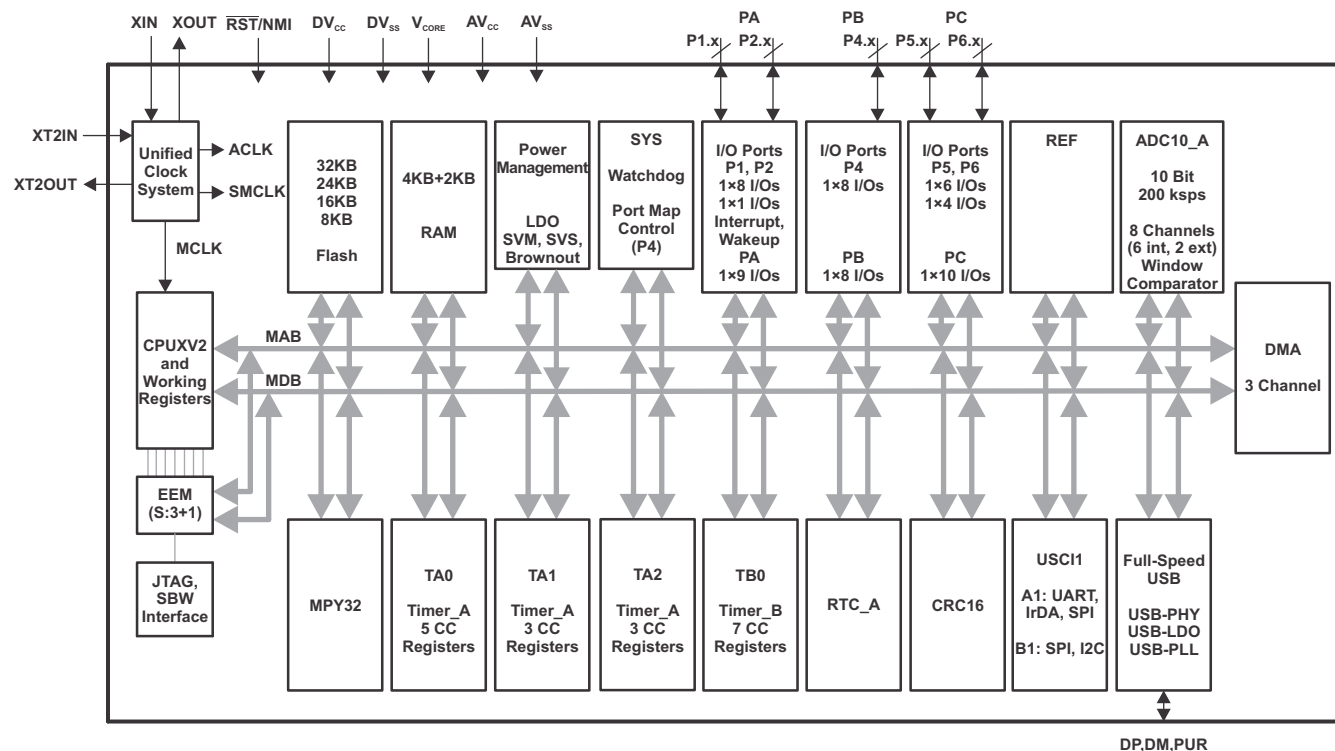
**Functional Block Diagram – MSP430F5510IRGZ, MSP430F5509IRGZ, MSP430F5508IRGZ,
MSP430F5510IPT, MSP430F5509IPT, MSP430F5508IPT**

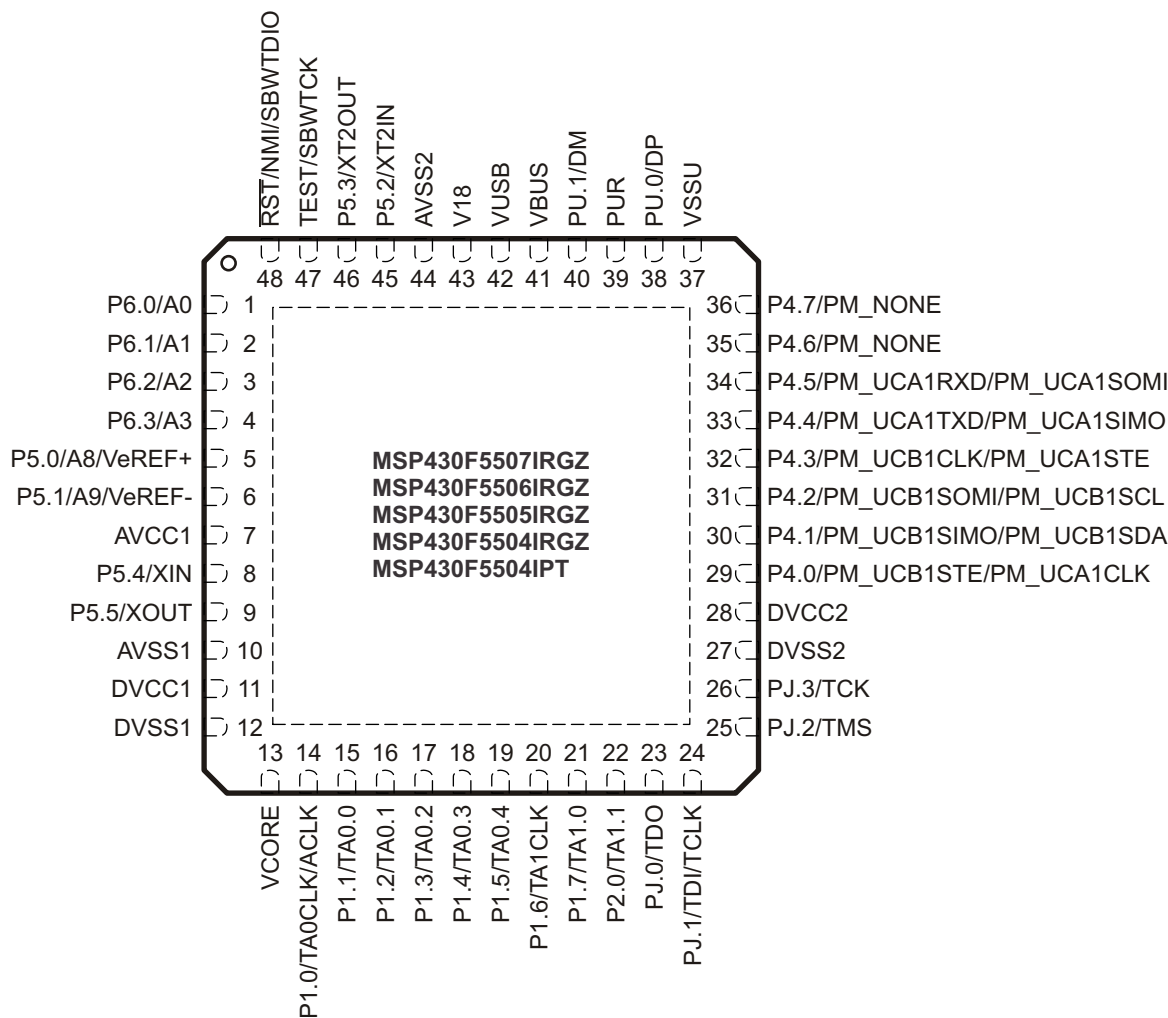


**Pin Designation – MSP430F5510IRGZ, MSP430F5509IRGZ, MSP430F5508IRGZ,
MSP430F5510IPT, MSP430F5509IPT, MSP430F5508IPT**


NOTE: TI recommends connection of the exposed thermal pad to V_{SS}.

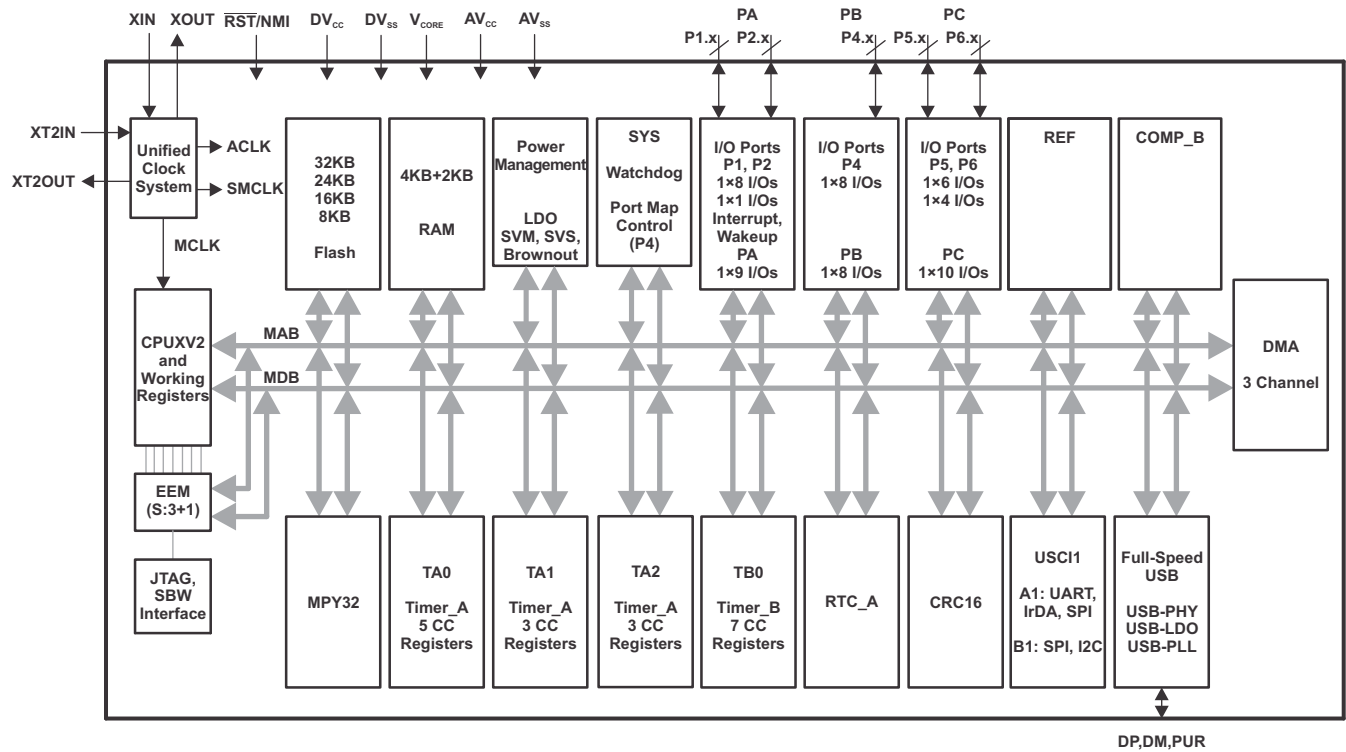
**Functional Block Diagram – MSP430F5507IRGZ, MSP430F5506IRGZ, MSP430F5505IRGZ,
MSP430F5504IRGZ, MSP430F5504IPT**

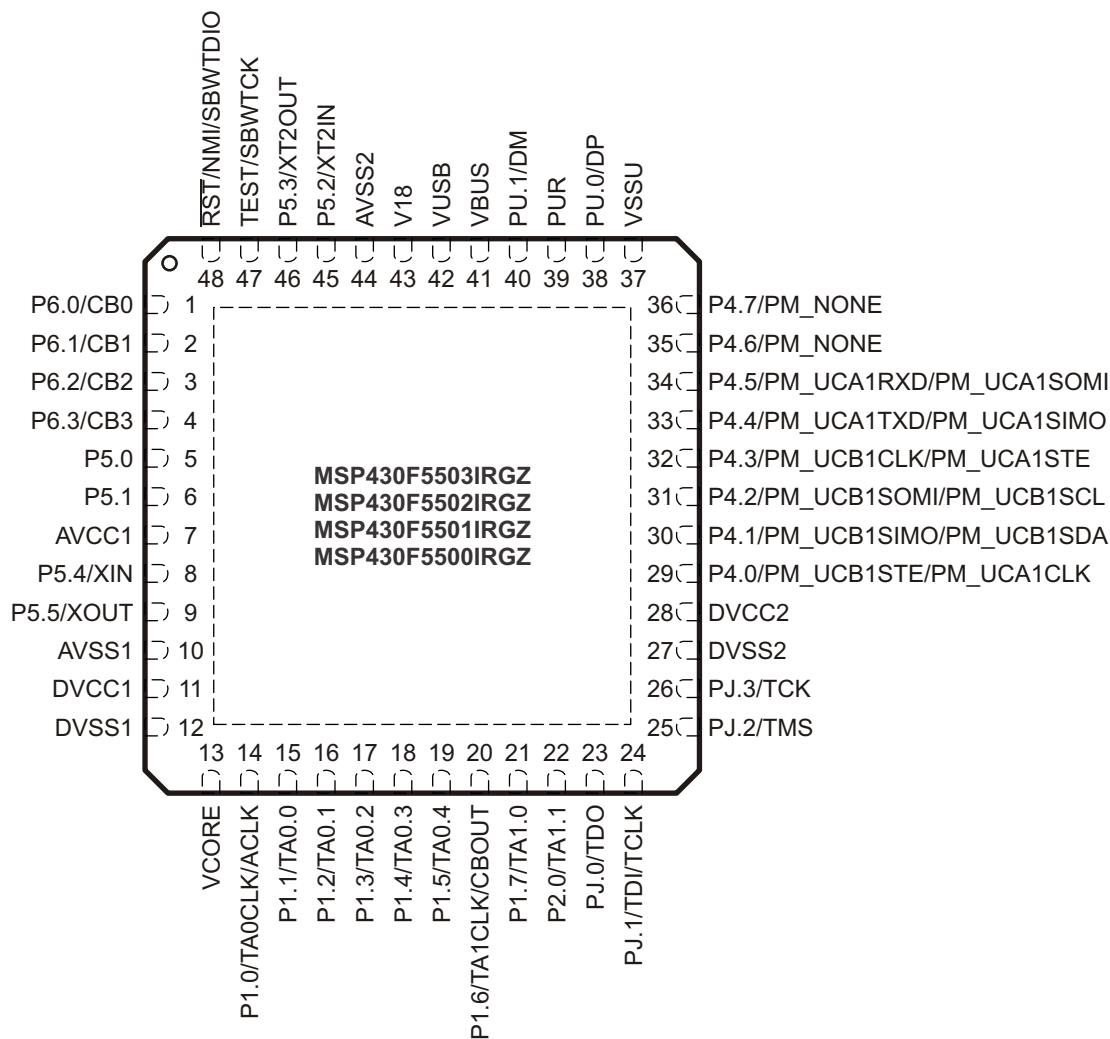


**Pin Designation – MSP430F5507IRGZ, MSP430F5506IRGZ, MSP430F5505IRGZ,
MSP430F5504IRGZ, MSP430F5504IPT**


NOTE: TI recommends connection of the exposed thermal pad to V_{SS}.

**Functional Block Diagram – MSP430F5503IRGZ, MSP430F5502IRGZ, MSP430F5501IRGZ,
MSP430F5500IRGZ**



**Pin Designation – MSP430F5503IRGZ, MSP430F5502IRGZ, MSP430F5501IRGZ,
MSP430F5500IRGZ**


NOTE: TI recommends connection of the exposed thermal pad to V_{SS}.

Table 3. Terminal Functions

TERMINAL				I/O ⁽¹⁾	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P6.4/CB4/A4	5	N/A	C1	I/O	General-purpose digital I/O Comparator_B input CB4 (not available on PT and RGZ package devices) Analog input A4 – ADC (not available on PT and RGZ package devices)
P6.5/CB5/A5	6	N/A	D2	I/O	General-purpose digital I/O Comparator_B input CB5 (not available on PT and RGZ package devices) Analog input A5 – ADC (not available on PT and RGZ package devices)
P6.6/CB6/A6	7	N/A	D1	I/O	General-purpose digital I/O Comparator_B input CB6 (not available on PT and RGZ package devices) Analog input A6 – ADC (not available on PT and RGZ package devices)
P6.7/CB7/A7	8	N/A	D3	I/O	General-purpose digital I/O Comparator_B input CB7 (not available on PT and RGZ package devices) Analog input A7 – ADC (not available on PT and RGZ package devices)
P5.0/A8/VeREF+	9	5	E1	I/O	General-purpose digital I/O Analog input A8 – ADC (not available on F5503, F5502, F5501, F5500 devices) Input for an external reference voltage to the ADC (not available on F5503, F5502, F5501, F5500 devices)
P5.1/A9/VeREF-	10	6	E2	I/O	General-purpose digital I/O Analog input A9 – ADC (not available on F5503, F5502, F5501, F5500 devices) Negative terminal for an externally provided ADC reference (not available on F5503, F5502, F5501, F5500 devices)
AVCC1	11	7	F2		Analog power supply
P5.4/XIN	12	8	F1	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P5.5/XOUT	13	9	G1	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS1	14	10	G2		Analog ground supply
DVCC1	15	11	H1		Digital power supply
DVSS1	16	12	J1		Digital ground supply
VCORE ⁽²⁾	17	13	J2		Regulated core power supply output (internal use only, no external current loading)
P1.0/TA0CLK/ACLK	18	14	H2	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0	19	15	H3	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	20	16	J3	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	21	17	G4	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	22	18	H4	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	23	19	J4	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA1CLK/CBOUT	24	20	G5	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output
P1.7/TA1.0	25	21	H5	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output

(1) I = input, O = output, N/A = not available

(2) VCore is for internal use only. No external current loading is possible. VCore should only be connected to the recommended capacitor value, C_{VCore} (see [Recommended Operating Conditions](#)).

Table 3. Terminal Functions (continued)

TERMINAL				I/O ⁽¹⁾	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P2.0/TA1.1	26	22	J5	I/O	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.1/TA1.2	27	N/A	G6	I/O	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.2/TA2CLK/SMCLK	28	N/A	J6	I/O	General-purpose digital I/O with port interrupt TA2 clock signal TA2CLK input SMCLK output
P2.3/TA2.0	29	N/A	H6	I/O	General-purpose digital I/O with port interrupt TA2 CCR0 capture: CCI0A input, compare: Out0 output
P2.4/TA2.1	30	N/A	J7	I/O	General-purpose digital I/O with port interrupt TA2 CCR1 capture: CCI1A input, compare: Out1 output
P2.5/TA2.2	31	N/A	J8	I/O	General-purpose digital I/O with port interrupt TA2 CCR2 capture: CCI2A input, compare: Out2 output
P2.6/RTCCLK/DMAE0	32	N/A	J9	I/O	General-purpose digital I/O with port interrupt RTC clock output for calibration DMA external trigger input
P2.7/UCB0STE/UCA0CLK	33	N/A	H7	I/O	General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.0/UCB0SIMO/UCB0SDA	34	N/A	H8	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode
P3.1/UCB0SOMI/UCB0SCL	35	N/A	H9	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode
P3.2/UCB0CLK/UCA0STE	36	N/A	G8	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
P3.3/UCA0TXD/UCA0SIMO	37	N/A	G9	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.4/UCA0RXD/UCA0SOMI	38	N/A	G7	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
P4.0/PM_UCB1STE/ PM_UCA1CLK	41	29	E8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode
P4.1/PM_UCB1SIMO/ PM_UCB1SDA	42	30	E7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I2C data – USCI_B1 I2C mode
P4.2/PM_UCB1SOMI/ PM_UCB1SCL	43	31	D9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I2C clock – USCI_B1 I2C mode
P4.3/PM_UCB1CLK/ PM_UCA1STE	44	32	D8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode
DVSS2	39	27	F9		Digital ground supply
DVCC2	40	28	E9		Digital power supply

Table 3. Terminal Functions (continued)

TERMINAL				I/O ⁽¹⁾	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P4.4/PM_UCA1TXD/ PM_UCA1SIMO	45	33	D7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	46	34	C9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode
P4.6/PM_NONE	47	35	C8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P4.7/PM_NONE	48	36	C7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
VSSU	49	37	B8, B9		USB PHY ground supply
PU.0/DP	50	38	A9	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DP
PUR	51	39	B7	I/O	USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL. Recommended 1-MΩ resistor to ground. See USB BSL for more information.
PU.1/DM	52	40	A8	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DM
VBUS	53	41	A7		USB LDO input (connect to USB power source)
VUSB	54	42	A6		USB LDO output
V18	55	43	B6		USB regulated power (internal use only, no external current loading)
AVSS2	56	44	A5		Analog ground supply
P5.2/XT2IN	57	45	B5	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	58	46	B4	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK	59	47	A4	I	Test mode pin – select digital I/O on JTAG pins Spy-By-Wire input clock
PJ.0/TDO	60	23	C5	I/O	General-purpose digital I/O Test data output port
PJ.1/TDI/TCLK	61	24	C4	I/O	General-purpose digital I/O Test data input or test clock input
PJ.2/TMS	62	25	A3	I/O	General-purpose digital I/O Test mode select
PJ.3/TCK	63	26	B3	I/O	General-purpose digital I/O Test clock
$\overline{\text{RST}}$ /NMI/SBWTIO	64	48	A2	I/O	Reset input active low Non-maskable interrupt input Spy-By-Wire data input/output
P6.0/CB0/A0	1	1	A1	I/O	General-purpose digital I/O Comparator_B input CB0 (not available on F5507, F5506, F5505, F5504 devices) Analog input A0 – ADC (not available on F5503, F5502, F5501, F5500 devices)
P6.1/CB1/A1	2	2	B2	I/O	General-purpose digital I/O Comparator_B input CB1 (not available on F5507, F5506, F5505, F5504 devices) Analog input A1 – ADC (not available on F5503, F5502, F5501, F5500 devices)

Table 3. Terminal Functions (continued)

TERMINAL				I/O ⁽¹⁾	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P6.2/CB2/A2	3	3	B1	I/O	General-purpose digital I/O Comparator_B input CB2 (not available on F5507, F5506, F5505, F5504 devices) Analog input A2 – ADC (not available on F5503, F5502, F5501, F5500 devices)
P6.3/CB3/A3	4	4	C2	I/O	General-purpose digital I/O Comparator_B input CB3 (not available on F5507, F5506, F5505, F5504 devices) Analog input A3 – ADC (not available on F5503, F5502, F5501, F5500 devices)
Reserved	N/A	N/A	(3)		
QFN Pad	Pad	Pad	N/A		Exposed QFN package pad. Connection to V _{SS} recommended (not available on PT package devices)

(3) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.

SHORT-FORM DESCRIPTION

CPU ([Link to User's Guide](#))

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

Operating Modes

The MSP430 devices have one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and FLL loop control and DCOCLK are disabled
 - DCO's dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's dc generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's dc generator is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No data retention
 - Wakeup from $\overline{\text{RST}}$ /NMI, P1, and P2.

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 4. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Timeout, Password Violation Flash Memory Password Violation	WDTIFG, KEYV (SYSRSTIV) ^{(1) (2)}	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRILIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ⁽¹⁾	(Non)maskable	0FFFCCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) ^{(1) (2)}	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV) ^{(1) (3)}	Maskable	0FFF8h	60
TB0	TB0CCR0 CCIFG0 ⁽³⁾	Maskable	0FFF6h	59
TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV) ^{(1) (3)}	Maskable	0FFF4h	58
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 Receive or Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV) ^{(1) (3)}	Maskable	0FFF0h	56
USCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV) ^{(1) (3)}	Maskable	0FFEEh	55
ADC10_A	ADC10IFG0 ^{(1) (3) (4)}	Maskable	0FFECCh	54
TA0	TA0CCR0 CCIFG0 ⁽³⁾	Maskable	0FFEAh	53
TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) ^{(1) (3)}	Maskable	0FFE8h	52
USB_UBM	USB interrupts (USBIV) ^{(1) (3)}	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ^{(1) (3)}	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0 ⁽³⁾	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) ^{(1) (3)}	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV) ^{(1) (3)}	Maskable	0FFDEh	47
USCI_A1 Receive or Transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV) ^{(1) (3)}	Maskable	0FFDCh	46
USCI_B1 Receive or Transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV) ^{(1) (3)}	Maskable	0FFDAh	45
TA2	TA2CCR0 CCIFG0 ⁽³⁾	Maskable	0FFD8h	44
TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV) ^{(1) (3)}	Maskable	0FFD6h	43
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV) ^{(1) (3)}	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) ^{(1) (3)}	Maskable	0FFD2h	41
Reserved	Reserved ⁽⁵⁾		0FFD0h	40
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(3) Interrupt flags are located in the module.

(4) Only on devices with ADC, otherwise reserved.

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Memory Organization

Table 5. Memory Organization⁽¹⁾

		MSP430F5504 MSP430F5500	MSP430F5508 MSP430F5505 MSP430F5501	MSP430F5509 MSP430F5506 MSP430F5502	MSP430F5510 MSP430F5507 MSP430F5503
Memory (flash) Main: interrupt vector Main: code memory	Total Size	8 KB 00FFFFh–00FF80h 00FFFFh–00E000h	16 KB 00FFFFh–00FF80h 00FFFFh–00C000h	24 KB 00FFFFh–00FF80h 00FFFFh–00A000h	32 KB 00FFFFh–00FF80h 00FFFFh–008000h
RAM	Sector 1	2 KB 0033FFh–002C00h	2 KB 0033FFh–002C00h	2 KB 0033FFh–002C00h	2 KB 0033FFh–002C00h
	Sector 0	2 KB 002BFFh–002400h	2 KB 002BFFh–002400h	2 KB 002BFFh–002400h	2 KB 002BFFh–002400h
USB RAM ⁽²⁾		2 KB 0023FFh–001C00h	2 KB 0023FFh–001C00h	2 KB 0023FFh–001C00h	2 KB 0023FFh–001C00h
Information memory (flash)	Info A	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h
	Info B	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h
	Info C	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info D	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootstrap loader (BSL) memory (flash)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4 KB 000FFFh–0h	4 KB 000FFFh–0h	4 KB 000FFFh–0h	4 KB 000FFFh–0h

(1) N/A = Not available

(2) USB RAM can be used as general purpose RAM when not used for USB operation.

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory via the BSL is protected by an user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

USB BSL

All devices come pre-programmed with the USB BSL. Use of the USB BSL requires external access to the six pins shown in Table 6. In addition to these pins, the application must support external components necessary for normal USB operation (for example, proper crystal on XT2IN and XT2OUT and proper decoupling). For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278).

Table 6. USB BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	Entry sequence signal
PU.0/DP	USB data terminal DP
PU.1/DM	USB data terminal DM
PUR	USB pullup resistor terminal
VBUS	USB bus power supply
VSSU	USB ground supply

NOTE

The default USB BSL evaluates the logic level of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless the BSL should be invoked, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. Applying a 1-M Ω resistor to ground is recommended.

UART BSL

A UART BSL is also available that can be programmed by the user into the BSL memory by replacing the pre-programmed factory-supplied USB BSL. Use of the UART BSL requires external access to the six pins shown in Table 7. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278).

Table 7. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

JTAG Operation

JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in [Table 8](#). For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)). For complete description of the features of the JTAG interface and its implementation, see the *MSP430 Memory Programming via the JTAG Interface User's Guide* ([SLAU320](#)).

Table 8. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	IN	External reset
VCC		Power supply
VSS		Ground supply

Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in [Table 9](#). For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)). For complete description of the features of the JTAG interface and its implementation, see the *MSP430 Memory Programming via the JTAG Interface User's Guide* ([SLAU320](#)).

Table 9. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

Flash Memory ([Link to User's Guide](#))

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory ([Link to User's Guide](#))

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sectors. The size of a sector can be found in [Memory Organization](#).
- Each sector 0 to n can be completely disabled, however data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.
- For Devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

Digital I/O ([Link to User's Guide](#))

There are up to six 8-bit I/O ports implemented: For 64-pin options, P1, P2, P4, P6, and are complete, P5 is reduced to 6-bit I/O and P3 to 5-bit I/O. For 48-pin options, P6 is reduced to 4-bit I/O, P2 to 1-bit I/O, and P3 is completely removed. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wakeup input capability is available for all bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P6) or word-wise in pairs (PA through PC).

Port Mapping Controller ([Link to User's Guide](#))

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4.

Table 10. Port Mapping, Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_CBOUT0	-	Comparator_B output
	PM_TB0CLK	TB0 clock input	
2	PM_ADC10CLK	-	ADC10CLK
	PM_DMAE0	DMAE0 input	
3	PM_SVMOUT	-	SVM output
	PM_TB0OUTH	TB0 high impedance input TB0OUTH	
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6
11	PM_UCA1RXD	USCI_A1 UART RXD (Direction controlled by USCI - input)	
	PM_UCA1SOMI	USCI_A1 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA1TXD	USCI_A1 UART TXD (Direction controlled by USCI - output)	
	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA1CLK	USCI_A1 clock input/output (direction controlled by USCI)	
	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)	

Table 10. Port Mapping, Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
14	PM_UCB1SOMI	USCI_B1 SPI slave out master in (direction controlled by USCI)	
	PM_UCB1SCL	USCI_B1 I2C clock (open drain and direction controlled by USCI)	
15	PM_UCB1SIMO	USCI_B1 SPI slave in master out (direction controlled by USCI)	
	PM_UCB1SDA	USCI_B1 I2C data (open drain and direction controlled by USCI)	
16	PM_UCB1CLK	USCI_B1 clock input/output (direction controlled by USCI)	
	PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI)	
17	PM_CBOUT1	None	Comparator_B output
18	PM_MCLK	None	MCLK
19	PM_RTCCLK	None	RTCCLK output
20	PM_UCA0RXD	USCI_A0 UART RXD (Direction controlled by USCI - input)	
	PM_UCA0SOMI	USCI_A0 SPI slave out master in (direction controlled by USCI)	
21	PM_UCA0TXD	USCI_A0 UART TXD (Direction controlled by USCI - output)	
	PM_UCA0SIMO	USCI_A0 SPI slave in master out (direction controlled by USCI)	
22	PM_UCA0CLK	USCI_A0 clock input/output (direction controlled by USCI)	
	PM_UCB0STE	USCI_B0 SPI slave transmit enable (direction controlled by USCI)	
23	PM_UCB0SOMI	USCI_B0 SPI slave out master in (direction controlled by USCI)	
	PM_UCB0SCL	USCI_B0 I2C clock (open drain and direction controlled by USCI)	
24	PM_UCB0SIMO	USCI_B0 SPI slave in master out (direction controlled by USCI)	
	PM_UCB0SDA	USCI_B0 I2C data (open drain and direction controlled by USCI)	
25	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)	
	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI)	
26 - 30	Reserved	None	DVSS
31 (0FFh) ⁽¹⁾	PM_ANALOG	Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored resulting in a read out value of 31.

Table 11. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P4.0/P4MAP0	PM_UCB1STE/PM_UCA1CLK	USCI_B1 SPI slave transmit enable (direction controlled by USCI) USCI_A1 clock input/output (direction controlled by USCI)	
P4.1/P4MAP1	PM_UCB1SIMO/PM_UCB1SDA	USCI_B1 SPI slave in master out (direction controlled by USCI) USCI_B1 I2C data (open drain and direction controlled by USCI)	
P4.2/P4MAP2	PM_UCB1SOMI/PM_UCB1SCL	USCI_B1 SPI slave out master in (direction controlled by USCI) USCI_B1 I2C clock (open drain and direction controlled by USCI)	
P4.3/P4MAP3	PM_UCB1CLK/PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI) USCI_B1 clock input/output (direction controlled by USCI)	
P4.4/P4MAP4	PM_UCA1TXD/PM_UCA1SIMO	USCI_A1 UART TXD (Direction controlled by USCI - output) USCI_A1 SPI slave in master out (direction controlled by USCI)	
P4.5/P4MAP5	PM_UCA1RXD/PM_UCA1SOMI	USCI_A1 UART RXD (Direction controlled by USCI - input) USCI_A1 SPI slave out master in (direction controlled by USCI)	
P4.6/P4MAP6	PM_NONE	None	DVSS
P4.7/P4MAP7	PM_NONE	None	DVSS

Oscillator and System Clock ([Link to User's Guide](#))

The clock system in the MSP430F550x family of devices is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 μ s. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM) ([Link to User's Guide](#))

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Hardware Multiplier (MPY) ([Link to User's Guide](#))

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

Real-Time Clock (RTC_A) ([Link to User's Guide](#))

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

Watchdog Timer (WDT_A) ([Link to User's Guide](#))

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

System Module (SYS) ([Link to User's Guide](#))

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, boot strap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 12. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$ /NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Wakeup from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT timeout (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

DMA Controller ([Link to User's Guide](#))

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion register to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

The USB timestamp generator also utilizes the DMA trigger assignments described in [Table 13](#).

Table 13. DMA Trigger Assignments⁽¹⁾

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC10IFG0 ⁽²⁾	ADC10IFG0 ⁽²⁾	ADC10IFG0 ⁽²⁾
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	USB FNRXD	USB FNRXD	USB FNRXD
28	USB ready	USB ready	USB ready
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) If a reserved trigger source is selected, no Trigger1 is generated.

(2) Only on devices with ADC. Reserved on devices without ADC.

Universal Serial Communication Interface (USCI) (Links to User's Guide: [UART Mode](#), [SPI Mode](#), [I2C Mode](#))

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3 pin or 4 pin) or I2C.

The MSP430F55xx series includes two complete USCI modules (n = 0, 1).

TA0 (Link to User's Guide)

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 14. TA0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
18, H2-P1.0	14-P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
18, H2-P1.0	14-P1.0	TA0CLK	$\overline{\text{TACLK}}$					
19, H3-P1.1	15-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	19, H3-P1.1	15-P1.1
		DV _{SS}	CCI0B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
20, J3-P1.2	16-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	20, J3-P1.2	16-P1.2
		CBOUT (internal)	CCI1B				ADC10 (internal) ⁽¹⁾ ADC10SHSx = {1}	ADC10 (internal) ⁽¹⁾ ADC10SHSx = {1}
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
21, G4-P1.3	17-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	21, G4-P1.3	17-P1.3
		ACLK (internal)	CCI2B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
22, H4-P1.4	18-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	22, H4-P1.4	18-P1.4
		DV _{SS}	CCI3B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
23, J4-P1.5	19-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	23, J4-P1.5	19-P1.5
		DV _{SS}	CCI4B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					

(1) Only on devices with ADC.

TA1 ([Link to User's Guide](#))

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 15. TA1 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
24, G5-P1.6	20-P1.6	TA1CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
24, G5-P1.6	20-P1.6	TA1CLK	$\overline{\text{TACLK}}$					
25, H5-P1.7	21-P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	25, H5-P1.7	21-P1.7
		DV _{SS}	CCI0B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
26, J5-P2.0	22-P2.0	TA1.1	CCI1A	CCR1	TA1	TA1.1	26, J5-P2.0	22-P2.0
		CBOUT (internal)	CCI1B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
27, G6-P2.1		TA1.2	CCI2A	CCR2	TA2	TA1.2	27, G6-P2.1	
		ACLK (internal)	CCI2B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					

TA2 (Link to User's Guide)

TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 16. TA2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
28, J6-P2.2		TA2CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
28, J6-P2.2		TA2CLK	$\overline{\text{TACLK}}$					
29, H6-P2.3		TA2.0	CCI0A	CCR0	TA0	TA2.0	29, H6-P2.3	
		DV _{SS}	CCI0B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
30, J7-P2.4		TA2.1	CCI1A	CCR1	TA1	TA2.1	30, J7-P2.4	
		CBOUT (internal)	CCI1B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
31, J8-P2.5		TA2.2	CCI2A	CCR2	TA2	TA2.2	31, J8-P2.5	
		ACLK (internal)	CCI2B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					

TB0 (Link to User's Guide)

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 17. TB0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE ⁽¹⁾	RGZ, PT ⁽¹⁾						RGC, ZQE ⁽¹⁾	RGZ, PT ⁽¹⁾
		TB0CLK	TBCLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
		TB0CLK	TBCLK					
		TB0.0	CCI0A	CCR0	TB0	TB0.0	ADC10 (internal) ⁽²⁾ ADC10SHSx = {2}	ADC10 (internal) ⁽²⁾ ADC10SHSx = {2}
		TB0.0	CCI0B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.1	CCI1A	CCR1	TB1	TB0.1	ADC10 (internal) ADC10SHSx = {3}	ADC10 (internal) ADC10SHSx = {3}
		CBOUT (internal)	CCI1B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.2	CCI2A	CCR2	TB2	TB0.2		
		TB0.2	CCI2B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.3	CCI3A	CCR3	TB3	TB0.3		
		TB0.3	CCI3B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.4	CCI4A	CCR4	TB4	TB0.4		
		TB0.4	CCI4B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.5	CCI5A	CCR5	TB5	TB0.5		
		TB0.5	CCI5B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					
		TB0.6	CCI6A	CCR6	TB6	TB0.6		
		ACLK (internal)	CCI6B					
		DV _{SS}	GND					
		DV _{CC}	V _{CC}					

(1) Timer functions selectable via the port mapping controller.

(2) Only on devices with ADC.

Comparator_B ([Link to User's Guide](#))

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

ADC10_A ([Link to User's Guide](#))

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

CRC16 ([Link to User's Guide](#))

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

REF Voltage Reference ([Link to User's Guide](#))

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

USB Universal Serial Bus ([Link to User's Guide](#))

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly-flexible and can support a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

Embedded Emulation Module (EEM) (S Version) ([Link to User's Guide](#))

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The S version of the EEM implemented on all devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

Peripheral File Map

Table 18. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 19)	0100h	000h-01Fh
PMM (see Table 20)	0120h	000h-01Fh
Flash Control (see Table 21)	0140h	000h-00Fh
CRC16 (see Table 22)	0150h	000h-007h
RAM Control (see Table 23)	0158h	000h-001h
Watchdog (see Table 24)	015Ch	000h-001h
UCS (see Table 25)	0160h	000h-01Fh
SYS (see Table 26)	0180h	000h-01Fh
Shared Reference (see Table 27)	01B0h	000h-001h
Port Mapping Control (see Table 28)	01C0h	000h-002h
Port Mapping Port P4 (see Table 28)	01E0h	000h-007h
Port P1, P2 (see Table 29)	0200h	000h-01Fh
Port P3, P4 (see Table 30)	0220h	000h-00Bh
Port P5, P6 (see Table 31)	0240h	000h-00Bh
Port PJ (see Table 32)	0320h	000h-01Fh
TA0 (see Table 33)	0340h	000h-02Eh
TA1 (see Table 34)	0380h	000h-02Eh
TB0 (see Table 35)	03C0h	000h-02Eh
TA2 (see Table 36)	0400h	000h-02Eh
Real-Time Clock (RTC_A) (see Table 37)	04A0h	000h-01Bh
32-bit Hardware Multiplier (see Table 38)	04C0h	000h-02Fh
DMA General Control (see Table 39)	0500h	000h-00Fh
DMA Channel 0 (see Table 39)	0510h	000h-00Ah
DMA Channel 1 (see Table 39)	0520h	000h-00Ah
DMA Channel 2 (see Table 39)	0530h	000h-00Ah
USCI_A0 (see Table 40)	05C0h	000h-01Fh
USCI_B0 (see Table 41)	05E0h	000h-01Fh
USCI_A1 (see Table 42)	0600h	000h-01Fh
USCI_B1 (see Table 43)	0620h	000h-01Fh
ADC10_A (see Table 44)	0740h	000h-01Fh
Comparator_B (see Table 45)	08C0h	000h-00Fh
USB configuration (see Table 46)	0900h	000h-014h
USB control (see Table 47)	0920h	000h-01Fh

Table 19. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 20. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high side control	SVSMHCTL	04h
SVS low side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM Power mode 5 control	PMM5CTL	10h

Table 21. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 22. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 23. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 24. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 25. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 26. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootstrap loader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 27. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

**Table 28. Port Mapping Registers
(Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)**

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping key/ID register	PMAPKEYID	00h
Port mapping control register	PMAPCTL	02h
Port P4.0 mapping register	P4MAP0	00h
Port P4.1 mapping register	P4MAP1	01h
Port P4.2 mapping register	P4MAP2	02h
Port P4.3 mapping register	P4MAP3	03h
Port P4.4 mapping register	P4MAP4	04h
Port P4.5 mapping register	P4MAP5	05h
Port P4.6 mapping register	P4MAP6	06h
Port P4.7 mapping register	P4MAP7	07h

Table 29. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 30. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

Table 31. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pullup/pulldown enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 32. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 33. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 34. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 35. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 register	TB0R	10h
Capture/compare register 0	TB0CCR0	12h
Capture/compare register 1	TB0CCR1	14h
Capture/compare register 2	TB0CCR2	16h
Capture/compare register 3	TB0CCR3	18h
Capture/compare register 4	TB0CCR4	1Ah
Capture/compare register 5	TB0CCR5	1Ch
Capture/compare register 6	TB0CCR6	1Eh
TB0 expansion register 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 36. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter register	TA2R	10h
Capture/compare register 0	TA2CCR0	12h
Capture/compare register 1	TA2CCR1	14h
Capture/compare register 2	TA2CCR2	16h
TA2 expansion register 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 37. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter register 1	RTCSEC/RTCNT1	10h
RTC minutes/counter register 2	RTCMIN/RTCNT2	11h
RTC hours/counter register 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter register 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

Table 38. 32-bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

**Table 39. DMA Registers (Base Address DMA General Control: 0500h,
DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)**

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Ah

Table 40. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA0CTL1	00h
USCI control 1	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 41. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 42. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA1CTL1	00h
USCI control 1	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 43. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 0	UCB1CTL1	00h
USCI synchronous control 1	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

Table 44. ADC10_A Registers (Base Address: 0740h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC10_A Control register 0	ADC10CTL0	00h
ADC10_A Control register 1	ADC10CTL1	02h
ADC10_A Control register 2	ADC10CTL2	04h
ADC10_A Window Comparator Low Threshold	ADC10LO	06h
ADC10_A Window Comparator High Threshold	ADC10HI	08h
ADC10_A Memory Control Register 0	ADC10MCTL0	0Ah
ADC10_A Conversion Memory Register	ADC10MEM0	12h
ADC10_A Interrupt Enable	ADC10IE	1Ah
ADC10_A Interrupt Flags	ADC10IGH	1Ch
ADC10_A Interrupt Vector Word	ADC10IV	1Eh

Table 45. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control register 0	CBCTL0	00h
Comp_B control register 1	CBCTL1	02h
Comp_B control register 2	CBCTL2	04h
Comp_B control register 3	CBCTL3	06h
Comp_B interrupt register	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

Table 46. USB Configuration Registers (Base Address: 0900h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USB key/ID	USBKEYID	00h
USB module configuration	USBCNF	02h
USB PHY control	USBPHYCTL	04h
USB power control	USBPWRCTL	08h
USB PLL control	USBPLLCTL	10h
USB PLL divider	USBPLLDIV	12h
USB PLL interrupts	USBPLLIR	14h

Table 47. USB Control Registers (Base Address: 0920h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Input endpoint#0 configuration	IEPCNF_0	00h
Input endpoint #0 byte count	IEPCNT_0	01h
Output endpoint#0 configuration	OEPCNF_0	02h
Output endpoint #0 byte count	OEPCNT_0	03h
Input endpoint interrupt enables	IEPIE	0Eh
Output endpoint interrupt enables	OEPIE	0Fh
Input endpoint interrupt flags	IEPIFG	10h
Output endpoint interrupt flags	OEPIFG	11h
USB interrupt vector	USBIV	12h
USB maintenance	MAINT	16h
Time stamp	TSREG	18h
USB frame number	USBFN	1Ah
USB control	USBCTL	1Ch
USB interrupt enables	USBIE	1Dh
USB interrupt flags	USBIFG	1Eh
Function address	FUNADR	1Fh

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

Voltage applied at V_{CC} to V_{SS}	–0.3 V to 4.1 V
Voltage applied to any pin (excluding V _{CORE} , V _{BUS} , V18) ⁽²⁾	–0.3 V to $V_{CC} + 0.3$ V
Diode current at any device pin	±2 mA
Storage temperature range, T_{stg} ⁽³⁾	–55°C to 150°C
Maximum junction temperature, T_J	95°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Thermal Packaging Characteristics⁽¹⁾

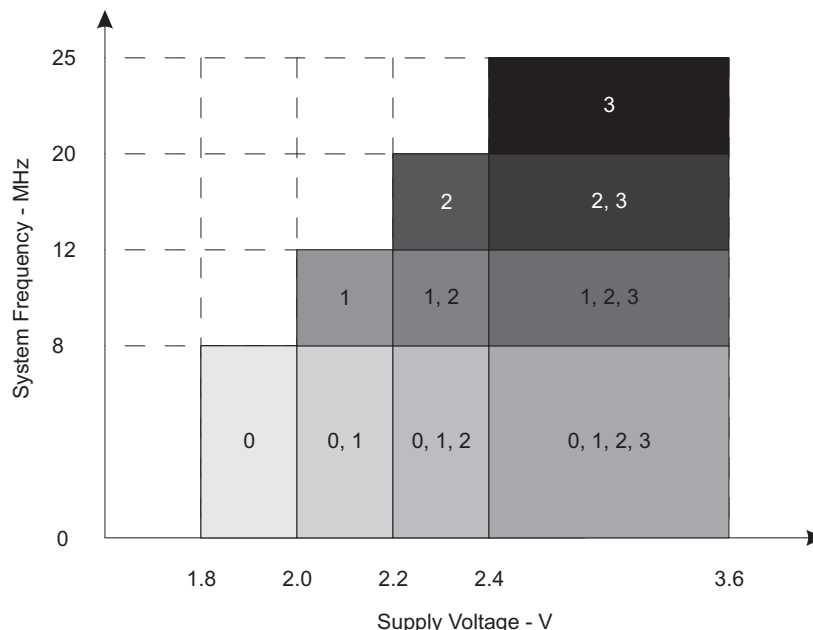
PARAMETER		VALUE	UNIT
θ_{JA} Junction-to-ambient thermal resistance, still air ⁽²⁾	VQFN (RGC)	30	°C/W
	VQFN (RGZ)	28.6	
	LQFP (PT)	62.8	
	BGA (ZQE)	55.5	
$\theta_{JC(TOP)}$ Junction-to-case (top) thermal resistance ⁽³⁾	VQFN (RGC)	15.6	°C/W
	VQFN (RGZ)	14.4	
	LQFP (PT)	18.2	
	BGA (ZQE)	21.2	
$\theta_{JC(BOTTOM)}$ Junction-to-case (bottom) thermal resistance ⁽⁴⁾	VQFN(RGC)	1.6	°C/W
	VQFN (RGZ)	1.6	
	LQFP (PT)	N/A	
	BGA (ZQE)	N/A	
θ_{JB} Junction-to-board thermal resistance ⁽⁵⁾	VQFN (RGC)	8.9	°C/W
	VQFN (RGZ)	5.5	
	LQFP (PT)	28.3	
	BGA (ZQE)	19.3	

- (1) N/A = not applicable
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-case(bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage during program execution and flash programming (AV _{CC} = DV _{CC}) ⁽¹⁾⁽²⁾	PMMCOREVx = 0	1.8	3.6	V
		PMMCOREVx = 0, 1	2.0	3.6	V
		PMMCOREVx = 0, 1, 2	2.2	3.6	V
		PMMCOREVx = 0, 1, 2, 3	2.4	3.6	V
V _{CC,USB}	Supply voltage during USB operation, USB PLL disabled, USB_EN = 1, UPLLEN = 0	PMMCOREVx = 0	1.8	3.6	V
		PMMCOREVx = 0, 1	2.0	3.6	V
		PMMCOREVx = 0, 1, 2	2.2	3.6	V
		PMMCOREVx = 0, 1, 2, 3	2.4	3.6	V
	Supply voltage during USB operation, USB PLL enabled ⁽³⁾ , USB_EN = 1, UPLLEN = 1	PMMCOREVx = 2	2.2	3.6	V
		PMMCOREVx = 2, 3	2.4	3.6	V
V _{SS}	Supply voltage (AV _{SS} = DV _{SS1/2} = DV _{SS})		0		V
T _A	Operating free-air temperature	I version	–40	85	°C
T _J	Operating junction temperature	I version	–40	85	°C
C _{VCORE}	Capacitor at V _{CORE}		470		nF
C _{DVCC} / C _{VCORE}	Capacitor ratio of DV _{CC} to V _{CORE}		10		
f _{SYSTEM}	Processor frequency (maximum MCLK frequency) ⁽⁴⁾ (see Figure 1)	PMMCOREVx = 0, 1.8 V ≤ V _{CC} ≤ 3.6 V (default condition)	0	8.0	MHz
		PMMCOREVx = 1, 2.0 V ≤ V _{CC} ≤ 3.6 V	0	12.0	
		PMMCOREVx = 2, 2.2 V ≤ V _{CC} ≤ 3.6 V	0	20.0	
		PMMCOREVx = 3, 2.4 V ≤ V _{CC} ≤ 3.6 V	0	25.0	
f _{SYSTEM_USB}	Minimum processor frequency for USB operation		1.5		MHz
USB_wait	Wait state cycles during USB operation		16		cycles

- (1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [PMM](#), [SVS High Side](#) threshold parameters for the exact values and further details.
- (3) USB operation with USB PLL enabled requires PMMCOREVx ≥ 2 for proper operation.
- (4) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 1. Maximum System Frequency

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

PARAMETER	EXECUTION MEMORY	V _{CC}	PMMCOREVx	FREQUENCY (f _{DCO} = f _{MCLK} = f _{SMCLK})										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{AM, Flash}	Flash	3 V	0	0.25	0.27	1.55	1.68							mA
			1	0.28		1.74		2.58	2.78					
			2	0.30		1.91		2.84		4.68	5.06			
			3	0.32		2.09		3.10		5.13		6.0	6.5	
I _{AM, RAM}	RAM	3 V	0	0.17	0.19	0.91	1.00							mA
			1	0.19		1.03		1.54	1.67					
			2	0.20		1.16		1.73		2.84	3.11			
			3	0.21		1.24		1.87		3.1		3.9	4.3	

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Characterized with program executing typical data processing. USB disabled ($V_{USBEN} = 0$, $SLDOEN = 0$).

$f_{ACLK} = 32786$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.

$XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0$.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

PARAMETER	V_{CC}	PMMCOREVx	-40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$ Low-power mode 0 ⁽³⁾⁽⁴⁾	2.2 V	0	73		77	85	80		85	97	μA
	3 V	3	79		83	92	88		95	105	
I_{LPM2} Low-power mode 2 ⁽⁵⁾⁽⁴⁾	2.2 V	0	6.5		6.5	8	7.5		8	11	μA
	3 V	3	7.0		7.0	9	7.9		8.9	13	
$I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ⁽⁶⁾⁽⁴⁾	2.2 V	0	1.60		1.90		2.6		3.4		μA
		1	1.65		2.00		2.7		3.6		
		2	1.75		2.15		2.9		3.8		
	3 V	0	1.8		2.1	2.6	2.8		3.6	6.0	
		1	1.9		2.3		2.9		3.8		
		2	2.0		2.4		3.0		4.0		
		3	2.0		2.5	3.0	3.1		4.0	6.5	
$I_{LPM3,VLO}$ Low-power mode 3, VLO mode ⁽⁷⁾⁽⁴⁾	3 V	0	1.1		1.3	1.8	1.9		2.7	5.0	μA
		1	1.1		1.4		2.0		2.8		
		2	1.2		1.5		2.1		2.9		
		3	1.3		1.5	2.0	2.2		3.0	5.5	
I_{LPM4} Low-power mode 4 ⁽⁸⁾⁽⁴⁾	3 V	0	0.9		1.1	1.5	1.8		2.5	4.8	μA
		1	1.1		1.2		2.0		2.6		
		2	1.2		1.2		2.1		2.7		
		3	1.3		1.3	1.6	2.2		2.8	5.0	
$I_{LPM4.5}$ Low-power mode 4.5 ⁽⁹⁾	3 V		0.15		0.18	0.35	0.26		0.45	0.80	μA

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz USB disabled (VUSBEN = 0, SLDOEN = 0).

(4) Current for brownout, high side supervisor (SVSH) normal mode included. Low side supervisor and monitors disabled (SVSL, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.

(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled. USB disabled (VUSBEN = 0, SLDOEN = 0)

(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz USB disabled (VUSBEN = 0, SLDOEN = 0)

(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz USB disabled (VUSBEN = 0, SLDOEN = 0)

(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz USB disabled (VUSBEN = 0, SLDOEN = 0)

(9) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

Schmitt-Trigger Inputs – General Purpose I/O⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+} Positive-going input threshold voltage		1.8 V	0.80		1.40	V
		3 V	1.50		2.10	
V _{IT–} Negative-going input threshold voltage		1.8 V	0.45		1.00	V
		3 V	0.75		1.65	
V _{hys} Input voltage hysteresis (V _{IT+} – V _{IT–})		1.8 V	0.3		0.85	V
		3 V	0.4		1.0	
R _{Pull} Pullup/pulldown resistor	For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC}		20	35	50	kΩ
C _I Input capacitance	V _{IN} = V _{SS} or V _{CC}			5		pF

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

Inputs – Ports P1 and P2⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
t _(int) External interrupt timing ⁽²⁾	Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag	2.2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

Leakage Current – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
I _{lkg} (P _{x.x}) High-impedance leakage current	(1) (2)	1.8 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Outputs – General Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH} High-level output voltage	I _(OHmax) = –3 mA ⁽¹⁾	1.8 V	V _{CC} – 0.25	V _{CC}	V
	I _(OHmax) = –10 mA ⁽²⁾		V _{CC} – 0.60	V _{CC}	
	I _(OHmax) = –5 mA ⁽¹⁾	3 V	V _{CC} – 0.25	V _{CC}	
	I _(OHmax) = –15 mA ⁽²⁾		V _{CC} – 0.60	V _{CC}	
V _{OL} Low-level output voltage	I _(OLmax) = 3 mA ⁽¹⁾	1.8 V	V _{SS}	V _{SS} + 0.25	V
	I _(OLmax) = 10 mA ⁽²⁾		V _{SS}	V _{SS} + 0.60	
	I _(OLmax) = 5 mA ⁽¹⁾	3 V	V _{SS}	V _{SS} + 0.25	
	I _(OLmax) = 15 mA ⁽²⁾		V _{SS}	V _{SS} + 0.60	

(1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Outputs – General Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH} High-level output voltage	I _(OHmax) = –1 mA ⁽²⁾	1.8 V	V _{CC} – 0.25	V _{CC}	V
	I _(OHmax) = –3 mA ⁽³⁾		V _{CC} – 0.60	V _{CC}	
	I _(OHmax) = –2 mA ⁽²⁾	3 V	V _{CC} – 0.25	V _{CC}	
	I _(OHmax) = –6 mA ⁽³⁾		V _{CC} – 0.60	V _{CC}	
V _{OL} Low-level output voltage	I _(OLmax) = 1 mA ⁽²⁾	1.8 V	V _{SS}	V _{SS} + 0.25	V
	I _(OLmax) = 3 mA ⁽³⁾		V _{SS}	V _{SS} + 0.60	
	I _(OLmax) = 2 mA ⁽²⁾	3 V	V _{SS}	V _{SS} + 0.25	
	I _(OLmax) = 6 mA ⁽³⁾		V _{SS}	V _{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

(3) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Output Frequency – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f _{Px,y} Port output frequency (with load)	⁽¹⁾⁽²⁾ V _{CC} = 1.8 V PMMCOREVx = 0		16	MHz
	V _{CC} = 3 V PMMCOREVx = 3		25	
f _{Port_CLK} Clock output frequency	ACLK SMCLK MCLK C _L = 20 pF ⁽²⁾	V _{CC} = 1.8 V PMMCOREVx = 0	16	MHz
		V _{CC} = 3 V PMMCOREVx = 3	25	

(1) A resistive divider with 2 × R₁ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R₁ = 550 Ω. For reduced drive strength, R₁ = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.

(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

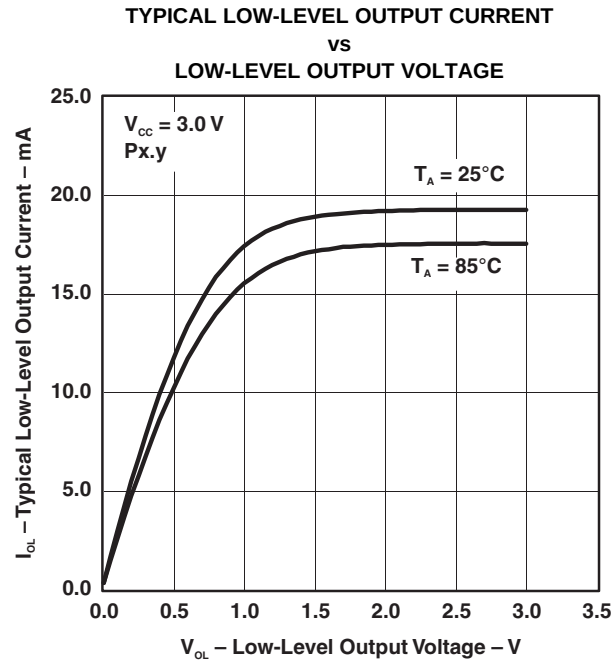


Figure 2.

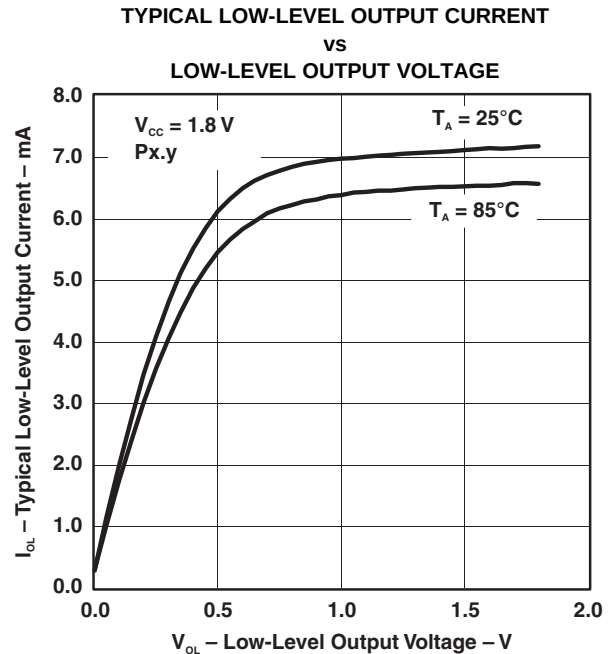


Figure 3.

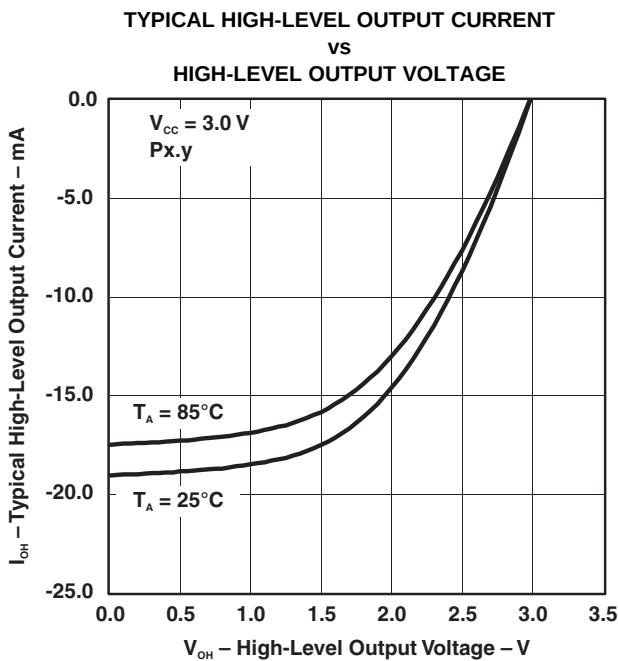


Figure 4.

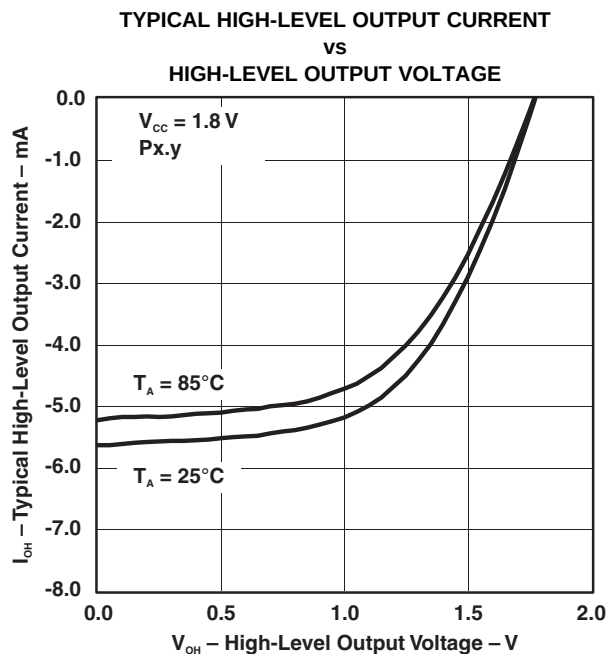


Figure 5.

Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

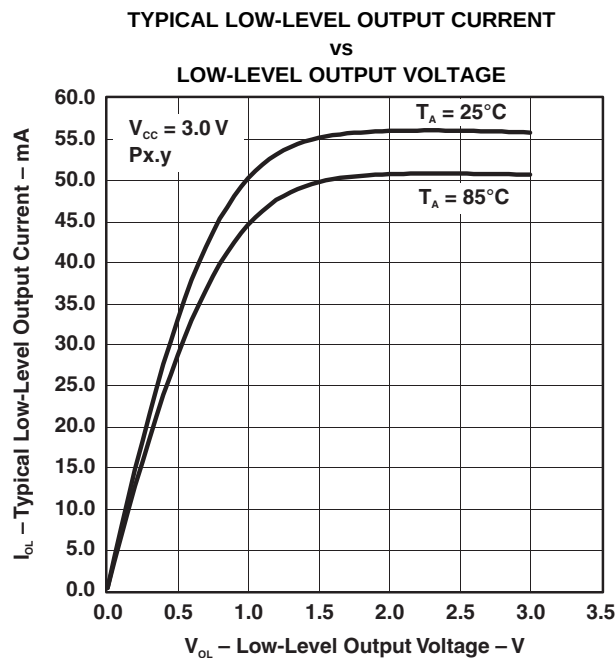


Figure 6.

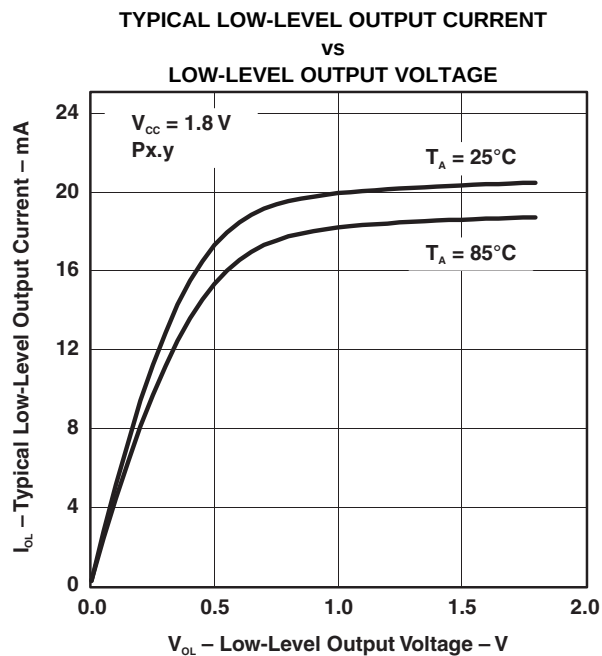


Figure 7.

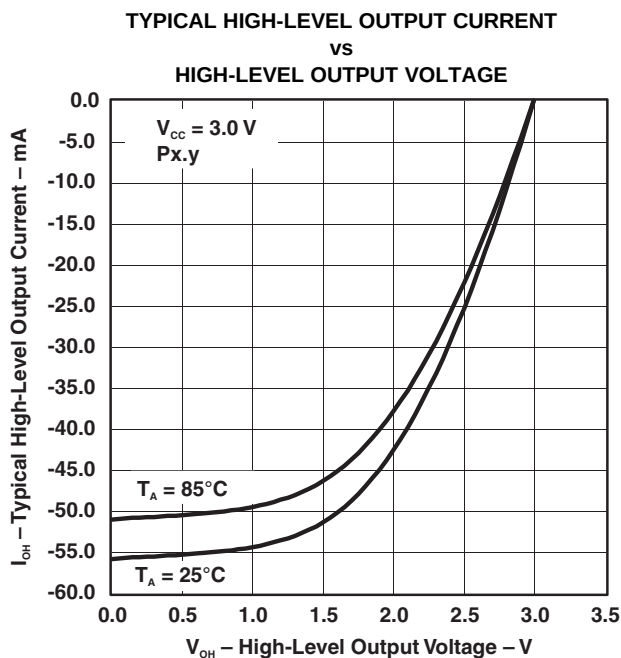


Figure 8.

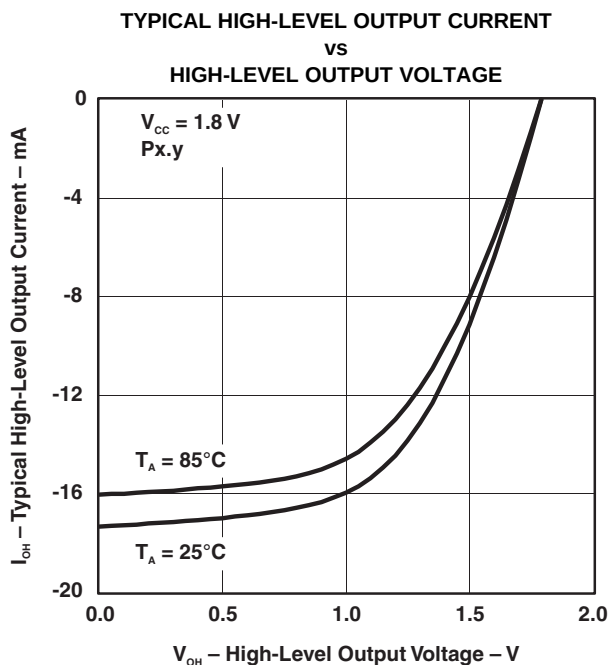


Figure 9.

Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
ΔI _{DVCC,LF}	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C	3 V	0.075			μA
		f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C		0.170			
		f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C		0.290			
f _{XT1,LF0}	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0		32768			Hz
f _{XT1,LF,SW}	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1 ⁽²⁾ ⁽³⁾		10	32.768	50	kHz
OA _{LF}	Oscillation allowance for LF crystals ⁽⁴⁾	XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, f _{XT1,LF} = 32768 Hz, C _{L,eff} = 6 pF		210			kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, f _{XT1,LF} = 32768 Hz, C _{L,eff} = 12 pF		300			
C _{L,eff}	Integrated effective load capacitance, LF mode ⁽⁵⁾	XTS = 0, XCAP _x = 0 ⁽⁶⁾		2			pF
		XTS = 0, XCAP _x = 1		5.5			
		XTS = 0, XCAP _x = 2		8.5			
		XTS = 0, XCAP _x = 3		12.0			
Duty cycle, LF mode		XTS = 0, Measured at ACLK, f _{XT1,LF} = 32768 Hz		30		70	%
f _{Fault,LF}	Oscillator fault frequency, LF mode ⁽⁷⁾	XTS = 0 ⁽⁸⁾		10		10000	Hz
t _{START,LF}	Startup time, LF mode	f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 6 pF	3 V	1000			ms
		f _{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF		500			

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - (a) For XT1DRIVE_x = 0, C_{L,eff} ≤ 6 pF.
 - (b) For XT1DRIVE_x = 1, 6 pF ≤ C_{L,eff} ≤ 9 pF.
 - (c) For XT1DRIVE_x = 2, 6 pF ≤ C_{L,eff} ≤ 10 pF.
 - (d) For XT1DRIVE_x = 3, C_{L,eff} ≥ 6 pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{DVCC,XT2} XT2 oscillator crystal current consumption	f _{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C	3 V		200		μA
	f _{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 1, T _A = 25°C			260		
	f _{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C			325		
	f _{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 3, T _A = 25°C			450		
f _{XT2,HF0} XT2 oscillator crystal frequency, mode 0	XT2DRIVE _x = 0, XT2BYPASS = 0 ⁽³⁾		4		8	MHz
f _{XT2,HF1} XT2 oscillator crystal frequency, mode 1	XT2DRIVE _x = 1, XT2BYPASS = 0 ⁽³⁾		8		16	MHz
f _{XT2,HF2} XT2 oscillator crystal frequency, mode 2	XT2DRIVE _x = 2, XT2BYPASS = 0 ⁽³⁾		16		24	MHz
f _{XT2,HF3} XT2 oscillator crystal frequency, mode 3	XT2DRIVE _x = 3, XT2BYPASS = 0 ⁽³⁾		24		32	MHz
f _{XT2,HF,SW} XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1 ^{(4) (3)}		0.7		32	MHz
O _{AHF} Oscillation allowance for HF crystals ⁽⁵⁾	XT2DRIVE _x = 0, XT2BYPASS = 0, f _{XT2,HF0} = 6 MHz, C _{L,eff} = 15 pF			450		Ω
	XT2DRIVE _x = 1, XT2BYPASS = 0, f _{XT2,HF1} = 12 MHz, C _{L,eff} = 15 pF			320		
	XT2DRIVE _x = 2, XT2BYPASS = 0, f _{XT2,HF2} = 20 MHz, C _{L,eff} = 15 pF			200		
	XT2DRIVE _x = 3, XT2BYPASS = 0, f _{XT2,HF3} = 32 MHz, C _{L,eff} = 15 pF			200		
t _{START,HF} Startup time	f _{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 15 pF	3 V		0.5		ms
	f _{OSC} = 20 MHz, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C, C _{L,eff} = 15 pF			0.3		
C _{L,eff} Integrated effective load capacitance, HF mode ^{(6) (1)}				1		pF
Duty cycle	Measured at ACLK, f _{XT2,HF2} = 20 MHz		40	50	60	%
f _{Fault,HF} Oscillator fault frequency ⁽⁷⁾	XT2BYPASS = 1 ⁽⁸⁾		30		300	kHz

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

(a) Keep the traces between the device and the crystal as short as possible.

(b) Design a good ground plane around the oscillator pins.

(c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.

(d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.

(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.

(f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{VLO} VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df _{VLO} /dT VLO frequency temperature drift	Measured at ACLK ⁽¹⁾	1.8 V to 3.6 V		0.5		%/°C
df _{VLO} /dV _{CC} VLO frequency supply voltage drift	Measured at ACLK ⁽²⁾	1.8 V to 3.6 V		4		%/V
Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{REFO} REFO oscillator current consumption	T _A = 25°C	1.8 V to 3.6 V		3		μA
REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
f _{REFO} REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5	%
	T _A = 25°C	3 V			±1.5	%
df _{REFO} /dT REFO frequency temperature drift	Measured at ACLK ⁽¹⁾	1.8 V to 3.6 V		0.01		%/°C
df _{REFO} /dV _{CC} REFO frequency supply voltage drift	Measured at ACLK ⁽²⁾	1.8 V to 3.6 V		1.0		%/V
Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
t _{START} REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		25		μs

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
f _{DCO(0,0)}	DCO frequency (0, 0)	DCORSELx = 0, DCOx = 0, MODx = 0		0.07	0.20	MHz	
f _{DCO(0,31)}	DCO frequency (0, 31)	DCORSELx = 0, DCOx = 31, MODx = 0		0.70	1.70	MHz	
f _{DCO(1,0)}	DCO frequency (1, 0)	DCORSELx = 1, DCOx = 0, MODx = 0		0.15	0.36	MHz	
f _{DCO(1,31)}	DCO frequency (1, 31)	DCORSELx = 1, DCOx = 31, MODx = 0		1.47	3.45	MHz	
f _{DCO(2,0)}	DCO frequency (2, 0)	DCORSELx = 2, DCOx = 0, MODx = 0		0.32	0.75	MHz	
f _{DCO(2,31)}	DCO frequency (2, 31)	DCORSELx = 2, DCOx = 31, MODx = 0		3.17	7.38	MHz	
f _{DCO(3,0)}	DCO frequency (3, 0)	DCORSELx = 3, DCOx = 0, MODx = 0		0.64	1.51	MHz	
f _{DCO(3,31)}	DCO frequency (3, 31)	DCORSELx = 3, DCOx = 31, MODx = 0		6.07	14.0	MHz	
f _{DCO(4,0)}	DCO frequency (4, 0)	DCORSELx = 4, DCOx = 0, MODx = 0		1.3	3.2	MHz	
f _{DCO(4,31)}	DCO frequency (4, 31)	DCORSELx = 4, DCOx = 31, MODx = 0		12.3	28.2	MHz	
f _{DCO(5,0)}	DCO frequency (5, 0)	DCORSELx = 5, DCOx = 0, MODx = 0		2.5	6.0	MHz	
f _{DCO(5,31)}	DCO frequency (5, 31)	DCORSELx = 5, DCOx = 31, MODx = 0		23.7	54.1	MHz	
f _{DCO(6,0)}	DCO frequency (6, 0)	DCORSELx = 6, DCOx = 0, MODx = 0		4.6	10.7	MHz	
f _{DCO(6,31)}	DCO frequency (6, 31)	DCORSELx = 6, DCOx = 31, MODx = 0		39.0	88.0	MHz	
f _{DCO(7,0)}	DCO frequency (7, 0)	DCORSELx = 7, DCOx = 0, MODx = 0		8.5	19.6	MHz	
f _{DCO(7,31)}	DCO frequency (7, 31)	DCORSELx = 7, DCOx = 31, MODx = 0		60	135	MHz	
S _{DCORSEL}	Frequency step between range DCORSEL and DCORSEL + 1	S _{RSEL} = f _{DCO(DCORSEL+1,DCO)} /f _{DCO(DCORSEL,DCO)}		1.2	2.3	ratio	
S _{DCO}	Frequency step between tap DCO and DCO + 1	S _{DCO} = f _{DCO(DCORSEL,DCO+1)} /f _{DCO(DCORSEL,DCO)}		1.02	1.12	ratio	
	Duty cycle	Measured at SMCLK		40	50	60	%
df _{DCO} /dT	DCO frequency temperature drift ⁽¹⁾	f _{DCO} = 1 MHz,		0.1		%/°C	
df _{DCO} /dV _{CC}	DCO frequency voltage drift ⁽²⁾	f _{DCO} = 1 MHz		1.9		%/V	

(1) Calculated using the box method: $(\text{MAX}(-40 \text{ to } 85^\circ\text{C}) - \text{MIN}(-40 \text{ to } 85^\circ\text{C})) / \text{MIN}(-40 \text{ to } 85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$

(2) Calculated using the box method: $(\text{MAX}(1.8 \text{ to } 3.6 \text{ V}) - \text{MIN}(1.8 \text{ to } 3.6 \text{ V})) / \text{MIN}(1.8 \text{ to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$

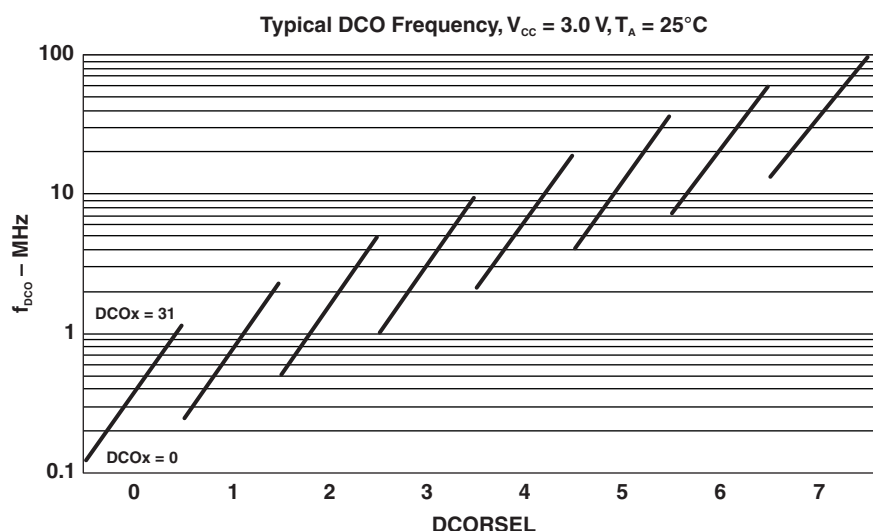


Figure 10. Typical DCO frequency

PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V(DV _{CC} _BOR_IT–)	BOR _H on voltage, DV _{CC} falling level	dDV _{CC} /dt < 3 V/s			1.45	V
V(DV _{CC} _BOR_IT+)	BOR _H off voltage, DV _{CC} rising level	dDV _{CC} /dt < 3 V/s	0.80	1.30	1.50	V
V(DV _{CC} _BOR_hys)	BOR _H hysteresis		60		250	mV
t _{RESET}	Pulse duration required at RST/NMI pin to accept a reset		2			μs

PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{CORE3} (AM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV _{CC} ≤ 3.6 V		1.90		V
V _{CORE2} (AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV _{CC} ≤ 3.6 V		1.80		V
V _{CORE1} (AM)	Core voltage, active mode, PMMCOREV = 1	2.0 V ≤ DV _{CC} ≤ 3.6 V		1.60		V
V _{CORE0} (AM)	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV _{CC} ≤ 3.6 V		1.40		V
V _{CORE3} (LPM)	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV _{CC} ≤ 3.6 V		1.94		V
V _{CORE2} (LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV _{CC} ≤ 3.6 V		1.84		V
V _{CORE1} (LPM)	Core voltage, low-current mode, PMMCOREV = 1	2.0 V ≤ DV _{CC} ≤ 3.6 V		1.64		V
V _{CORE0} (LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV _{CC} ≤ 3.6 V		1.44		V

PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$ SVS current consumption	SVSHE = 0, DV _{CC} = 3.6 V		0		nA
	SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 0		200		nA
	SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 1		1.5		μA
$V_{(SVSH_IT-)}$ SVS _H on voltage level ⁽¹⁾	SVSHE = 1, SVSHRVL = 0	1.57	1.68	1.78	V
	SVSHE = 1, SVSHRVL = 1	1.79	1.88	1.98	
	SVSHE = 1, SVSHRVL = 2	1.98	2.08	2.21	
	SVSHE = 1, SVSHRVL = 3	2.10	2.18	2.31	
$V_{(SVSH_IT+)}$ SVS _H off voltage level ⁽¹⁾	SVSHE = 1, SVSMHRRRL = 0	1.62	1.74	1.85	V
	SVSHE = 1, SVSMHRRRL = 1	1.88	1.94	2.07	
	SVSHE = 1, SVSMHRRRL = 2	2.07	2.14	2.28	
	SVSHE = 1, SVSMHRRRL = 3	2.20	2.30	2.42	
	SVSHE = 1, SVSMHRRRL = 4	2.32	2.40	2.55	
	SVSHE = 1, SVSMHRRRL = 5	2.52	2.70	2.88	
	SVSHE = 1, SVSMHRRRL = 6	2.90	3.10	3.23	
	SVSHE = 1, SVSMHRRRL = 7	2.90	3.10	3.23	
$t_{pd(SVSH)}$ SVS _H propagation delay	SVSHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVSHFP = 1		2.5		μs
	SVSHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVSHFP = 0		20		
$t_{(SVSH)}$ SVS _H on or off delay time	SVSHE = 0 → 1 SVSHFP = 1		12.5		μs
	SVSHE = 0 → 1 SVSHFP = 0		100		
dV _{DVCC} /dt DVCC rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and use.

PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$ SVM _H current consumption	SVMHE = 0, DV _{CC} = 3.6 V		0		nA
	SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0		200		nA
	SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1		1.5		μA
$V_{(SVMH)}$ SVM _H on or off voltage level ⁽¹⁾	SVMHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
	SVMHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
	SVMHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
	SVMHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
	SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
	SVMHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
	SVMHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
	SVMHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
$t_{pd(SVMH)}$ SVM _H propagation delay	SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1		2.5		μs
	SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0		20		
$t_{(SVMH)}$ SVM _H on or off delay time	SVMHE = 0 → 1, SVMHFP = 1		12.5		μs
	SVMHE = 0 → 1, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the V_{CORE} (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and use.

PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$ SVS _L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
	SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		nA
	SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		2.0		μA
$t_{pd(SVSL)}$ SVS _L propagation delay	SVSLE = 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1		2.5		μs
	SVSLE = 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0		20		
$t_{(SVSL)}$ SVS _L on or off delay time	SVSLE = 0 → 1, SVSLFP = 1		12.5		μs
	SVSLE = 0 → 1, SVSLFP = 0		100		

PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVM_L)}$ SVM _L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
	SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		nA
	SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		1.5		μA
$t_{pd(SVM_L)}$ SVM _L propagation delay	SVMLE = 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVMLFP = 1		2.5		μs
	SVMLE = 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVMLFP = 0		20		
$t_{(SVM_L)}$ SVM _L on or off delay time	SVMLE = 0 → 1, SVMLFP = 1		12.5		μs
	SVMLE = 0 → 1, SVMLFP = 0		100		

Wake-Up From Low Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$ Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1, $f_{MCLK} \geq 4.0 \text{ MHz}$			5	μs
	$f_{MCLK} < 4.0 \text{ MHz}$			6	
$t_{WAKE-UP-SLOW}$ Wake-up time from LPM2, LPM3 or LPM4 to active mode ⁽²⁾	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0		150	165	μs
$t_{WAKE-UP-LPM5}$ Wake-up time from LPM4.5 to active mode ⁽³⁾			2	3	ms
$t_{WAKE-UP-RESET}$ Wake-up time from $\overline{RST}$ or BOR event to active mode ⁽³⁾			2	3	ms

- (1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). Fastest wakeup times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430F6xx Family User's Guide (SLAU208)*.
- (2) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430F6xx Family User's Guide (SLAU208)*.
- (3) This value represents the time from the wakeup event to the reset vector execution.

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f_{TA} Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10%	1.8 V, 3 V			25	MHz
$t_{TA,cap}$ Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture.	1.8 V, 3 V	20			ns

Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f_{TB} Timer_B input clock frequency	Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ± 10%	1.8 V, 3 V			25	MHz
$t_{TB,cap}$ Timer_B capture timing	All capture inputs, Minimum pulse duration required for capture	1.8 V, 3 V	20			ns

USCI (UART Mode) Recommended Operating Conditions

PARAMETER	CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI} USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f _{SYSTEM}	MHz
f _{BITCLK} BITCLK clock frequency (equals baud rate in MBaud)					1	MHz

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _r UART receive deglitch time ⁽¹⁾		2.2 V	50		600	ns
		3 V	50		600	

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode) Recommended Operating Conditions

PARAMETER	CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI} USCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ± 10%				f _{SYSTEM}	MHz

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see Note ⁽¹⁾, [Figure 11](#) and [Figure 12](#))

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI} USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%				f _{SYSTEM}	MHz
t _{SU,MI} SOMI input data setup time	PMMCOREV = 0	1.8 V	55			ns
		3 V	38			
	PMMCOREV = 3	2.4 V	30			ns
		3 V	25			
t _{HD,MI} SOMI input data hold time	PMMCOREV = 0	1.8 V	0			ns
		3 V	0			
	PMMCOREV = 3	2.4 V	0			ns
		3 V	0			
t _{VALID,MO} SIMO output data valid time ⁽²⁾	UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 0	1.8 V			20	ns
		3 V			18	
	UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 3	2.4 V			16	ns
		3 V			15	
t _{HD,MO} SIMO output data hold time ⁽³⁾	C _L = 20 pF, PMMCOREV = 0	1.8 V	-10			ns
		3 V	-8			
	C _L = 20 pF, PMMCOREV = 3	2.4 V	-10			ns
		3 V	-8			

- (1) $f_{UCXCLK} = 1/2(t_{LO/Hi} \text{ with } t_{LO/Hi} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave)))$.
For the slave's parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$ see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 11](#) and [Figure 12](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 11](#) and [Figure 12](#).

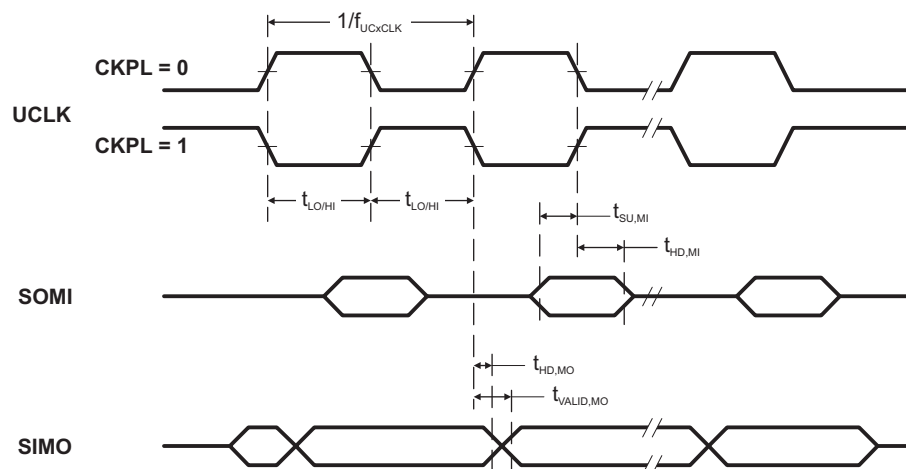


Figure 11. SPI Master Mode, CKPH = 0

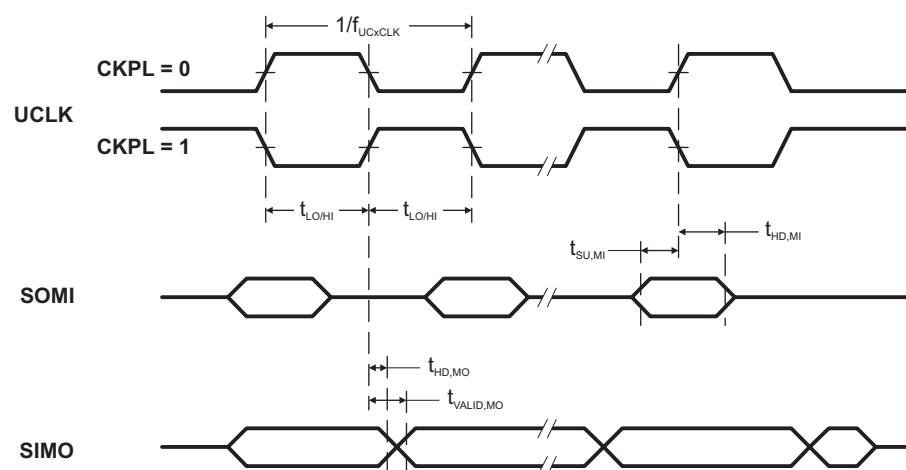


Figure 12. SPI Master Mode, CKPH = 1

USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see Note ⁽¹⁾, [Figure 13](#) and [Figure 14](#))

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$ STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11			ns
		3 V	8			
	PMMCOREV = 3	2.4 V	7			ns
		3 V	6			
$t_{STE,LAG}$ STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	3			ns
		3 V	3			
	PMMCOREV = 3	2.4 V	3			ns
		3 V	3			
$t_{STE,ACC}$ STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V			66	ns
		3 V			50	
	PMMCOREV = 3	2.4 V			36	ns
		3 V			30	
$t_{STE,DIS}$ STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V			30	ns
		3 V			23	
	PMMCOREV = 3	2.4 V			16	ns
		3 V			13	
$t_{SU,SI}$ SIMO input data setup time	PMMCOREV = 0	1.8 V	5			ns
		3 V	5			
	PMMCOREV = 3	2.4 V	2			ns
		3 V	2			
$t_{HD,SI}$ SIMO input data hold time	PMMCOREV = 0	1.8 V	5			ns
		3 V	5			
	PMMCOREV = 3	2.4 V	5			ns
		3 V	5			
$t_{VALID,SO}$ SOMI output data valid time ⁽²⁾	UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 0	1.8 V			76	ns
		3 V			60	
	UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 3	2.4 V			44	ns
		3 V			40	
$t_{HD,SO}$ SOMI output data hold time ⁽³⁾	C _L = 20 pF, PMMCOREV = 0	1.8 V	18			ns
		3 V	12			
	C _L = 20 pF, PMMCOREV = 3	2.4 V	10			ns
		3 V	8			

(1) $f_{UCXCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.

For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 11](#) and [Figure 12](#).

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 11](#) and [Figure 12](#).

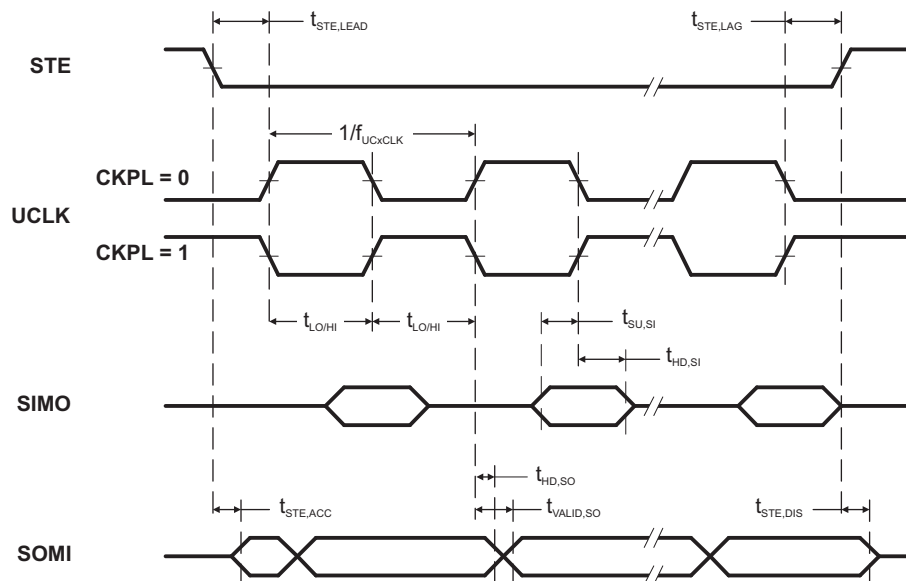


Figure 13. SPI Slave Mode, CKPH = 0

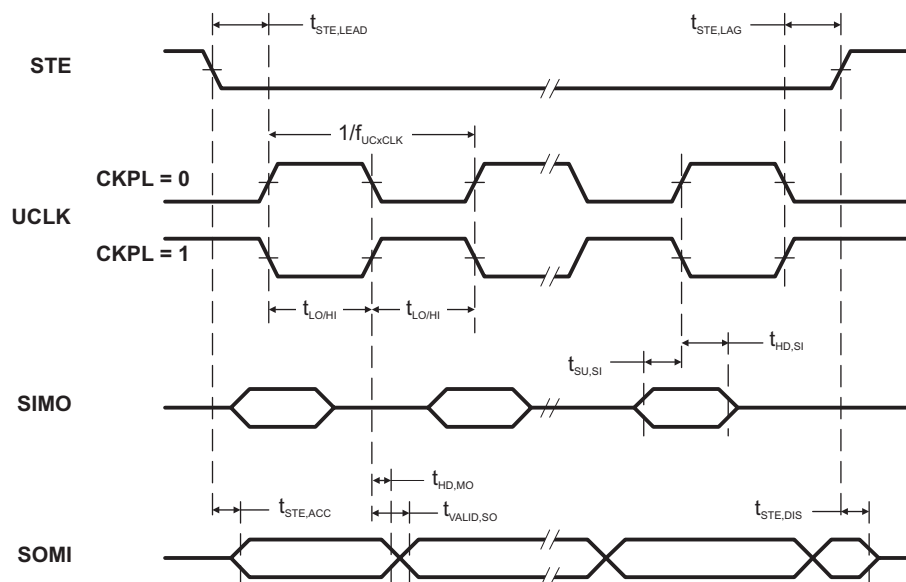


Figure 14. SPI Slave Mode, CKPH = 1

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 15](#))

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%			f _{SYSTEM}	MHz
f _{SCL}	SCL clock frequency	2.2 V, 3 V	0		400	kHz
t _{HD,STA}	Hold time (repeated) START	f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz	4.0 0.6			μs
t _{SU,STA}	Setup time for a repeated START	f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz	4.7 0.6			μs
t _{HD,DAT}	Data hold time	2.2 V, 3 V	0			ns
t _{SU,DAT}	Data setup time	2.2 V, 3 V	250			ns
t _{SU,STO}	Setup time for STOP	f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz	4.0 0.6			μs
t _{SP}	Pulse duration of spikes suppressed by input filter	2.2 V 3 V	50 50		600 600	ns

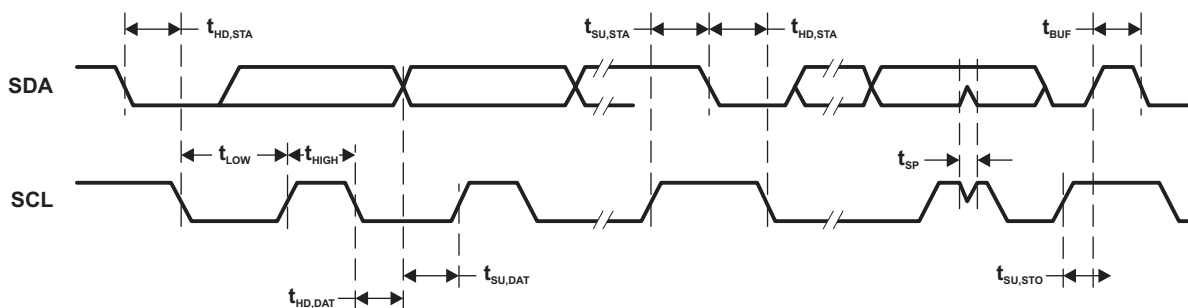


Figure 15. I2C Mode Timing

10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
AV _{CC}	Analog supply voltage	AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V		1.8		3.6	V
V _(Ax)	Analog input voltage range ⁽²⁾	All ADC10_A pins: P1.0 to P1.5 and P3.6 and P3.7 terminals		0		AV _{CC}	V
I _{ADC10_A}	Operating supply current into AVCC terminal, REF module and reference buffer off	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00	2.2 V		60	100	μA
			3 V		75	110	
	Operating supply current into AVCC terminal, REF module on, reference buffer on	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01	3 V		113	150	μA
	Operating supply current into AVCC terminal, REF module off, reference buffer on	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VEREF = 2.5 V	3 V		105	140	μA
	Operating supply current into AVCC terminal, REF module off, reference buffer off	f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VEREF = 2.5 V	3 V		70	110	μA
C _I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad.	2.2 V		3.5		pF
R _I	Input MUX ON resistance	AV _{CC} > 2.0V, 0 V ≤ V _{Ax} ≤ AV _{CC}				36	kΩ
		1.8V < AV _{CC} < 2.0V, 0 V ≤ V _{Ax} ≤ AV _{CC}				96	

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. Two decoupling capacitors, 10 μF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{ADC10CLK}		For specified performance of ADC10_A linearity parameters	2.2 V, 3 V	0.45	5	5.5	MHz
f _{ADC10OSC}	Internal ADC10_A oscillator ⁽¹⁾	ADC10DIV = 0, f _{ADC10CLK} = f _{ADC10OSC}	2.2 V, 3 V	4.2	4.8	5.4	MHz
t _{CONVERT}	Conversion time	REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode f _{ADC10OSC} = 4 MHz to 5 MHz	2.2 V, 3 V	2.4		3.0	μs
		External f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0			(2)		
t _{ADC10ON}	Turn on settling time of the ADC	See ⁽³⁾				100	ns
t _{Sample}	Sampling time	R _S = 1000 Ω, R _I = 96 kΩ, C _I = 3.5 pF ⁽⁴⁾	1.8 V	3			μs
		R _S = 1000 Ω, R _I = 36 kΩ, C _I = 3.5 pF ⁽⁴⁾	3 V	1			μs

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.

(2) $12 \times \text{ADC10DIV} \times 1/f_{\text{ADC10CLK}}$

(3) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

(4) Approximately eight Tau (τ) are needed to get an error of less than ±0.5 LSB

10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
E _I	Integral linearity error	$1.4\text{ V} \leq (V_{\text{eREF+}} - V_{\text{eREF-}})_{\text{min}} \leq 1.6\text{ V}$	2.2 V, 3 V			±1.0	LSB
		$1.6\text{ V} < (V_{\text{eREF+}} - V_{\text{eREF-}})_{\text{min}} \leq V_{\text{AVCC}}$				±1.0	
E _D	Differential linearity error	$(V_{\text{eREF+}} - V_{\text{eREF-}})_{\text{min}} \leq (V_{\text{eREF+}} - V_{\text{eREF-}})$, C _{VREF+} = 20 pF	2.2 V, 3 V			±1.0	LSB
E _O	Offset error	$(V_{\text{eREF+}} - V_{\text{eREF-}})_{\text{min}} \leq (V_{\text{eREF+}} - V_{\text{eREF-}})$, Internal impedance of source R _S < 100 Ω, C _{VREF+} = 20 pF	2.2 V, 3 V			±1.0	LSB
E _G	Gain error	$(V_{\text{eREF+}} - V_{\text{eREF-}})_{\text{min}} \leq (V_{\text{eREF+}} - V_{\text{eREF-}})$, C _{VREF+} = 20 pF	2.2 V, 3 V			±1.0	LSB
E _T	Total unadjusted error	$(V_{\text{eREF+}} - V_{\text{eREF-}})_{\text{min}} \leq (V_{\text{eREF+}} - V_{\text{eREF-}})$, C _{VREF+} = 20 pF	2.2 V, 3 V		±1.0	±2.0	LSB

REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{eREF+}	Positive external reference voltage input	V _{eREF+} > V _{eREF-} ⁽²⁾		1.4		V _{AVCC}	V
V _{eREF-}	Negative external reference voltage input	V _{eREF+} > V _{eREF-} ⁽³⁾		0		1.2	V
(V _{eREF+} - V _{eREF-})	Differential external reference voltage input	V _{eREF+} > V _{eREF-} ⁽⁴⁾		1.4		V _{AVCC}	V
I _{VeREF+} I _{VeREF-}	Static input current	$1.4\text{ V} \leq V_{\text{eREF+}} \leq V_{\text{AVCC}}$, V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x0001, Conversion rate 200 kpsps	2.2 V, 3 V		±8.5	±26	μA
		$1.4\text{ V} \leq V_{\text{eREF+}} \leq V_{\text{AVCC}}$, V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x1000, Conversion rate 20 kpsps	2.2 V, 3 V			±1	μA
C _{VeREF+/-}	Capacitance at VeREF+ or VeREF- terminal	⁽⁵⁾		10			μF

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.

REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{REF+}	REFVSEL = {2} for 2.5 V, REFON = 1	3 V	2.51	±1.5%		V
	REFVSEL = {1} for 2.0 V, REFON = 1	3 V	1.99	±1.5%		
	REFVSEL = {0} for 1.5 V, REFON = 1	2.2 V, 3 V	1.5	±1.5%		
AV _{CC(min)}	REFVSEL = {0} for 1.5 V		2.2			V
	REFVSEL = {1} for 2.0 V		2.2			
	REFVSEL = {2} for 2.5 V		2.7			
I _{REF+}	f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V	3 V	18	24		μA
	f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V	3 V	15.5	21		μA
	f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V	3 V	13.5	21		μA
TC _{REF+}	Temperature coefficient of built-in reference ⁽³⁾ I _{VREF+} = 0 A, REFVSEL = {0, 1, 2}, REFON = 1		30	50		ppm/°C
I _{SENSOR}	Operating supply current into AVCC terminal ⁽⁴⁾ REFON = 0, INCH = 0Ah, ADC10ON = N/A, T _A = 30°C	2.2 V	20	22		μA
		3 V	20	22		
V _{SENSOR}	See ⁽⁵⁾ ADC10ON = 1, INCH = 0Ah, T _A = 30°C	2.2 V	770			mV
		3 V	770			
V _{MID}	AVCC divider at channel 11 ADC10ON = 1, INCH = 0Bh, V _{MID} is approximately 0.5 × V _{AVCC}	2.2 V	1.06	1.1	1.14	V
		3 V	1.46	1.5	1.54	
t _{SENSOR(sample)}	Sample time required if channel 10 is selected ⁽⁶⁾ ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB		30			μs
t _{V_{MID}(sample)}	Sample time required if channel 11 is selected ⁽⁷⁾ ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB		1			μs
PSRR _{DC}	Power supply rejection ratio (dc) AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1		120			μV/V
PSRR _{AC}	Power supply rejection ratio (ac) AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1		6.4			mV/V
t _{SETTLE}	Settling time of reference voltage ⁽⁸⁾ AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFON = 0 → 1		75			μs

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

(2) The internal reference current is supplied via terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

(3) Calculated using the box method: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C - (-40°C)).

(4) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.

(5) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.

(6) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.

(7) The on-time t_{V_{MID}(on)} is included in the sampling time t_{V_{MID}(sample)}; no additional on time is needed.

(8) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

Comparator B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage			1.8		3.6	V
I _{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CBPWRMD = 00, CBON = 1, CBRs _x = 00	1.8 V			40	μA
			2.2 V		30	50	
			3 V		40	65	
		CBPWRMD = 01, CBON = 1, CBRs _x = 00	2.2 V, 3 V		10	17	
		CBPWRMD = 10, CBON = 1, CBRs _x = 00	2.2 V, 3 V		0.1	0.5	
I _{AVCC_REF}	Quiescent current of resistor ladder into AVCC, Includes REF module current	CBREFACC = 0, CBREFL _x = 01, CBRs _x = 10, REFON = 0, CBON = 0	2.2 V, 3 V		10	17	μA
		CBREFACC = 1, CBREFL _x = 01, CBRs _x = 10, REFON = 0, CBON = 0	2.2 V, 3 V			22	μA
V _{IC}	Common mode input range			0		V _{CC} - 1	V
V _{OFFSET}	Input offset voltage	CBPWRMD = 00				±20	mV
		CBPWRMD = 01, 10				±10	mV
C _{IN}	Input capacitance				5		pF
R _{SIN}	Series input resistance	ON - switch closed			3	4	kΩ
		OFF - switch opened		50			MΩ
t _{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	ns
		CBPWRMD = 10, CBF = 0				50	μs
t _{PD,filter}	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 00		0.35	0.6	1.0	μs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 01		0.6	1.0	1.8	μs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 10		1.0	1.8	3.4	μs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 11		1.8	3.4	6.5	μs
t _{EN_CMP}	Comparator enable time	CBON = 0 to CBON = 1 CBPWRMD = 00, 01			1	2	μs
		CBON = 0 to CBON = 1 CBPWRMD = 10				1.5	μs
t _{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			1	1.5	μs
V _{CB_REF}	Reference voltage for a given tap	V _{IN} = reference into resistor ladder, n = 0 to 31		V _{IN} × (n+0.5) /32	V _{IN} × (n+1) /32	V _{IN} × (n+1.5) /32	V

Ports PU.0 and PU.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	V _{USB} = 3.3 V ± 10%, I _{OH} = -25 mA. See Figure 17 for typical characteristics		2.4			V
V _{OL}	Low-level output voltage	V _{USB} = 3.3 V ± 10%, I _{OL} = 25 mA. See Figure 16 for typical characteristics				0.4	V
V _{IH}	High-level input voltage	V _{USB} = 3.3 V ± 10% See Figure 18 for typical characteristics		2.0			V
V _{IL}	Low-level input voltage	V _{USB} = 3.3 V ± 10% See Figure 18 for typical characteristics				0.8	V

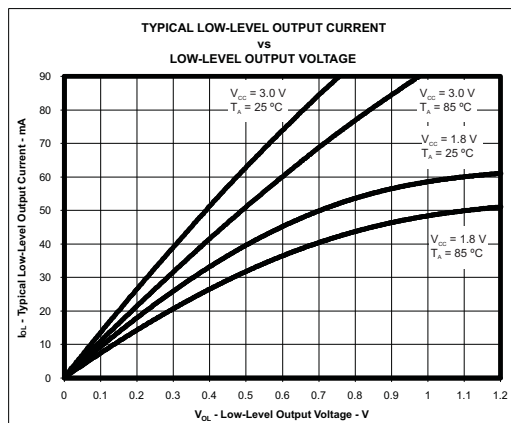


Figure 16. Ports PU.0, PU.1 Typical Low-Level Output Characteristics

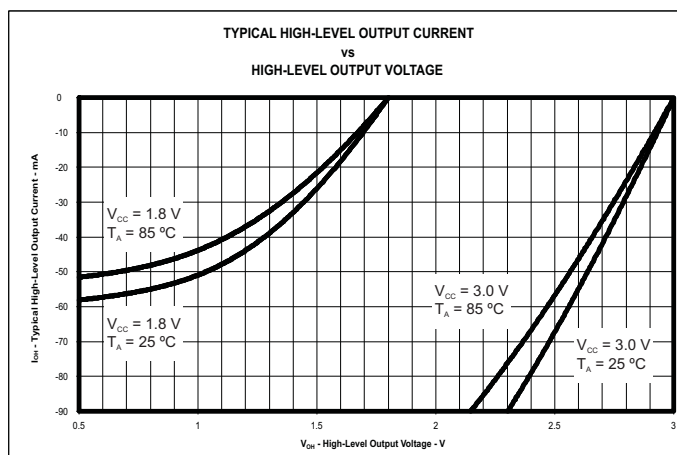


Figure 17. Ports PU.0, PU.1 Typical High-Level Output Characteristics

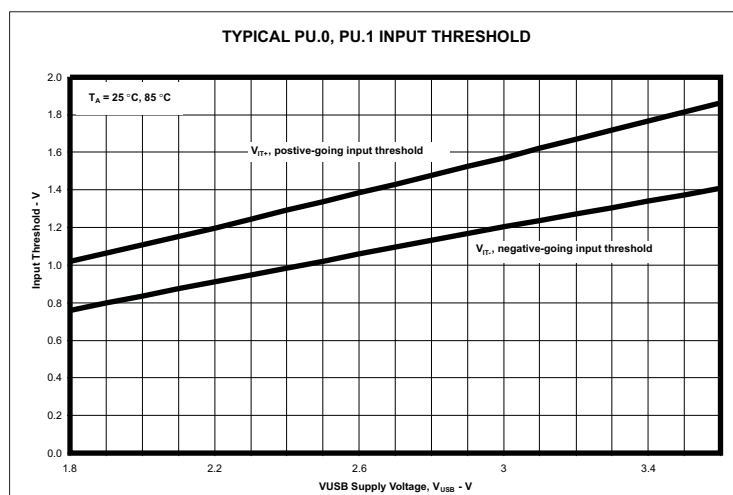


Figure 18. Ports PU.0, PU.1 Typical Input Threshold Characteristics

USB-Output Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	D+, D- single ended	USB 2.0 load conditions	2.8		3.6	V
V _{OL}	D+, D- single ended	USB 2.0 load conditions	0		0.3	V
Z(DRV)	D+, D- impedance	Including external series resistor of 27 Ω	28		44	Ω
t _{RISE}	Rise time	Full speed, differential, C _L = 50 pF, 10%/90%, Rpu on D+	4		20	ns
t _{FALL}	Fall time	Full speed, differential, C _L = 50 pF, 10%/90%, Rpu on D+	4		20	ns

USB-Input Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CM}	Differential input common mode range		0.8		2.5	V
Z _{IN}	Input impedance		300			k Ω
V _{CRS}	Crossover voltage		1.3		2.0	V
V _{IL}	Static SE input logic low level		0.8			V
V _{IH}	Static SE input logic high level				2.0	V
V _{DI}	Differential input voltage				0.2	V

USB-PWR (USB Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{LAUNCH}	V _{BUS} detection threshold				3.75	V
V _{BUS}	USB bus voltage	Normal operation	3.76		5.5	V
V _{USB}	USB LDO output voltage			3.3	±9%	V
V ₁₈	Internal USB voltage ⁽¹⁾			1.8		V
I _{USB_EXT}	Maximum external current from VUSB terminal ⁽²⁾	USB LDO is on			12	mA
I _{DET}	USB LDO current overload detection ⁽³⁾		60		100	mA
I _{SUSPEND}	Operating supply current into VBUS terminal ⁽⁴⁾	USB LDO on, USB PLL disabled			250	μ A
I _{USB_LDO}	Operating supply current into VBUS terminal, Represents the current of the 3.3-V LDO only	USB LDO on, USB 1.8-V LDO disabled, V _{BUS} = 5 V, USBDETEN = 0 or 1	1.8 V, 3 V	60		μ A
I _{VBUS_DETECT}	Operating supply current into VBUS terminal, Represents the current of the VBUS detection logic	USB LDO disabled, USB 1.8-V LDO disabled, V _{BUS} > V _{LAUNCH} , USBDETEN = 1	1.8 V, 3 V	30		μ A
C _{BUS}	VBUS terminal recommended capacitance			4.7		μ F
C _{USB}	VUSB terminal recommended capacitance			220		nF
C ₁₈	V18 terminal recommended capacitance			220		nF
t _{ENABLE}	Settling time V _{USB} and V ₁₈	Within 2%, recommended capacitances			2	ms
RPUR	Pullup resistance of PUR terminal ⁽⁵⁾		70	110	150	Ω

(1) This voltage is for internal usages only. No external DC loading should be applied.

(2) This represents additional current that can be supplied to the application from the VUSB terminal beyond the needs of the USB operation.

(3) A current overload is detected when the total current supplied from the USB LDO, including I_{USB_EXT}, exceeds this value.

(4) Does not include current contribution of Rpu and Rpd as outlined in the USB specification.

(5) This value, in series with an external resistor between PUR and D+, produces the Rpu as outlined in the USB specification.

USB-PLL (USB Phase Locked Loop)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{PLL}	Operating supply current				7	mA
f _{PLL}	PLL frequency			48		MHz
f _{UPD}	PLL reference frequency		1.5		3	MHz
t _{LOCK}	PLL lock time				2	ms
t _{Jitter}	PLL jitter			1000		ps

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DV _{CC(PGM/ERASE)}	Program and erase supply voltage	1.8		3.6	V
t _{READMARGIN}	Read access time during margin mode			200	ns
I _{PGM}	Supply current from DV _{CC} during program		3	5	mA
I _{ERASE}	Supply current from DV _{CC} during erase		2	6.5	mA
I _{MERASE} , I _{BANK}	Supply current from DV _{CC} during mass erase or bank erase			2.5	mA
t _{CPT}	Cumulative program time	See ⁽¹⁾		16	ms
	Program and erase endurance		10 ⁴	10 ⁵	cycles
t _{Retention}	Data retention duration	T _J = 25°C	100		years
t _{Word}	Word or byte program time	See ⁽²⁾	64	85	μs
t _{Block, 0}	Block program time for first byte or word	See ⁽²⁾	49	65	μs
t _{Block, 1–(N–1)}	Block program time for each additional byte or word, except for last byte or word	See ⁽²⁾	37	49	μs
t _{Block, N}	Block program time for last byte or word	See ⁽²⁾	55	73	μs
t _{Erase}	Erase time for segment, mass erase, and bank erase when available.	See ⁽²⁾	23	32	ms

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.

(2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	V _{CC}	MIN	TYP	MAX	UNIT
f _{SBW}	2.2 V, 3 V	0		20	MHz
t _{SBW,Low}	2.2 V, 3 V	0.025		15	μs
t _{SBW,En}	2.2 V, 3 V			1	μs
t _{SBW,Rst}		15		100	μs
f _{TCK}	2.2 V	0		5	MHz
	3 V	0		10	MHz
R _{Internal}	2.2 V, 3 V	45	60	80	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger

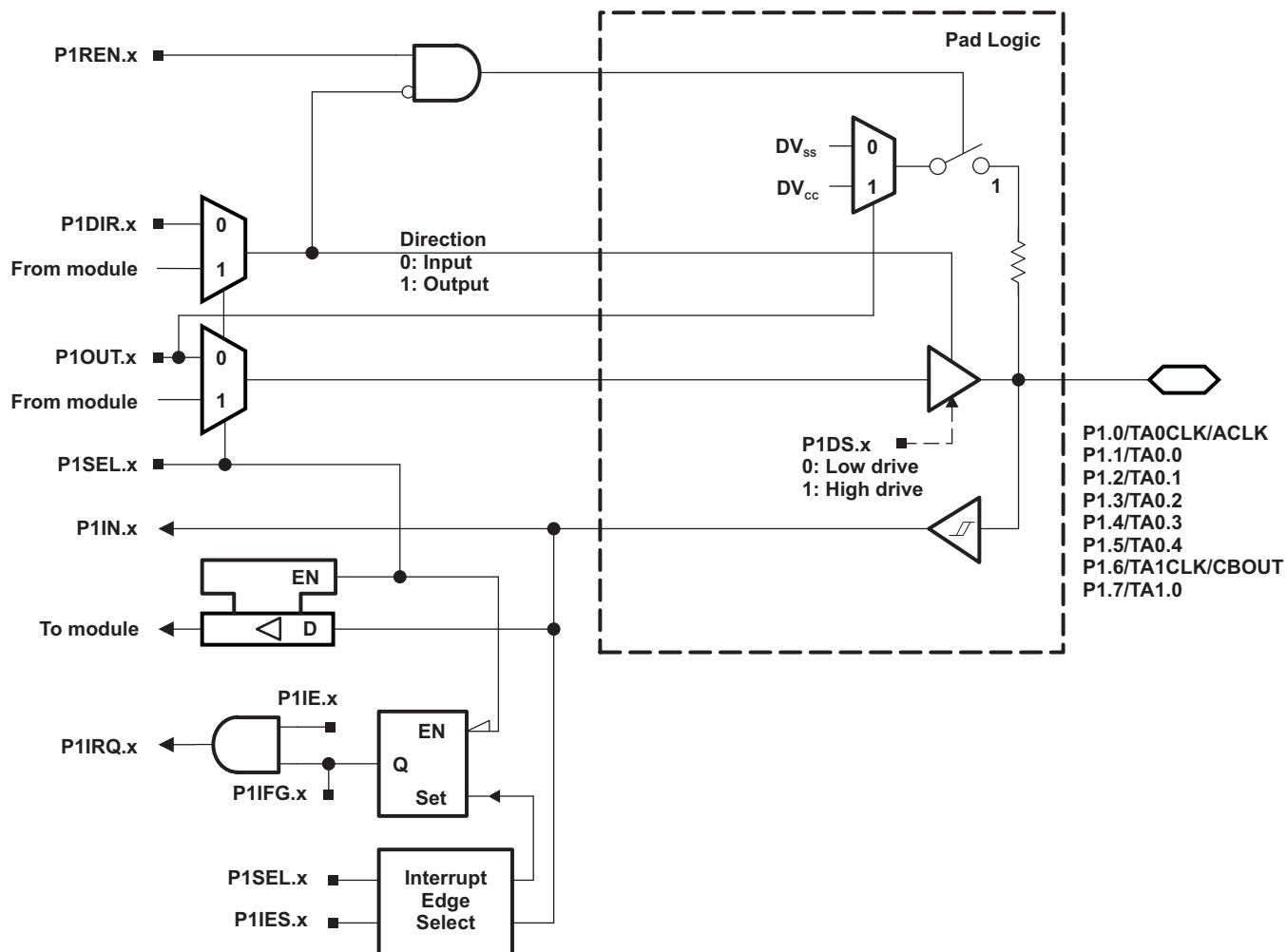


Table 48. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/TA1CLK/CBOUT	6	P1.6 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		CBOUT comparator B	1	1
P1.7/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1

Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger

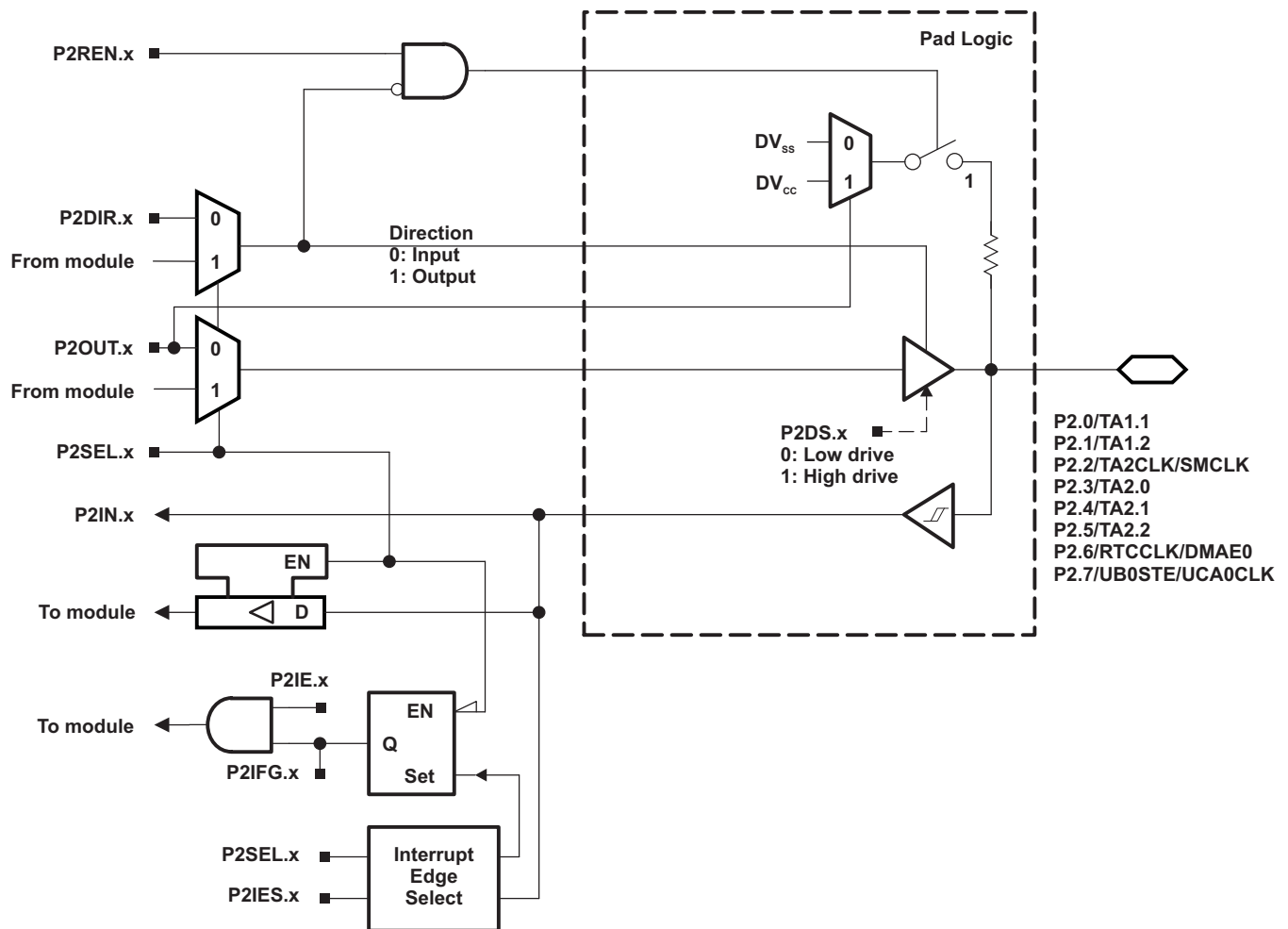


Table 49. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾	
			P2DIR.x	P2SEL.x
P2.0/TA1.1	0	P2.0 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	1
P2.1/TA1.2	1	P2.1 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	1
P2.2/TA2CLK/SMCLK	2	P2.2 (I/O)	I: 0; O: 1	0
		TA2CLK	0	1
		SMCLK	1	1
P2.3/TA2.0	3	P2.3 (I/O)	I: 0; O: 1	0
		TA2.CCI0A	0	1
		TA2.0	1	1
P2.4/TA2.1	4	P2.4 (I/O)	I: 0; O: 1	0
		TA2.CCI1A	0	1
		TA2.1	1	1
P2.5/TA2.2	5	P2.5 (I/O)	I: 0; O: 1	0
		TA2.CCI2A	0	1
		TA2.2	1	1
P2.6/RTCCLK/DMAE0	6	P2.6 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		RTCCLK	1	1
P2.7/UCB0STE/UCA0CLK	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK ^{(2) (3)}	X	1

(1) X = Don't care

(2) The pin direction is controlled by the USC1 module.

(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USC1 B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Port P3, P3.0 to P3.4, Input/Output With Schmitt Trigger

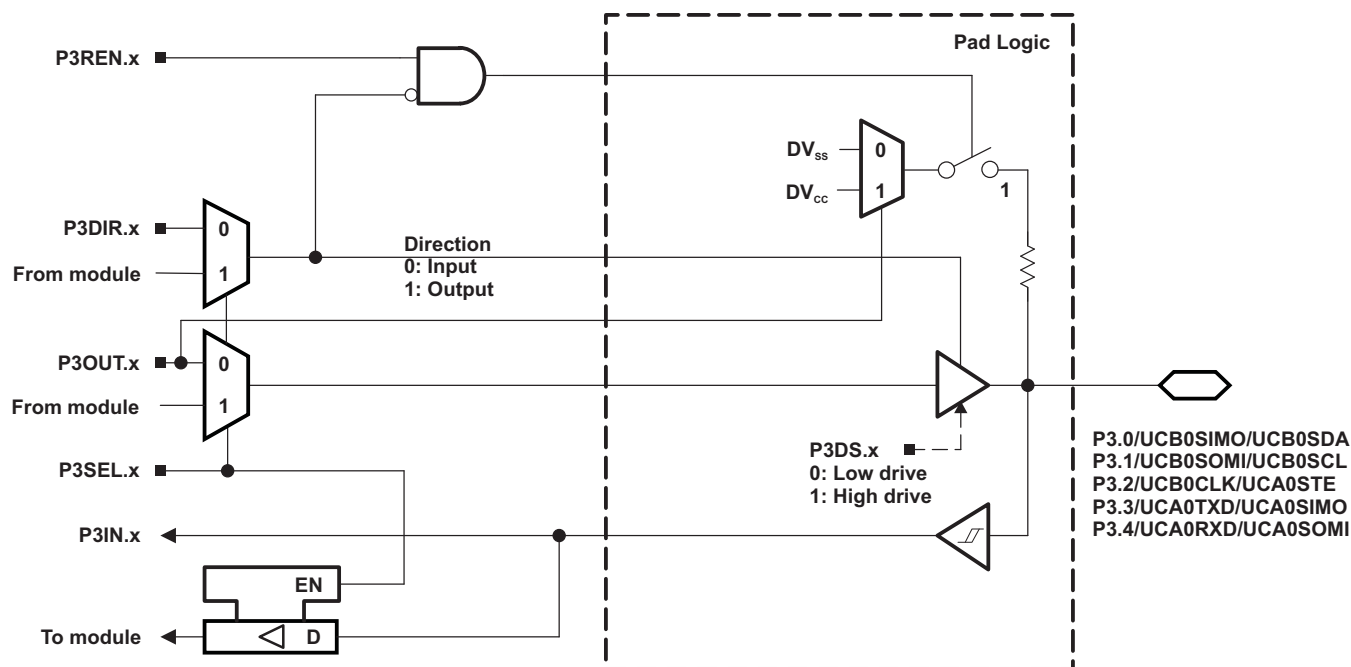


Table 50. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾	
			P3DIR.x	P3SEL.x
P3.0/UCB0SIMO/UCB0SDA	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA ^{(2) (3)}	X	1
P3.1/UCB0SOMI/UCB0SCL	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL ^{(2) (3)}	X	1
P3.2/UCB0CLK/UCA0STE	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE ^{(2) (4)}	X	1
P3.3/UCA0TXD/UCA0SIMO	3	P3.3 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO ⁽²⁾	X	1
P3.4/UCA0RXD/UCA0SOMI	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI ⁽²⁾	X	1

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

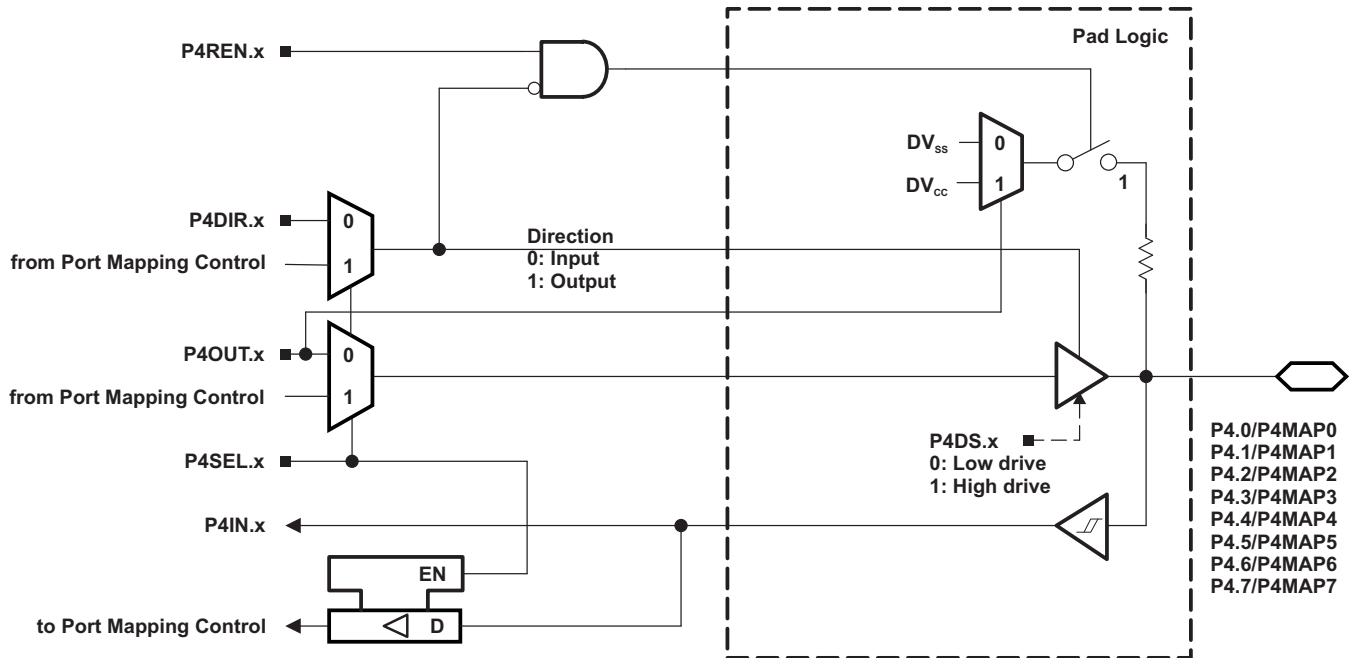


Table 51. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS		
			P4DIR.x ⁽¹⁾	P4SEL.x	P4MAPx
P4.0/P4MAP0	0	P4.0 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.1/P4MAP1	1	P4.1 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.2/P4MAP2	2	P4.2 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.3/P4MAP3	3	P4.3 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.4/P4MAP4	4	P4.4 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.5/P4MAP5	5	P4.5 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.6/P4MAP6	6	P4.6 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.7/P4MAP7	7	P4.7 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30

(1) The direction of some mapped secondary functions are controlled directly by the module. See [Table 10](#) for specific direction control information of mapped secondary functions.

Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

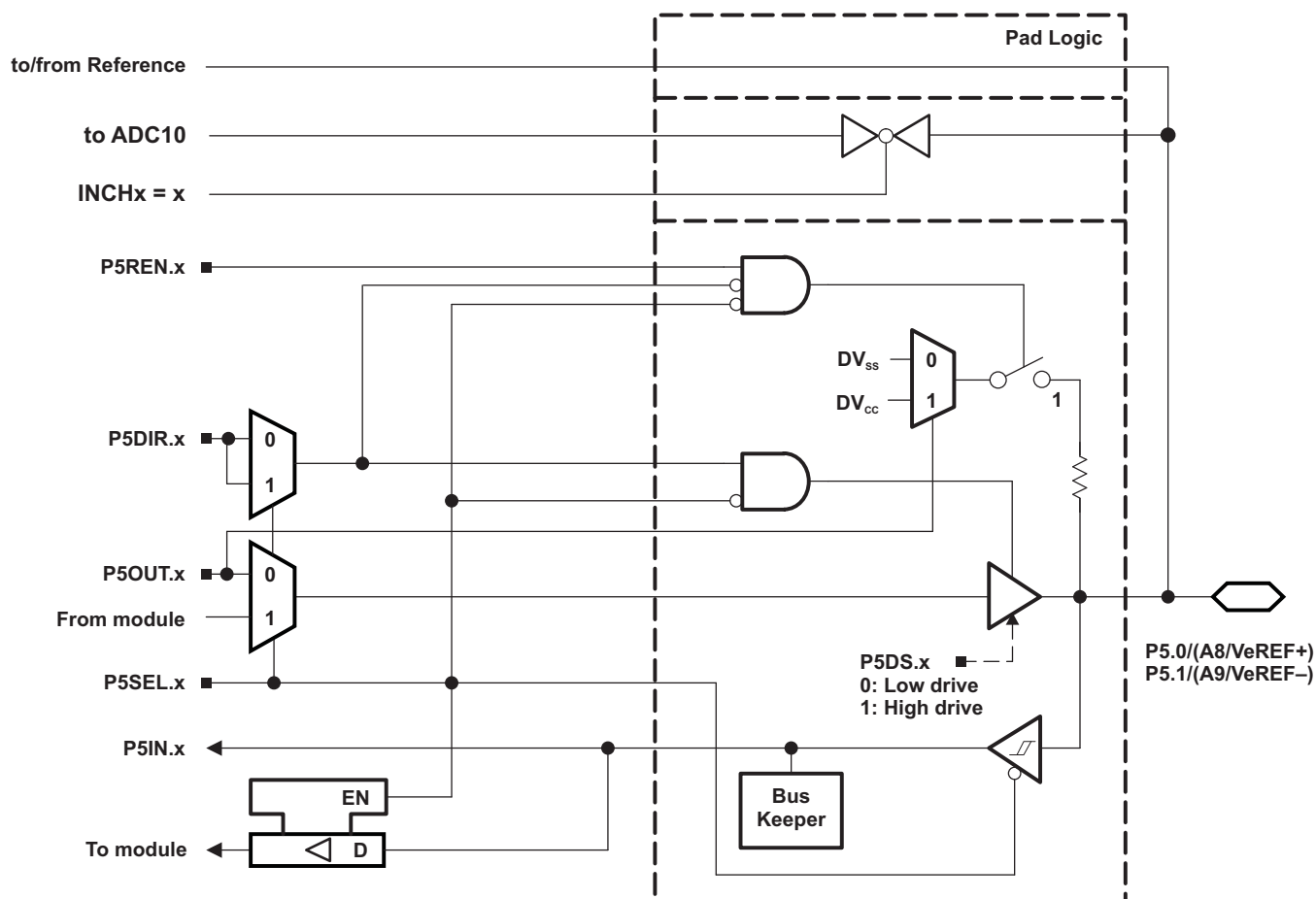


Table 52. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾	
			P5DIR.x	P5SEL.x
P5.0/A8/VeREF+ ⁽²⁾	0	P5.0 (I/O) ⁽³⁾	I: 0; O: 1	0
		A8/VeREF+ ⁽⁴⁾	X	1
P5.1/A9/VeREF- ⁽⁵⁾	1	P5.1 (I/O) ⁽³⁾	I: 0; O: 1	0
		A9/VeREF- ⁽⁶⁾	X	1

(1) X = Don't care

(2) VeREF+ available on devices with ADC10_A.

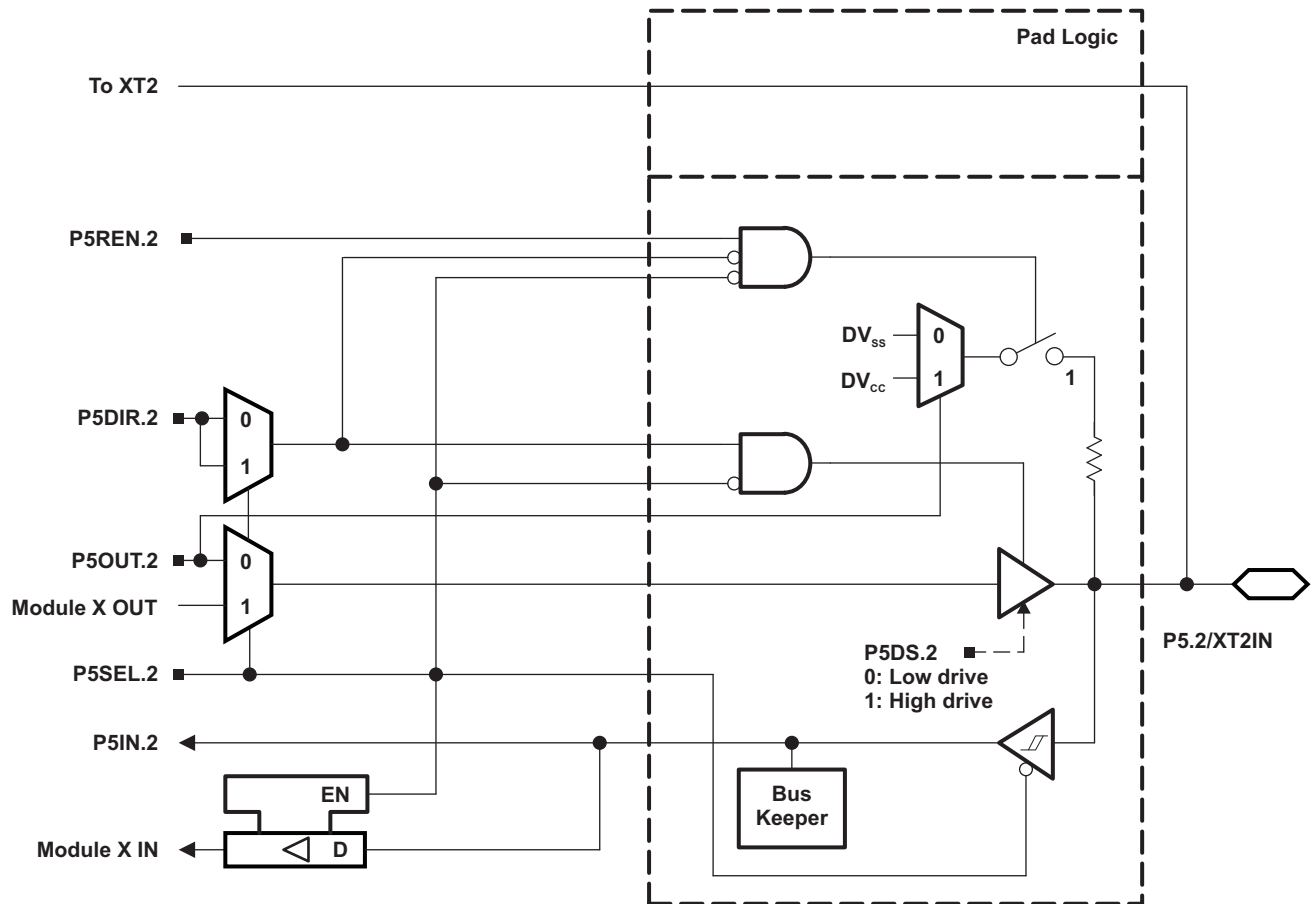
(3) Default condition

(4) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC10_A when available.

(5) VeREF- available on devices with ADC10_A.

(6) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC10_A when available.

Port P5, P5.2, Input/Output With Schmitt Trigger



Port P5, P5.3, Input/Output With Schmitt Trigger

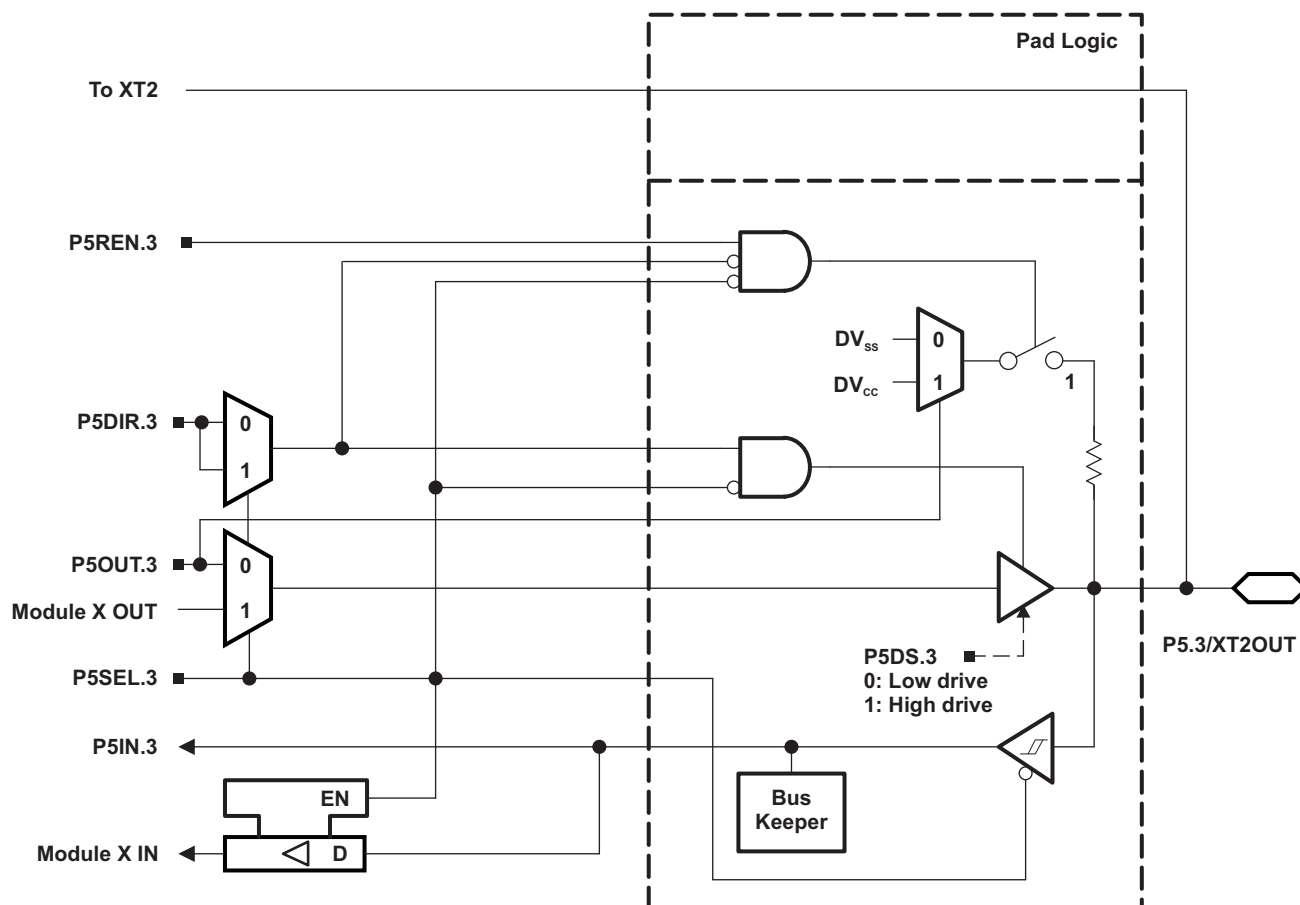


Table 53. Port P5 (P5.2, P5.3) Pin Functions

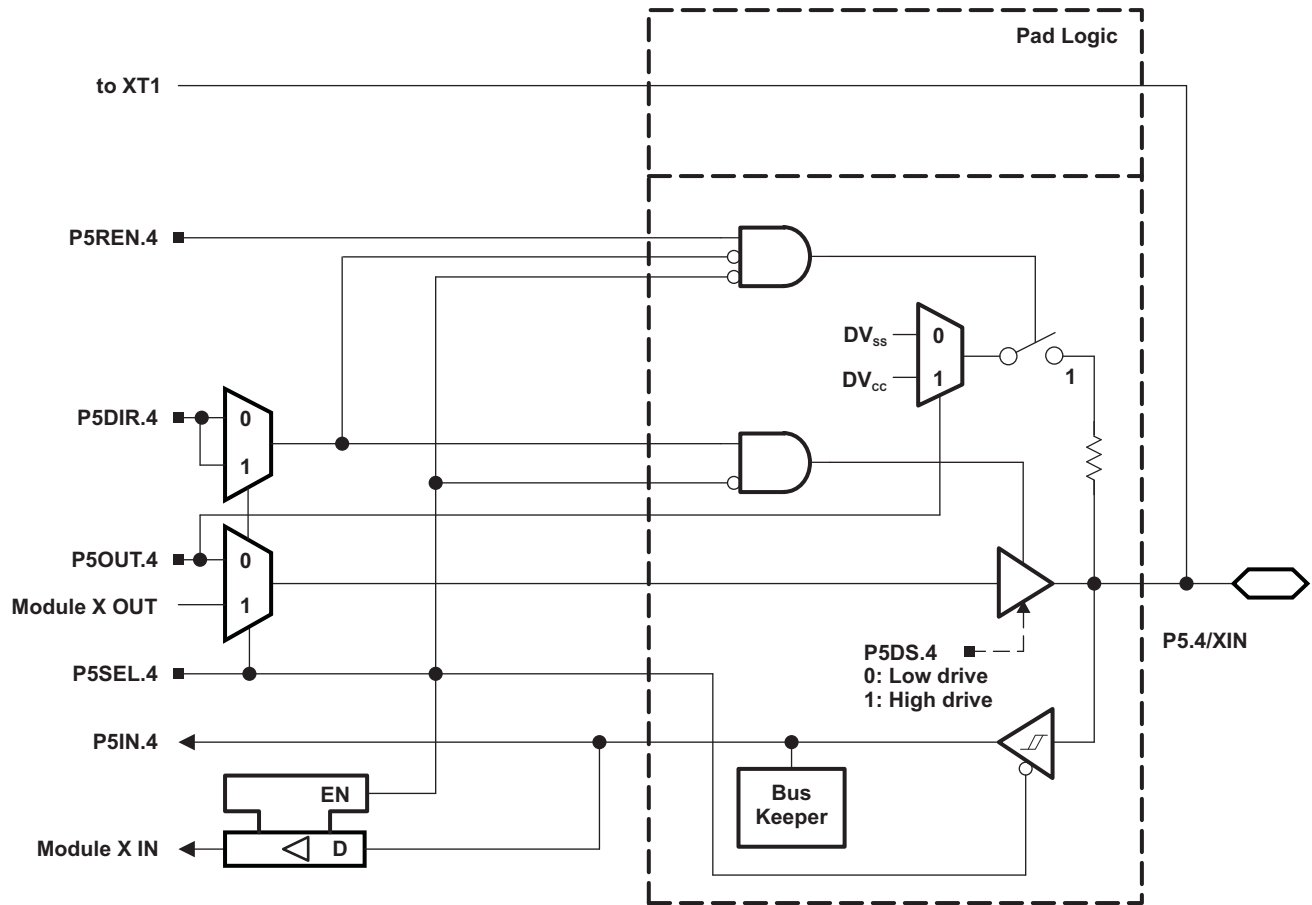
PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode ⁽²⁾	X	1	X	0
		XT2IN bypass mode ⁽²⁾	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	X	X
		XT2OUT crystal mode ⁽³⁾	X	1	X	0
		P5.3 (I/O) ⁽³⁾	X	1	X	1

(1) X = Don't care

(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

Port P5, P5.4 and P5.5 Input/Output With Schmitt Trigger



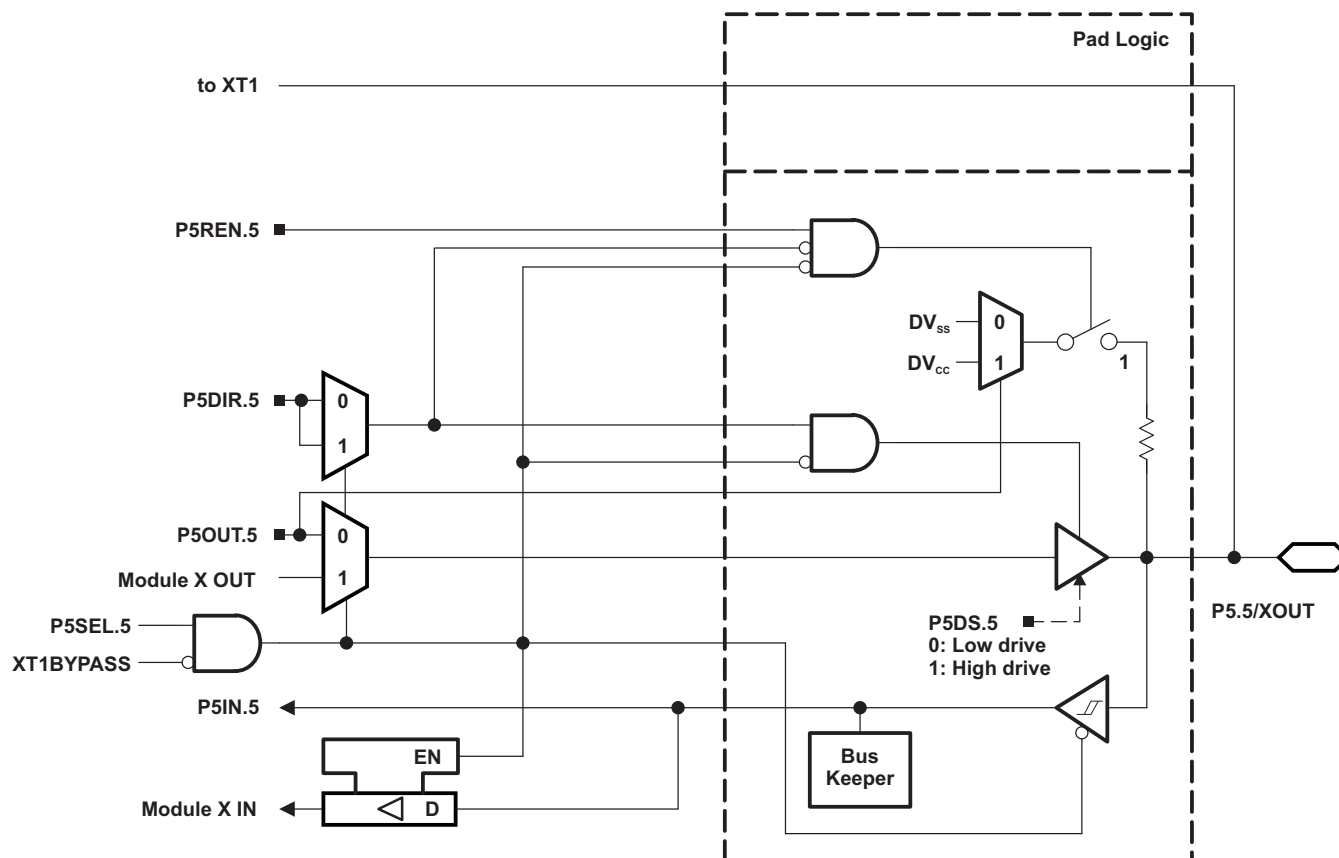


Table 54. Port P5 (P5.4 and P5.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS ⁽¹⁾			
			P5DIR.x	P5SEL.4	P5SEL.5	XT1BYPASS
P5.4/XIN	4	P5.4 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode ⁽²⁾	X	1	X	0
		XIN bypass mode ⁽²⁾	X	1	X	1
P5.5/XOUT	5	P5.5 (I/O)	I: 0; O: 1	0	X	X
		XOUT crystal mode ⁽³⁾	X	1	X	0
		P5.5 (I/O) ⁽³⁾	X	1	X	1

- (1) X = Don't care
- (2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.
- (3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.

Port P6, P6.0 to P6.7, Input/Output With Schmitt Trigger

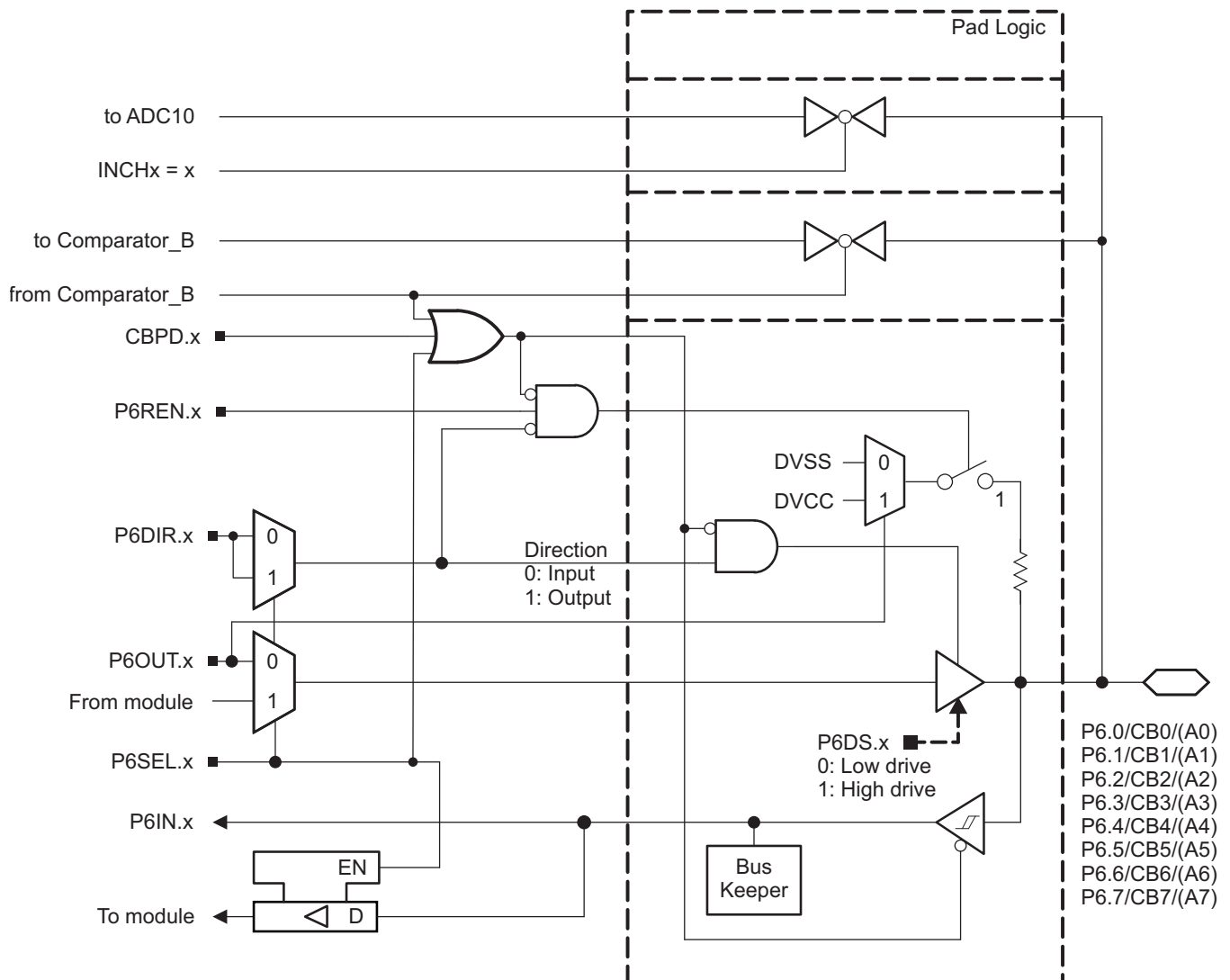


Table 55. Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS/SIGNALS		
			P6DIR.x	P6SEL.x	CBPD
P6.0/CB0/(A0)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		A0 (only on devices with ADC)	X	1	X
		CB0 ⁽¹⁾	X	X	1
P6.1/CB1/(A1)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		A1 (only on devices with ADC)	X	1	X
		CB1 ⁽¹⁾	X	X	1
P6.2/CB2/(A2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		A2 (only on devices with ADC)	X	1	X
		CB2 ⁽¹⁾	X	X	1
P6.3/CB3/(A3)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		A3 (only on devices with ADC)	X	1	X
		CB3 ⁽¹⁾	X	X	1
P6.4/CB4/(A4)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		A4 (only on devices with ADC)	X	1	X
		CB4 ⁽²⁾	X	X	1
P6.5/CB5/(A5)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		A5 (only on devices with ADC)	X	1	X
		CB5 ⁽²⁾	X	X	1
P6.6/CB6/(A6)	6	P6.6 (I/O)	I: 0; O: 1	0	0
		A6 (only on devices with ADC)	X	1	X
		CB6 ⁽²⁾	X	X	1
P6.7/CB7/(A7)	7	P6.7 (I/O)	I: 0; O: 1	0	0
		A7 (only on devices with ADC)	X	1	X
		CB7 ⁽²⁾	X	X	1

- (1) Setting the CBPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.
- (2) Setting the CBPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

Port PU.0/DP, PU.1/DM, PUR USB Ports

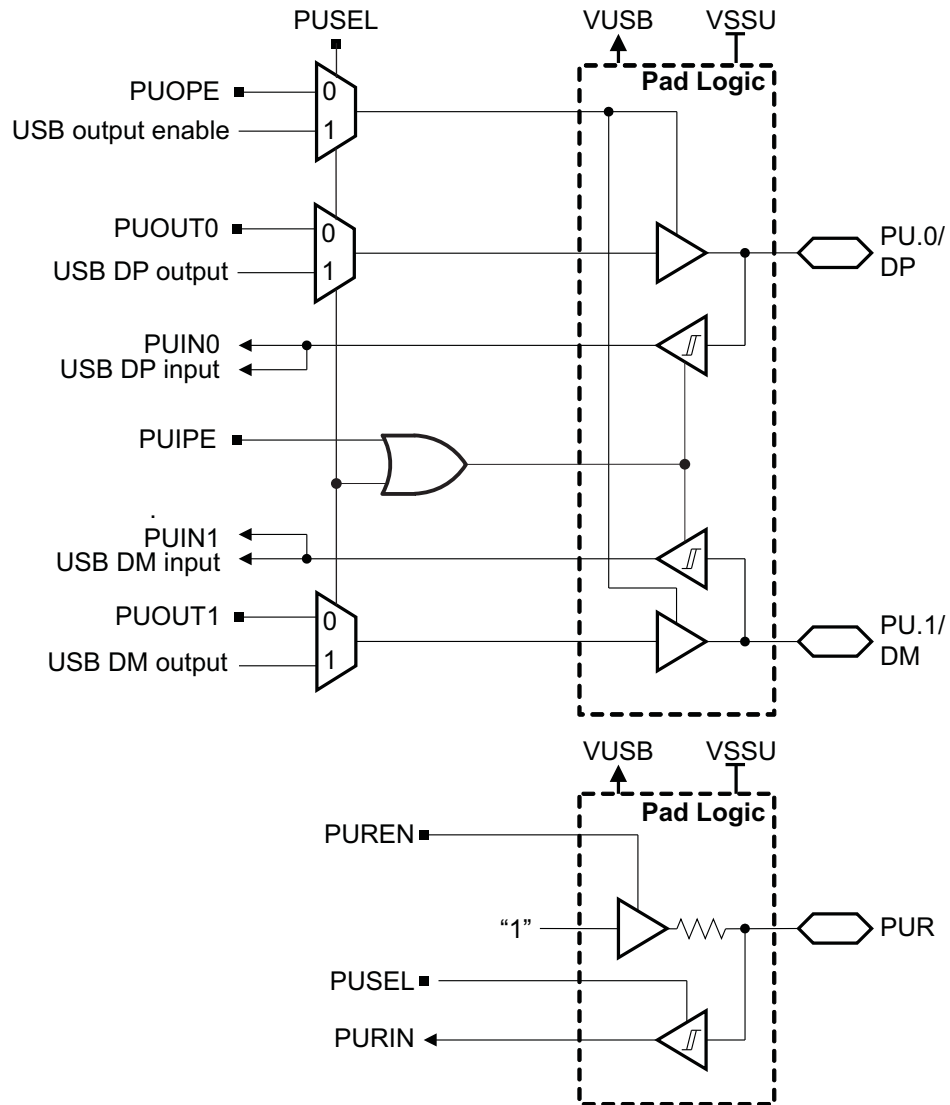


Table 56. Port PU.0/DP, PU.1/DM Output Functions⁽¹⁾

CONTROL BITS				PIN NAME	
PUSEL	PUOPE	PUOUT1	PUOUT0	PU.1/DM	PU.0/DP
0	0	X	X	Output disabled	Output disabled
0	1	0	0	Output low	Output low
0	1	0	1	Output low	Output high
0	1	1	0	Output high	Output low
0	1	1	1	Output high	Output high
1	X	X	X	DM ⁽²⁾	DP ⁽²⁾

- (1) PU.1/DM and PU.0/DP inputs and outputs are supplied from VUSB. VUSB can be generated by the device using the integrated 3.3-V LDO when enabled. VUSB can also be supplied externally when the 3.3-V LDO is not being used and is disabled.
- (2) Output state set by the USB module.

Table 57. Port PU.0/DP, PU.1/DM Input Functions⁽¹⁾

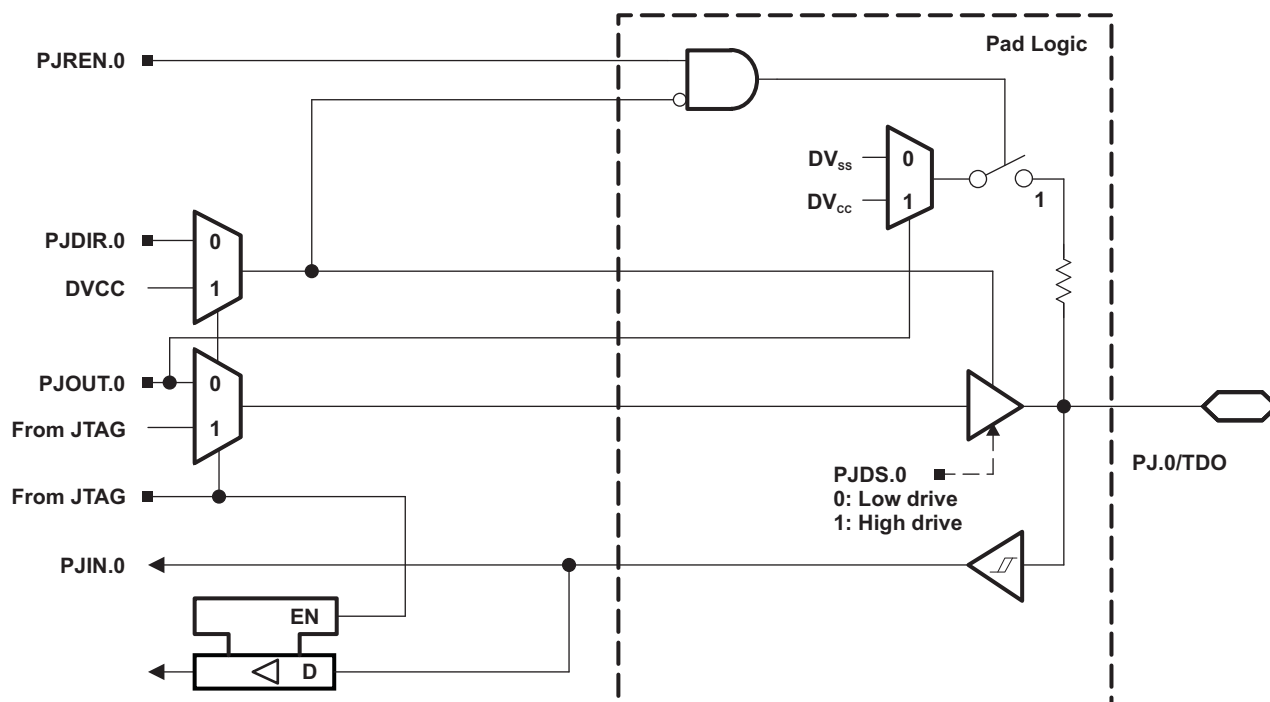
CONTROL BITS		PIN NAME	
PUSEL	PUIPE	PU.1/DM	PU.0/DP
0	0	Input disabled	Input disabled
0	1	Input enabled	Input enabled
1	X	DM input	DP input

- (1) PU.1/DM and PU.0/DP inputs and outputs are supplied from VUSB. VUSB can be generated by the device using the integrated 3.3-V LDO when enabled. VUSB can also be supplied externally when the 3.3-V LDO is not being used and is disabled.

Table 58. Port PUR Input Functions

CONTROL BITS		FUNCTION
PUSEL	PUREN	
0	0	Input disabled Pull up disabled
0	1	Input disabled Pull up enabled
1	0	Input enabled Pull up disabled
1	1	Input enabled Pull up enabled

Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

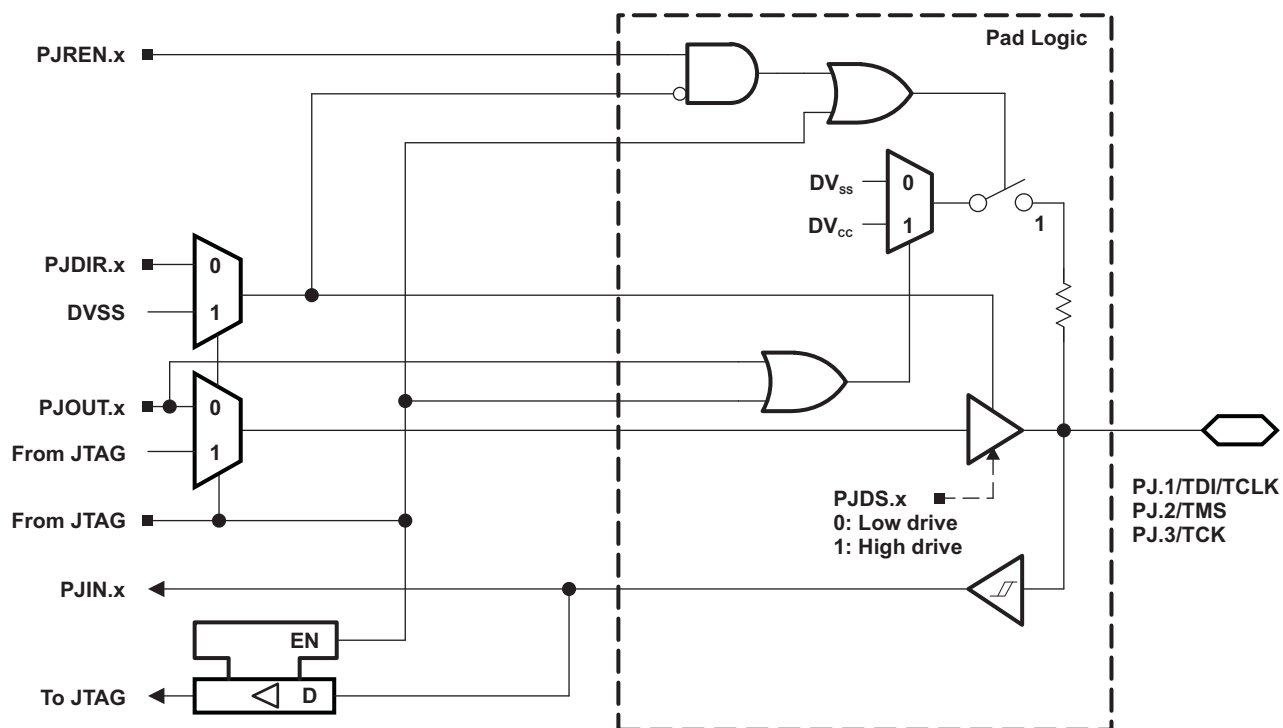


Table 59. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS ⁽¹⁾
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O) ⁽²⁾	I: 0; O: 1
		TDO ⁽³⁾	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O) ⁽²⁾	I: 0; O: 1
		TDI/TCLK ^{(3) (4)}	X
PJ.2/TMS	2	PJ.2 (I/O) ⁽²⁾	I: 0; O: 1
		TMS ^{(3) (4)}	X
PJ.3/TCK	3	PJ.3 (I/O) ⁽²⁾	I: 0; O: 1
		TCK ^{(3) (4)}	X

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

DEVICE DESCRIPTORS

Table 60 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 60. F5504 to F5510 Device Descriptor Table ⁽¹⁾

	DESCRIPTION	ADDRESS	SIZE (bytes)	F5510 RGC	F5510 RGZ	F5509 RGC	F5509 RGZ	F5508 RGC	F5508 RGZ	F5507	F5506	F5505	F5504
				VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	1	31h	31h	3Ah	3Ah	39h	39h	38h	37h	36h	35h
	Device ID	01A05h	1	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h
	Hardware revision	01A06h	1	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h	08h	08h	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
ADC10 Calibration	ADC10 Calibration Tag	01A14h	1	13h	13h	13h	13h	13h	13h	13h	13h	13h	13h
	ADC10 Calibration length	01A15h	1	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h
	ADC Gain Factor	01A16h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC Offset	01A18h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 30°C	01A1Ah	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 85°C	01A1Ch	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 30°C	01A1Eh	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 85°C	01A20h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
REF Calibration	REF Calibration Tag	01A26h	1	12h	12h	12h	12h	12h	12h	12h	12h	12h	12h
	REF Calibration length	01A27h	1	06h	06h	06h	06h	06h	06h	06h	06h	06h	06h
	REF 1.5-V Reference Factor	01A28h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	REF 2.0-V Reference Factor	01A2Ah	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	REF 2.5-V Reference Factor	01A2Ch	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
Peripheral Descriptor	Peripheral Descriptor Tag	01A2Eh	1	02h	02h	02h	02h	02h	02h	02h	02h	02h	02h
	Peripheral Descriptor Length	01A2Fh	1	61h	61h	62h	62h	61h	61h	5Dh	5Eh	5Dh	5Dh
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	00Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah

(1) N/A = Not applicable

Table 60. F5504 to F5510 Device Descriptor Table ⁽¹⁾ (continued)

	DESCRIPTION	ADDRESS	SIZE (bytes)	F5510 RGC	F5510 RGZ	F5509 RGC	F5509 RGZ	F5508 RGC	F5508 RGZ	F5507	F5506	F5505	F5504
				VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
	Memory 4		2	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch
	Memory 5		2	40h 92h	40h 92h	50h 91h	50h 91h	60h 90h	60h 90h	40h 92h	50h 91h	60h 90h	70h 8Eh
	Memory 6			N/A	N/A	8Eh	8Eh	N/A	N/A	N/A	8Eh	N/A	N/A
	delimiter		1	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
	Peripheral count		1	20h	20h	20h	20h	20h	20h	1Eh	1Eh	1Eh	1Eh
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-S		2	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h
	Port Mapping		2	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1/2		2	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h
	Port 3/4		2	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5/6		2	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h
	JTAG		2	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h

Table 60. F5504 to F5510 Device Descriptor Table ⁽¹⁾ (continued)

	DESCRIPTION	ADDRESS	SIZE (bytes)	F5510 RGC	F5510 RGZ	F5509 RGC	F5509 RGZ	F5508 RGC	F5508 RGZ	F5507	F5506	F5505	F5504
				VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A/B		2	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	10h 90h	10h 90h	10h 90h	10h 90h
	USCI_A/B		2	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	N/A	N/A	N/A	N/A
	ADC10_A		2	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h
	COMP_B		2	18h A8h	18h A8h	18h A8h	18h A8h	18h A8h	18h A8h	N/A	N/A	N/A	N/A
	USB		2	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	1Ch 98h	1Ch 98h	1Ch 98h	1Ch 98h
Interrupts	COMP_B		1	A8h	A8h	A8h	A8h	A8h	A8h	01h	01h	01h	01h
	TB0.CCIFG0		1	64h	64h	64h	64h	64h	64h	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h	65h	65h	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h	40h	40h	40h	40h	40h	40h
	USCI_A0		1	90h	90h	90h	90h	90h	90h	01h	01h	01h	01h
	USCI_B0		1	91h	91h	91h	91h	91h	91h	01h	01h	01h	01h
	ADC10_A		1	D0h	D0h	D0h	D0h	D0h	D0h	D0h	D0h	D0h	D0h
	TA0.CCIFG0		1	60h	60h	60h	60h	60h	60h	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h	61h	61h	61h	61h	61h	61h
	USB		1	98h	98h	98h	98h	98h	98h	98h	98h	98h	98h
	DMA		1	46h	46h	46h	46h	46h	46h	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h	62h	62h	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h	63h	63h	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h	50h	50h	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h	92h	92h	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h	93h	93h	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h	66h	66h	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h	67h	67h	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h	51h	51h	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h	68h	68h	68h	68h	68h	68h
	delimiter		1	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h

Table 61. F5500 to F5503 Device Descriptor Table⁽¹⁾

	DESCRIPTION	ADDRESS	SIZE (bytes)	F5503RGZ	F5502RGZ	F5501RGC	F5500RGZ
				VALUE	VALUE	VALUE	VALUE
Info Block	Info length	01A00h	1	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit
	Device ID	01A04h	1	34h	33h	32h	3Bh
	Device ID	01A05h	1	80h	80h	80h	80h
	Hardware revision	01A06h	1	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit	per unit
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit
ADC10 Calibration	Empty Tag	01A14h	1	05h	05h	05h	05h
	Empty Tag length	01A15h	1	10h	10h	10h	10h
REF Calibration	REF Calibration Tag	01A26h	1	12h	12h	12h	12h
	REF Calibration length	01A27h	1	06h	06h	06h	06h
	REF 1.5-V Reference Factor	01A28h	2	per unit	per unit	per unit	per unit
	REF 2.0-V Reference Factor	01A2Ah	2	per unit	per unit	per unit	per unit
Peripheral Descriptor	REF 2.5-V Reference Factor	01A2Ch	2	per unit	per unit	per unit	per unit
	Peripheral Descriptor Tag	01A2Eh	1	02h	02h	02h	02h
	Peripheral Descriptor Length	01A2Fh	1	5Dh	5Eh	5Dh	5Dh
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah
	Memory 4		2	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch
	Memory 5		2	40h 92h	50h 91	60h 90h	70h 8Eh
	Memory 6		1	N/A	8E	N/A	N/A
	delimiter		1	00h	00h	00h	00h
	Peripheral count		1	1Eh	1Eh	1Eh	1Eh
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-S		2	00h 03h	00h 03h	00h 03h	00h 03h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch

(1) N/A = Not applicable

Table 61. F5500 to F5503 Device Descriptor Table⁽¹⁾ (continued)

	DESCRIPTION	ADDRESS	SIZE (bytes)	F5503RGZ	F5502RGZ	F5501RGC	F5500RGZ
				VALUE	VALUE	VALUE	VALUE
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h
	Port Mapping		2	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1/2		2	04h 51h	04h 51h	04h 51h	04h 51h
	Port 3/4		2	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5/6		2	02h 53h	02h 53h	02h 53h	02h 53h
	JTAG		2	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A/B		2	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h
	USCI_A/B		2	04h 90h	04h 90h	04h 90h	04h 90h
	ADC10_A		2	N/A	N/A	N/A	N/A
	COMP_B		2	2Ch A8h	2Ch A8h	2Ch A8h	2Ch A8h
	USB		2	04h 98h	04h 98h	04h 98h	04h 98h
Interrupts	COMP_B		1	A8h	A8h	A8h	A8h
	TB0.CCIFG0		1	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h
	USCI_A0		1	01h	01h	01h	01h
	USCI_B0		1	01h	01h	01h	01h
	ADC10_A		1	01h	01h	01h	01h
	TA0.CCIFG0		1	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h
	USB		1	98h	98h	98h	98h
	DMA		1	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h

Table 61. F5500 to F5503 Device Descriptor Table⁽¹⁾ (continued)

	DESCRIPTION	ADDRESS	SIZE (bytes)	F5503RGZ	F5502RGZ	F5501RGC	F5500RGZ
				VALUE	VALUE	VALUE	VALUE
	P1		1	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h
	delimiter		1	00h	00h	00h	00h

REVISION HISTORY

VERSION	COMMENTS
SLAS645	Product Preview release
SLAS645A	Changes throughout for updated Product Preview
SLAS645B	Changes throughout for updated Product Preview
SLAS645C	Updated Embedded Emulation Module (EEM, Version S) section
SLAS645D	Changes throughout for Production Data release
SLAS645E	Released BGA package. Corrected V_{CB_REF} min and max values by swapping them as they were backward. Added I_{USB_LDO} and I_{VBUS_DETECT} to USB-PWR table. Added QFN thermal pad connection to pinout drawing and terminal function table. Updated t_{EN_REF} typ value from 0.3 to 1.
SLAS645F	Corrected F5504 to F5510 Device Descriptor Table addresses for ADC10 ADC Gain to Peripheral Descriptor Tag
SLAS645G	Table 1, Functional Block Diagram – MSP430F5510IRGZ, MSP430F5509IRGZ, MSP430F5508IRGZ, MSP430F5510IPT, MSP430F5509IPT, MSP430F5508IPT, Functional Block Diagram – MSP430F5507IRGZ, MSP430F5506IRGZ, MSP430F5505IRGZ, MSP430F5504IRGZ, MSP430F5504IPT, Functional Block Diagram – MSP430F5503IRGZ, MSP430F5502IRGZ, MSP430F5501IRGZ, MSP430F5500IRGZ : Changed to show correct number of USCI modules in RGZ and PT package options (one module). Functional Block Diagram – MSP430F5510IRGC, MSP430F5509IRGC, MSP430F5508IRGC, MSP430F5510IZQE, MSP430F5509IZQE, MSP430F5508IZQE , Corrected block diagram to show REF module available on devices with COMP_B . Table 3 , Changed description of ACLK and PUR signals. Table 4 , Corrected typo: UCAB0IV to UCB0IV. Table 12 , Changed SYSRSTIV interrupt event at 1Ch to Reserved. USB BSL , Added note regarding PUR terminal. Recommended Operating Conditions , Added note regarding interaction between minimum VCC and SVSH. Table 49, Table 50 , Corrected notes regarding USCI CLK functions taking precedence over USCI STE functions.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
MSP430F5500IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5500IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5501IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5501IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5502IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5502IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5503IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5503IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5504IPT	ACTIVE	LQFP	PT	48	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5504IPTR	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5504IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5504IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5505IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5505IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5506IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5506IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5507IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
MSP430F5507IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5508IPT	ACTIVE	LQFP	PT	48	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5508IPTR	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5508IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5508IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5508IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5508IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5508IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430F5508IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430F5509IPT	ACTIVE	LQFP	PT	48	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5509IPTR	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5509IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5509IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5509IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5509IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5509IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
MSP430F5509IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430F5510IPT	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5510IPTR	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5510IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5510IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5510IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5510IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430F5510IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430F5510IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
XMS430F5510IRGCR	OBSOLETE	VQFN	RGC	64		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

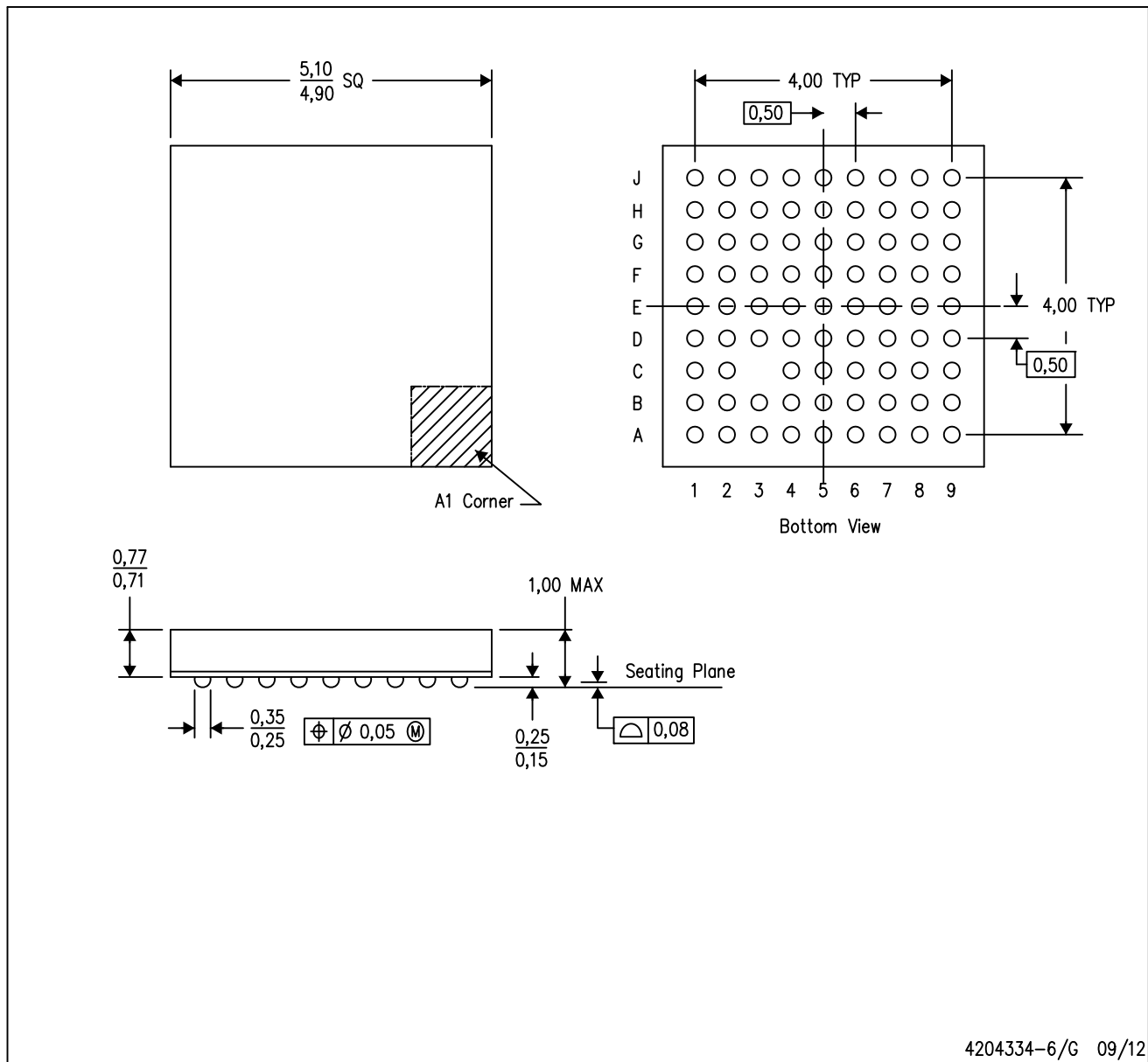
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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ZQE (S-PBGA-N80)

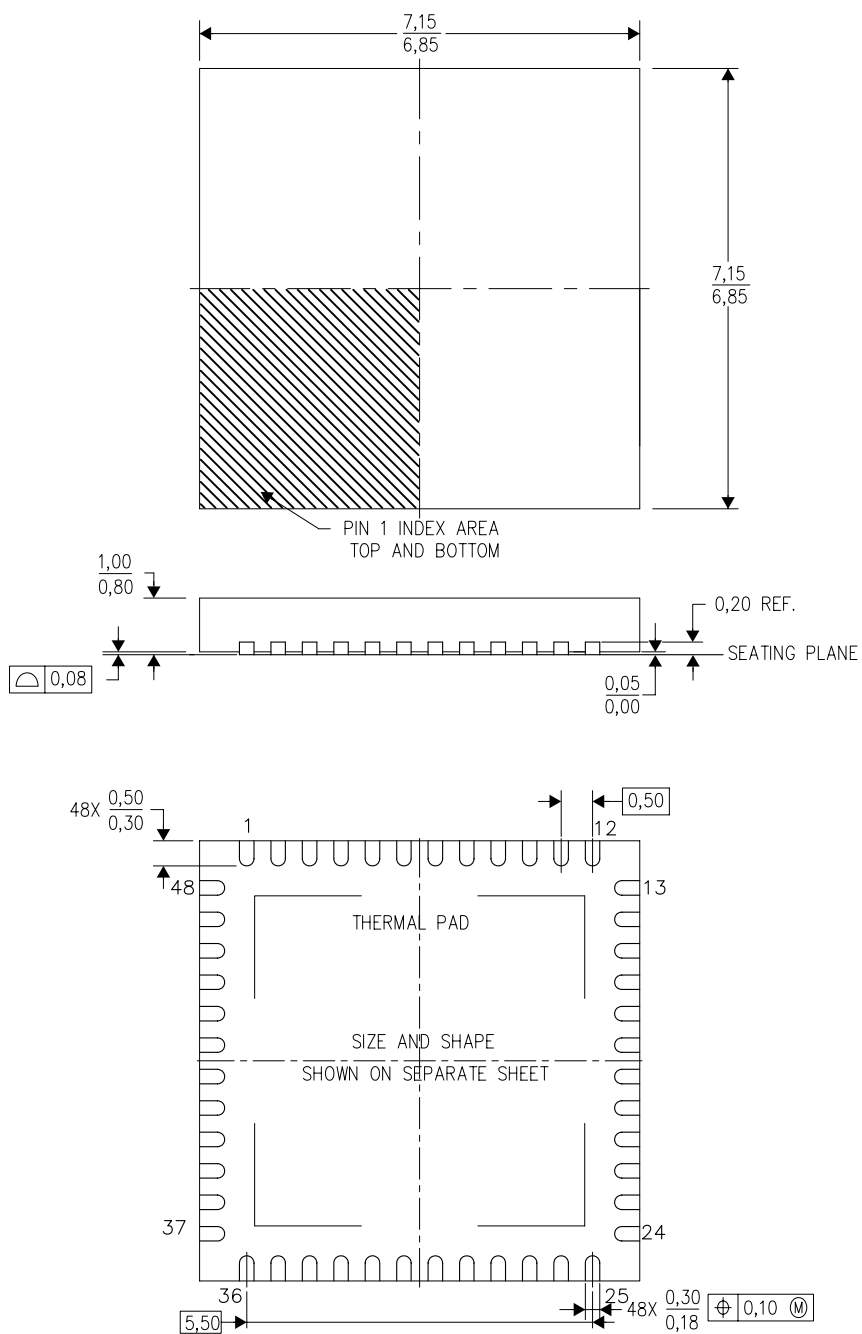
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225
 - D. This is a Pb-free solder ball design.

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

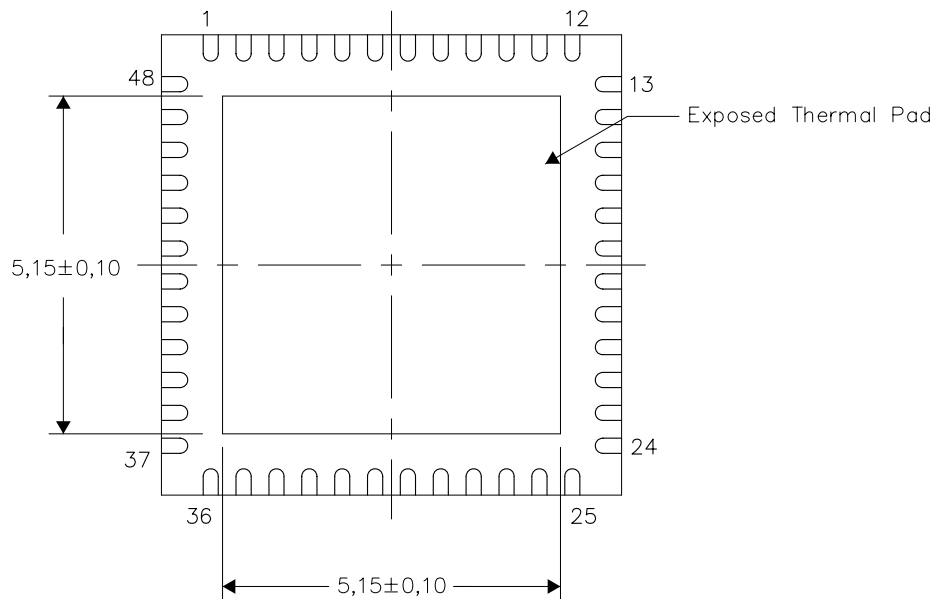
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

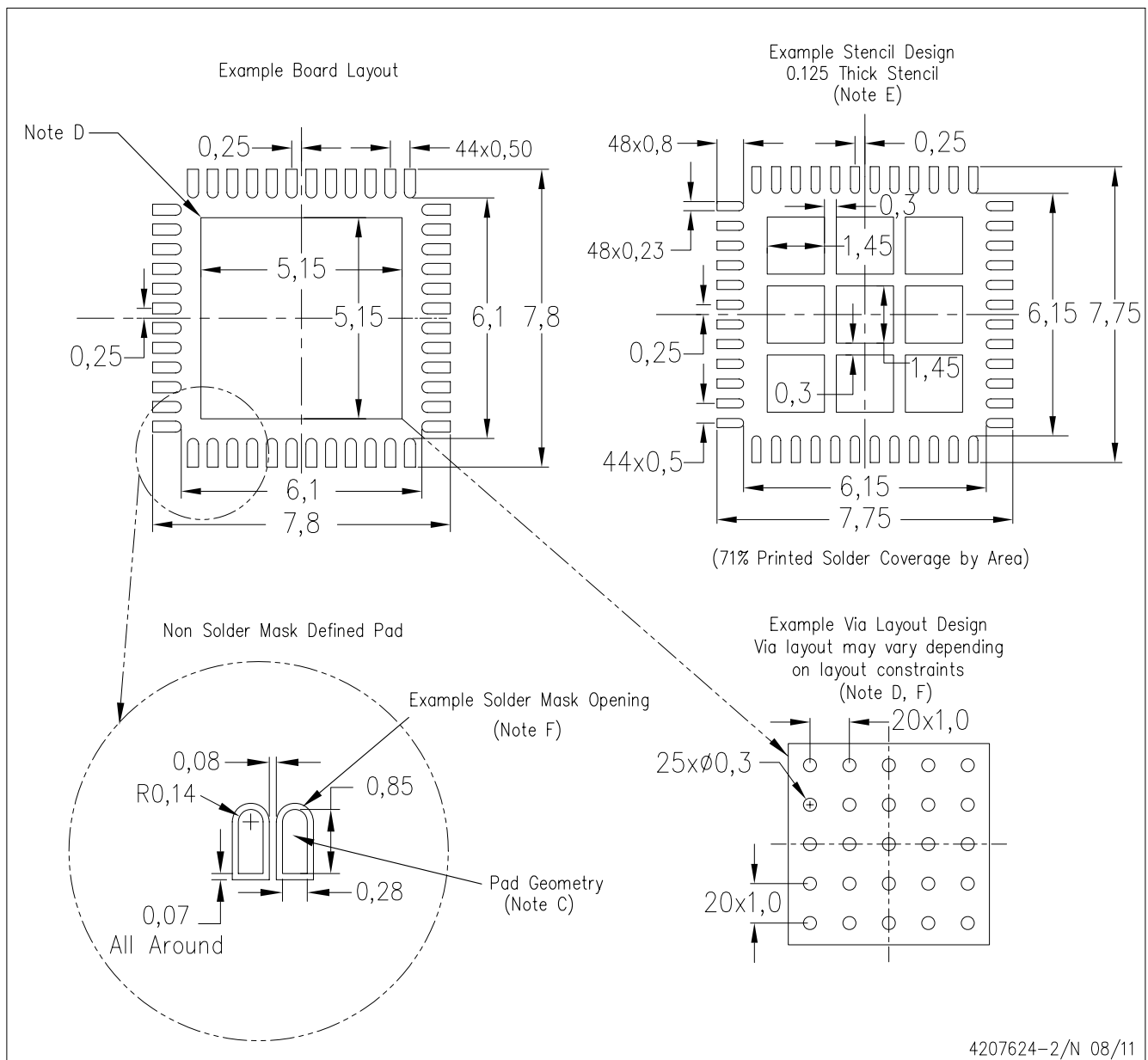
Exposed Thermal Pad Dimensions

4206354-2/R 08/11

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD

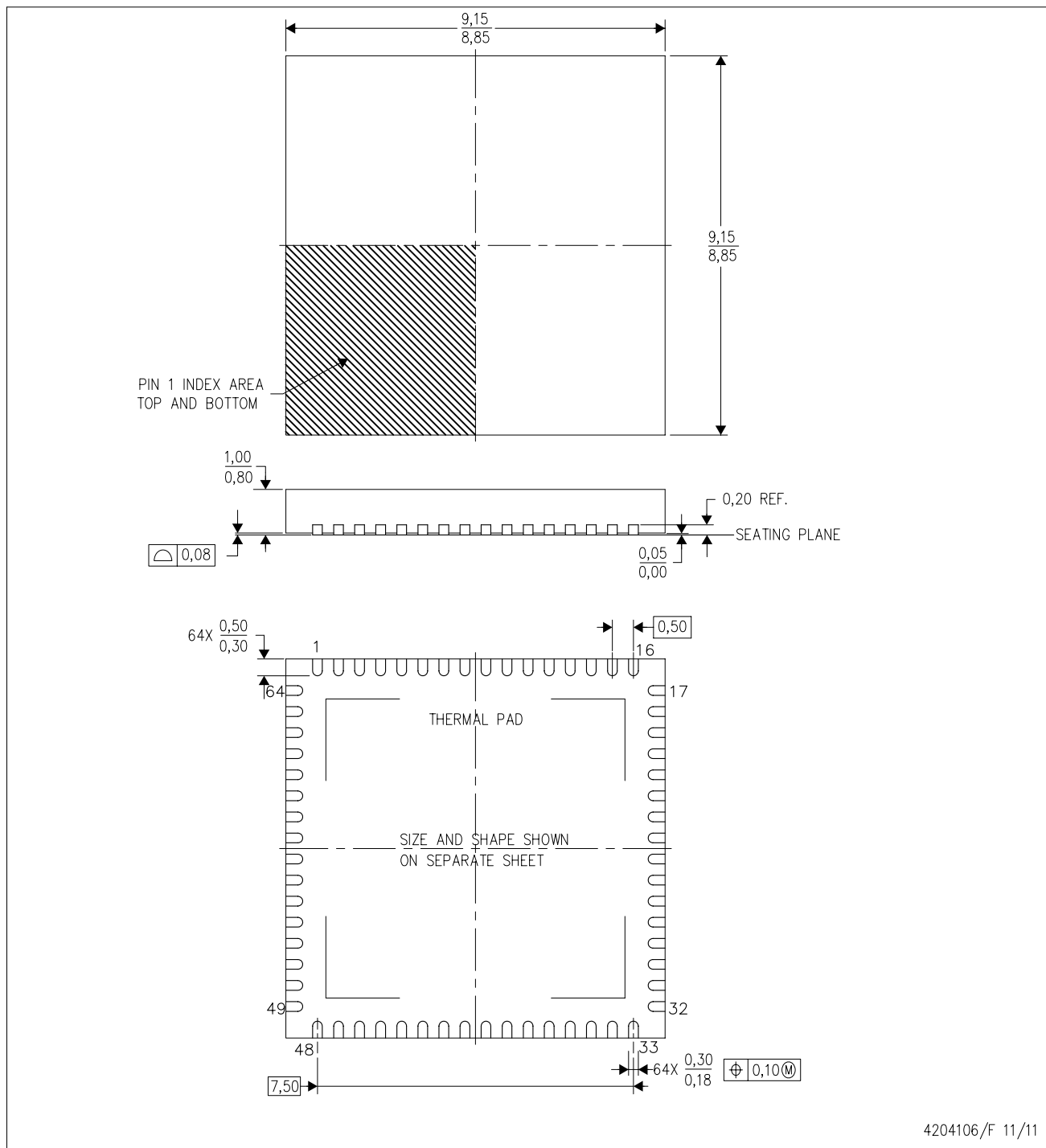


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RGC(S-PVQFN-N64)

CUSTOM DEVICE

PLASTIC QUAD FLATPACK NO-LEAD



4204106/F 11/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

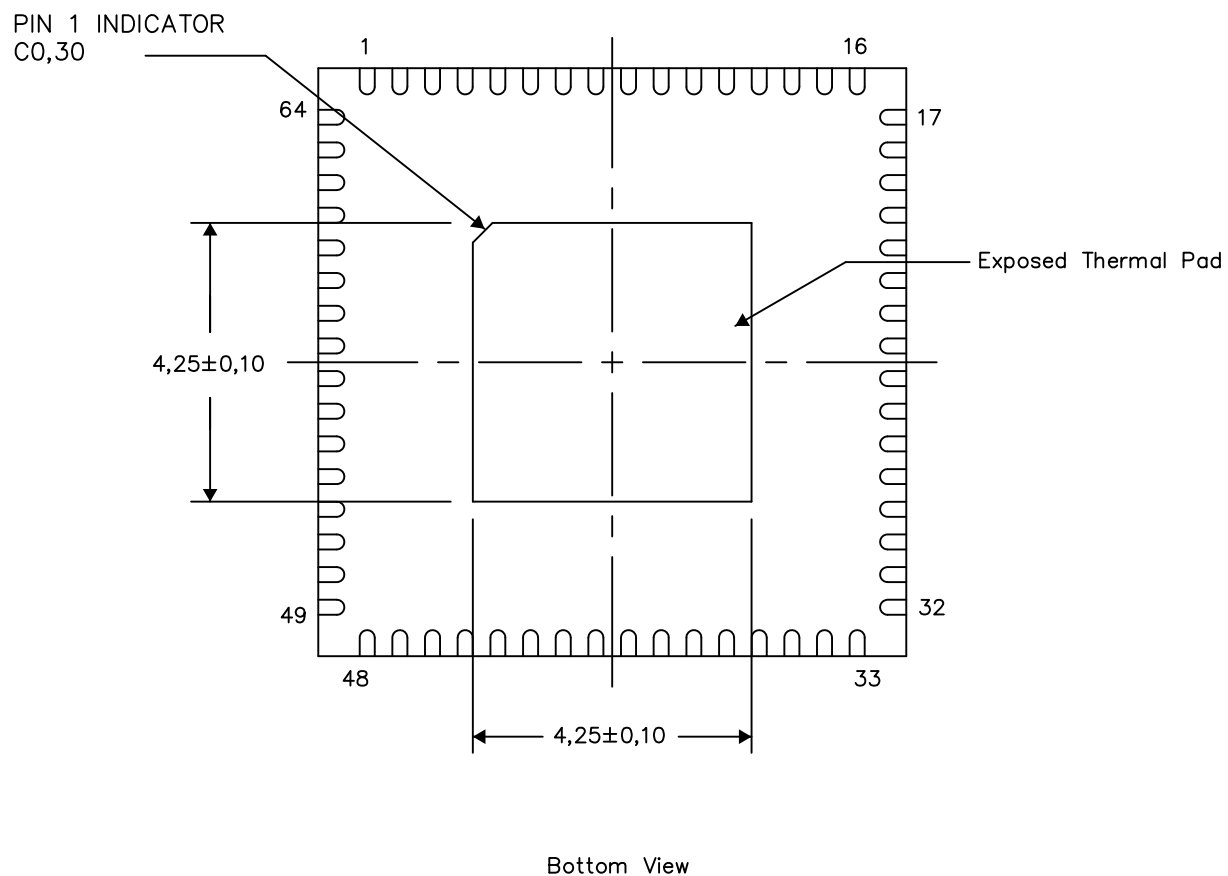
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



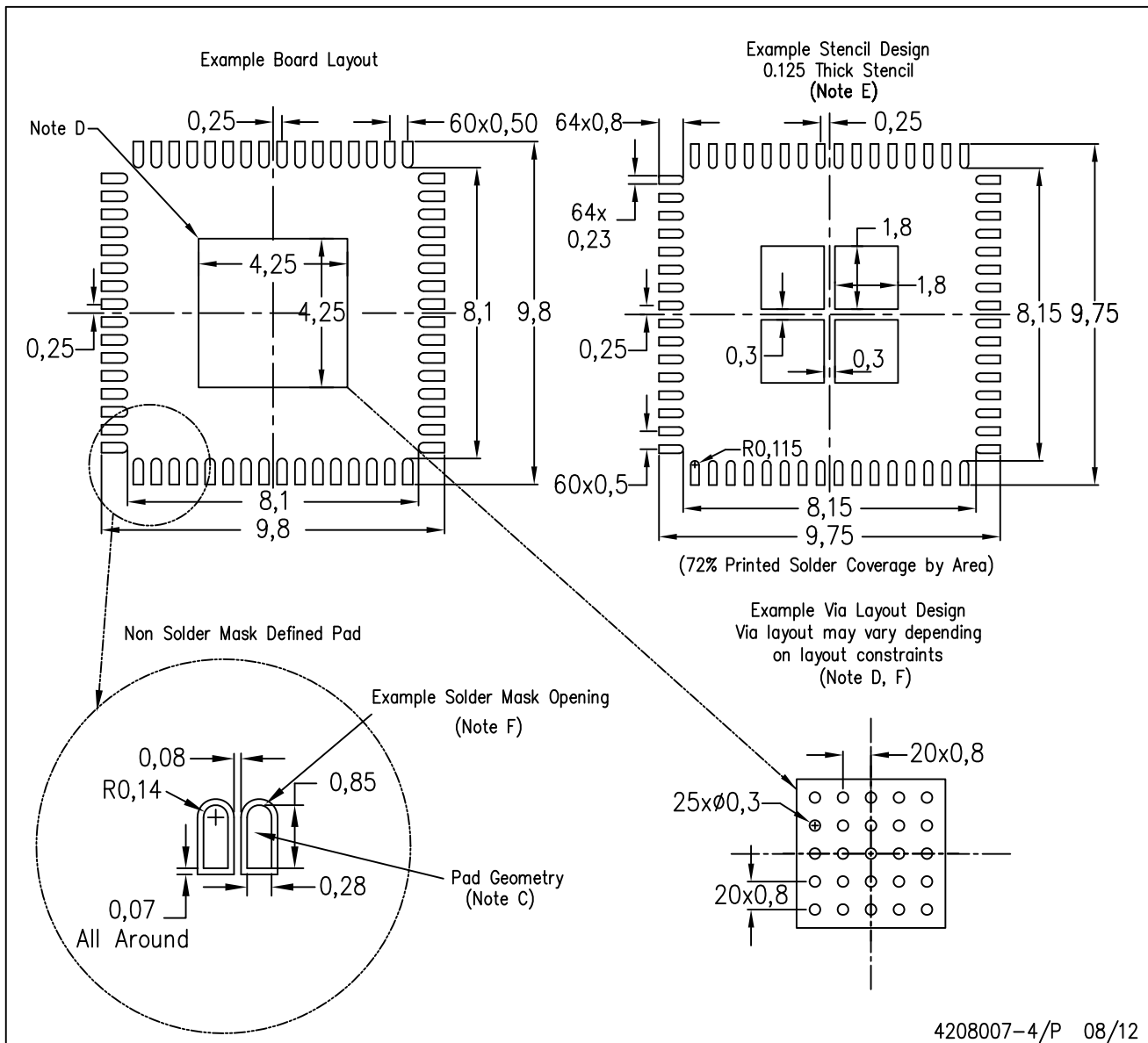
Exposed Thermal Pad Dimensions

4206192-3/U 08/12

NOTE: A. All linear dimensions are in millimeters

RGC (S-PVQFN-N64)

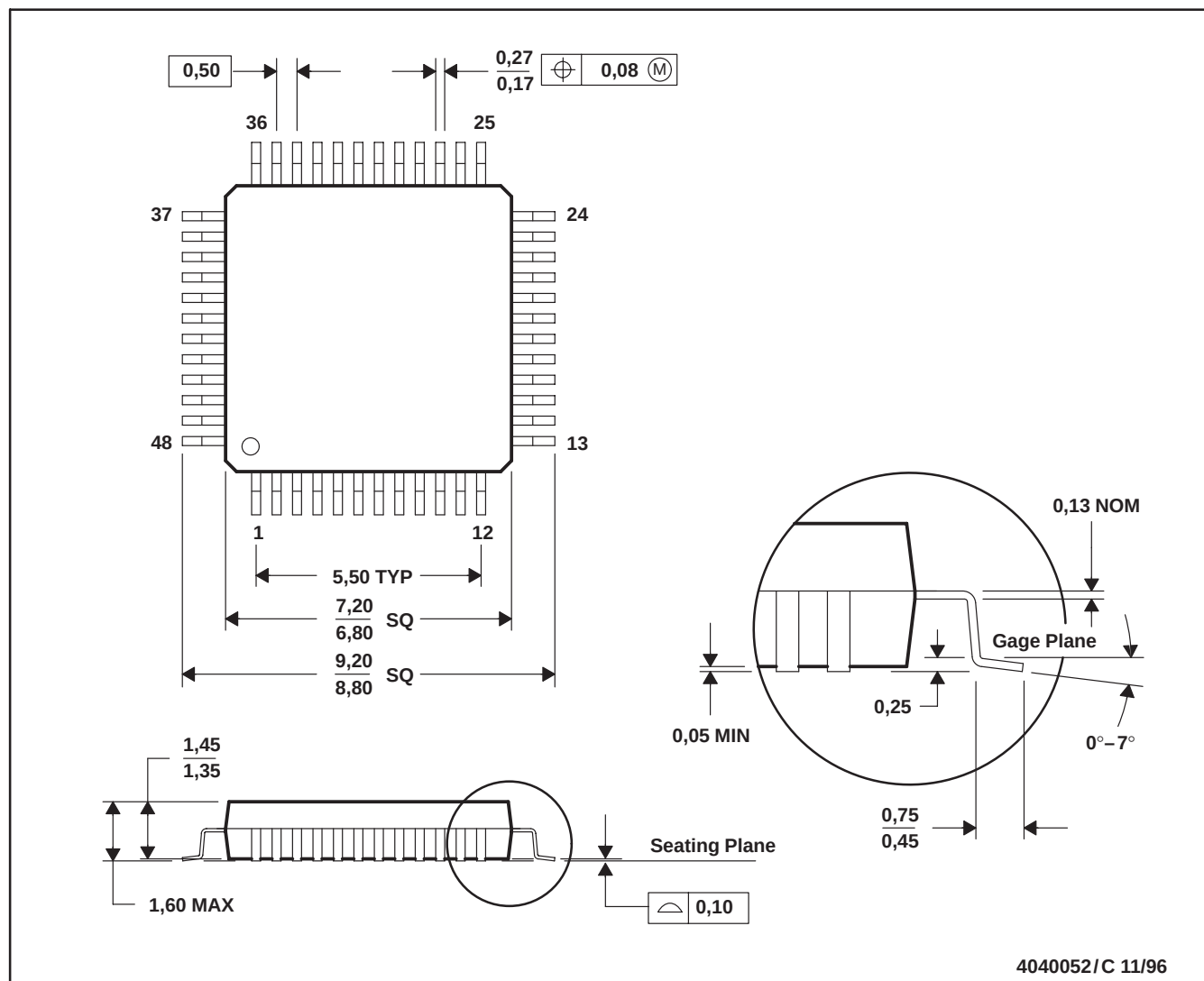
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

PT (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-026
 - This may also be a thermally enhanced plastic package with leads connected to the die pads.

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