MIXED SIGNAL MICROCONTROLLER

FEATURES

- Embedded Microcontroller
  - 16-Bit RISC Architecture up to 16-MHz Clock
  - Wide Supply Voltage Range (1.8 V to 3.6 V)
- Optimized Ultra-Low-Power Modes

Mode	Consumption (Typical)
Active Mode	100 µA/MHz
Standby (LPM3 With VLO)	0.7 µA
Real-Time Clock (LPM3.5 With Crystal)	0.5 µA
Shutdown (LPM4.5)	0.1 µA

- Ultra-Low-Power Ferroelectric RAM (FRAM)
  - Up to 64KB Nonvolatile Memory
  - Ultra-Low-Power Writes
  - Fast Write at 125 ns Per Word (64KB in 4 ms)
  - Unified Memory = Program + Data + Storage in One Single Space
  - 10^{15} Write Cycle Endurance
  - Radiation Resistant and Nonmagnetic
- Intelligent Digital Peripherals
  - 32-Bit Hardware Multiplier (MPY)
  - Three-Channel Internal DMA
  - Real-Time Clock With Calendar and Alarm Functions
  - Five 16-Bit Timers With up to Seven Capture/Compare Registers Each
  - 16-Bit Cyclic Redundancy Checker (CRC)
- High-Performance Analog
  - 16-Channel Analog Comparator
  - 14-Channel 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference and Sample-and-Hold
    - 200 ksps at 75-µA Consumption
- Code Security and Encryption
  - 128-Bit or 256-Bit AES Security Encryption and Decryption Coprocessor (MSP430FR59xx Only)
  - Random Number Seed for Random Number Generation Algorithms
- Enhanced Serial Communication
  - eUSCI_A0 and eUSCI_A1 Support:
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI at Rates up to 10 Mbps
  - eUSCI_B0 Supports:
    - I^2C With Multi-Slave Addressing
    - SPI at Rates up to 8 Mbps
  - Hardware UART and I^2C Bootstrap Loader (BSL)
- Flexible Clock System
  - Fixed-Frequency DCO With Ten Selectable Factory-Trimmed Frequencies
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - 32-kHz Crystals (LFXT)
  - High-Frequency Crystals (HFXT)
- Development Tools and Software
  - Free Professional Development Environments
  - Development Kit (MSP-TS430RGZ48C)
- Family Members
  - 18 Variants in 3 Available Package Types Summarized in Table 2 and Table 3
- For Complete Module Descriptions, See the *MSP430FR59xx and MSP430FR58xx Family User's Guide* (SLAU367)

PRODUCT PREVIEW

DESCRIPTION

The Texas Instruments MSP430FR58xx and MSP430FR59xx family of ultra-low-power microcontrollers consists of several devices featuring embedded FRAM nonvolatile memory, an ultra-low-power 16-bit MSP430 CPU, and different sets of peripherals targeted for various applications. The architecture, FRAM, and peripherals, combined with seven low-power modes, are optimized to achieve extended battery life in portable and wireless sensing applications. FRAM is a new nonvolatile memory that combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash, all at lower total power consumption.

The MSP430FR59xx devices provide an 256-bit AES security encryption and decryption coprocessor. The family members available are summarized in Table 2.

MSP430FR58xx devices do not provide AES encryption and decryption in hardware. The family members available are summarized in Table 3.

Table 1. Ordering Information(1)

T_A	PACKAGED DEVICES(2)		
	PLASTIC 48-PIN QFN (RGZ)	PLASTIC 40-PIN QFN (RHA)	PLASTIC 38-PIN TSSOP (DA)
–40°C to 85°C	MSP430FR5969IRGZ	MSP430FR5949IRHA	MSP430FR5949IDA
	MSP430FR5968IRGZ	MSP430FR5948IRHA	MSP430FR5948IDA
	MSP430FR5967IRGZ	MSP430FR5947IRHA	MSP430FR5947IDA
		MSP430FR5959IRHA	MSP430FR5959IDA
		MSP430FR5958IRHA	MSP430FR5958IDA
		MSP430FR5957IRHA	MSP430FR5957IDA
	MSP430FR5869IRGZ	MSP430FR5849IRHA	MSP430FR5849IDA
	MSP430FR5868IRGZ	MSP430FR5848IRHA	MSP430FR5848IDA
	MSP430FR5867IRGZ	MSP430FR5847IRHA	MSP430FR5847IDA
		MSP430FR5859IRHA	MSP430FR5859IDA
		MSP430FR5858IRHA	MSP430FR5858IDA
		MSP430FR5857IRHA	MSP430FR5857IDA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

PRODUCT PREVIEW

Table 2. MSP430FR59xx Family Members With AES

Device	FRAM (kB)	SRAM (kB)	Clock System	ADC12_B	Comp_E	Timer_A(1)	Timer_B(2)	eUSCI		AES + True Random Seed	I/O	Package Type
								Channel A: UART, IrDA, SPI	Channel B: SPI, I²C			
MSP430FR5969	64	2	Up to 16-MHz DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	40	48 RGZ
MSP430FR5968	48	2	Up to 16-MHz DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	40	48 RGZ
MSP430FR5967	32	1	Up to 16-MHz DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	40	48 RGZ
MSP430FR5949	64	2	Up to 16-MHz DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5948	48	2	Up to 16-MHz DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5947	32	1	Up to 16-MHz DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5959	64	2	Up to 16-MHz DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5958	48	2	Up to 16-MHz DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5957	32	1	Up to 16-MHz DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3(3) 2, 2(4)	7	2	1	yes	33	40 RHA
				12 ext, 2 int ch.							31	38 DA

(1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(2) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(3) Timers TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
(4) Timers TA2 and TA3 provide only internal capture/compare inputs and only internal PWM outputs (if any).

PRODUCT PREVIEW

Table 3. MSP430FR58xx Family Members Without AES

Device	FRAM (kB)	SRAM (kB)	Clock System	ADC12_B	Comp_E	Timer_A[1]	Timer_B[2]	eUSCI		AES + True Random Seed	I/O	Package Type
								Channel A: UART, IrDA, SPI	Channel B: SPI, I²C			
MSP430FR5869	64	2	Up to 16-MHz DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	40	48 RGZ
MSP430FR5868	48	2	Up to 16-MHz DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	40	48 RGZ
MSP430FR5867	32	1	Up to 16-MHz DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	40	48 RGZ
MSP430FR5849	64	2	Up to 16-MHz DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5848	48	2	Up to 16-MHz DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5847	32	1	Up to 16-MHz DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5859	64	2	Up to 16-MHz DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5858	48	2	Up to 16-MHz DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	33	40 RHA
				12 ext, 2 int ch.							31	38 DA
MSP430FR5857	32	1	Up to 16-MHz DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3[3] 2, 2[4]	7	2	1	no	33	40 RHA
				12 ext, 2 int ch.							31	38 DA

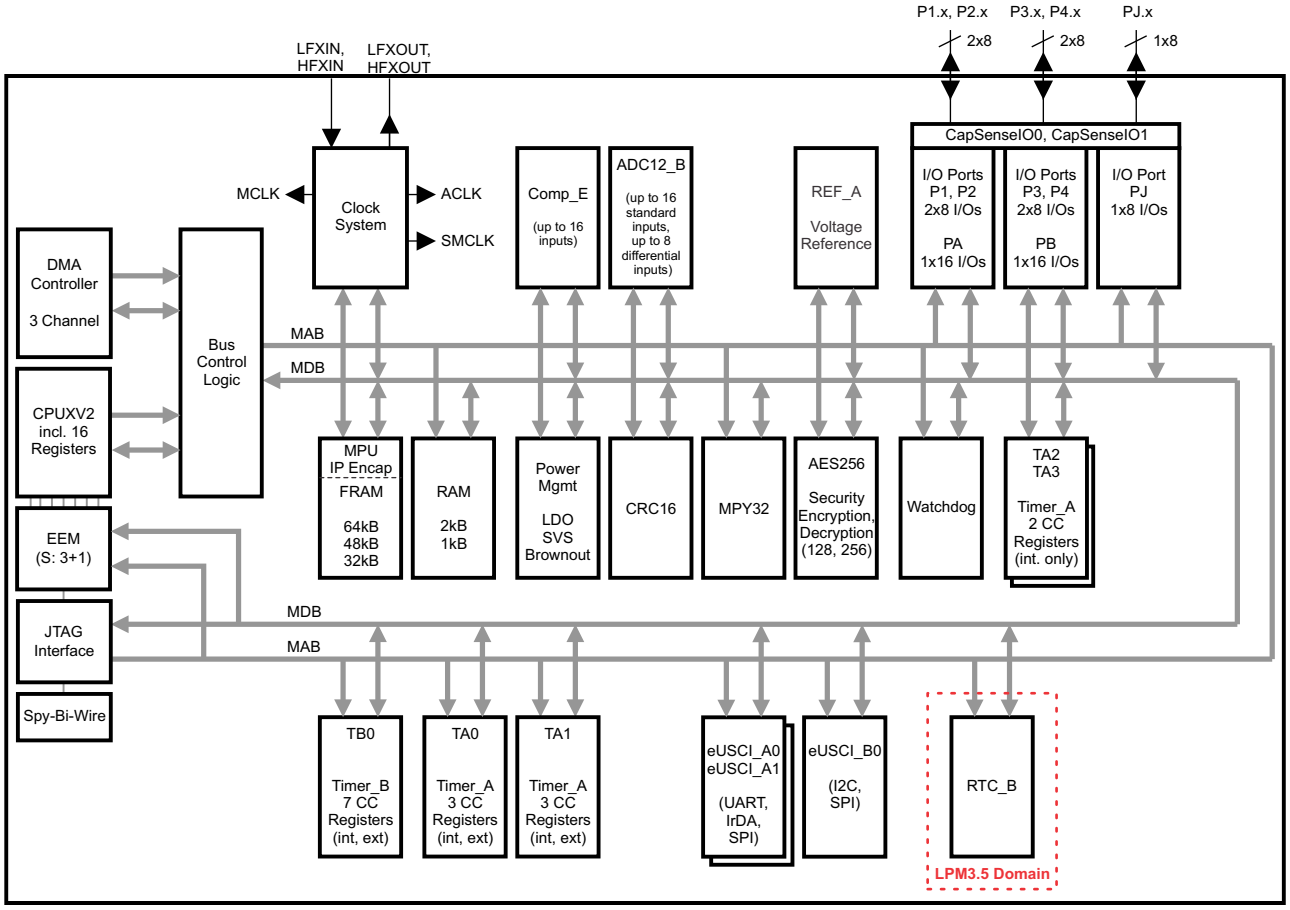
(1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

(2) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

(3) Timers TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.

(4) Timers TA2 and TA3 provide only internal capture/compare inputs and only internal PWM outputs (if any).

Functional Block Diagram



A. AES256 is not implemented in MSP430FR58xx devices.

B. The low-frequency (LF) crystal oscillator and the corresponding LFXIN and LFXOUT pins are available only in MSP430FR5x6x and MSP430FR5x4x devices.

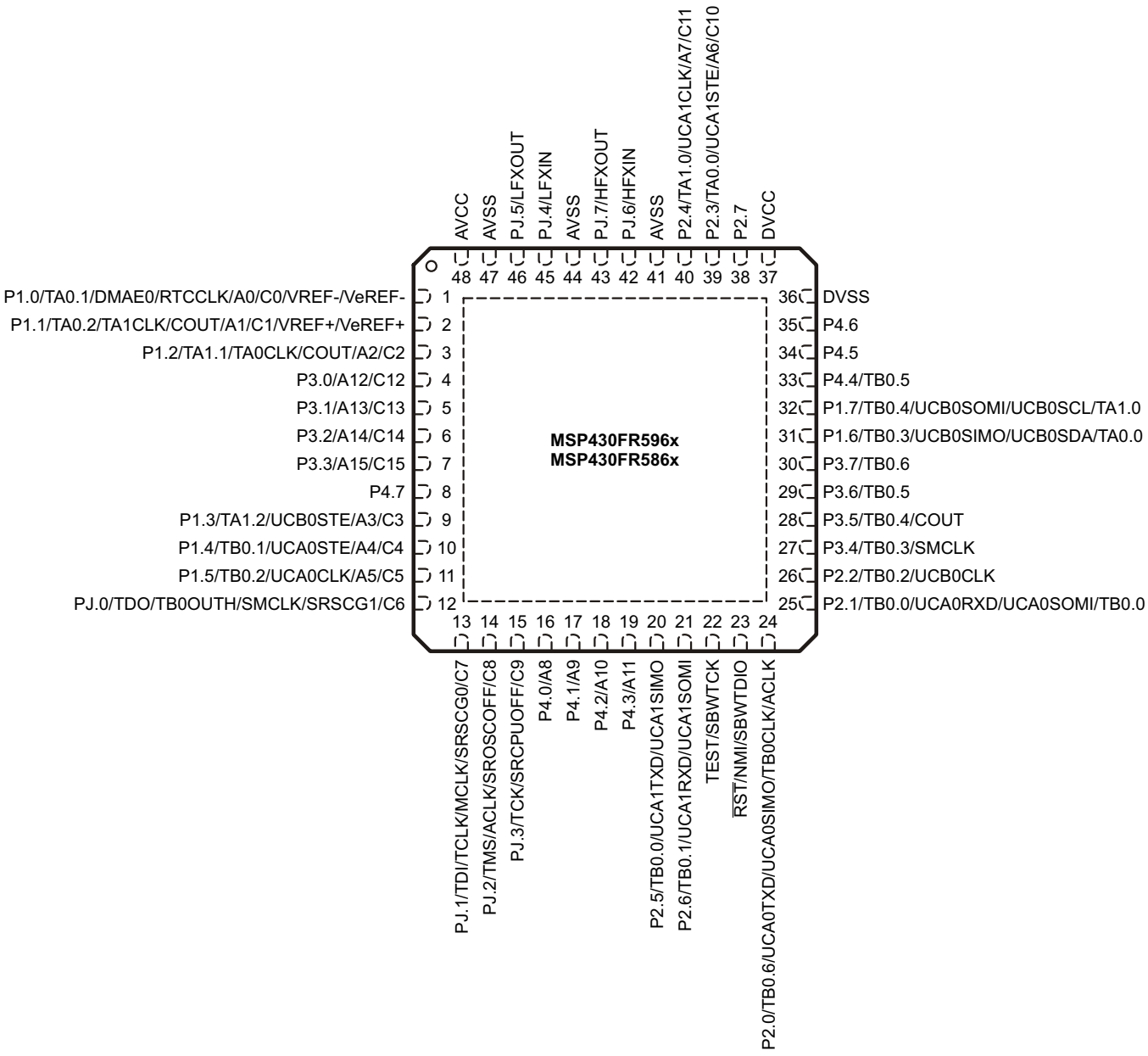
RTC_B is available only in conjunction with the LF crystal oscillator in MSP430FR5x6x and MSP430FR5x4x devices.

C. The high-frequency (HF) crystal oscillator and the corresponding HFXIN and HFXOUT pins are available only in MSP430FR5x6x and MSP430FR5x5x devices.

MSP430FR5x5x devices with the HF crystal oscillator only do not include the RTC_B module.

PRODUCT PREVIEW

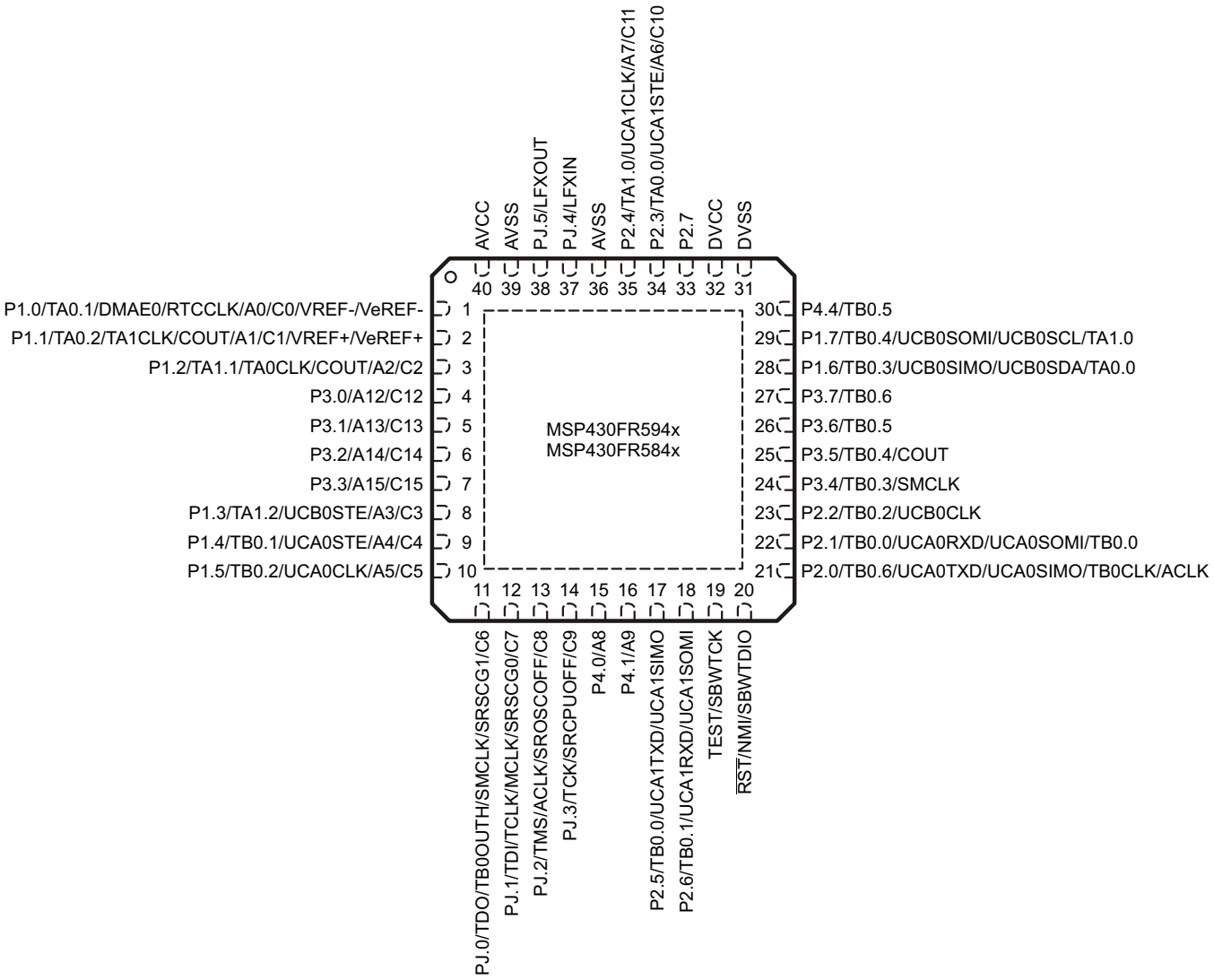
Pin Designation, RGZ - MSP430FR596x and MSP430FR586x



NOTE: QFN package pad connection to V_{SS} recommended.

PRODUCT PREVIEW

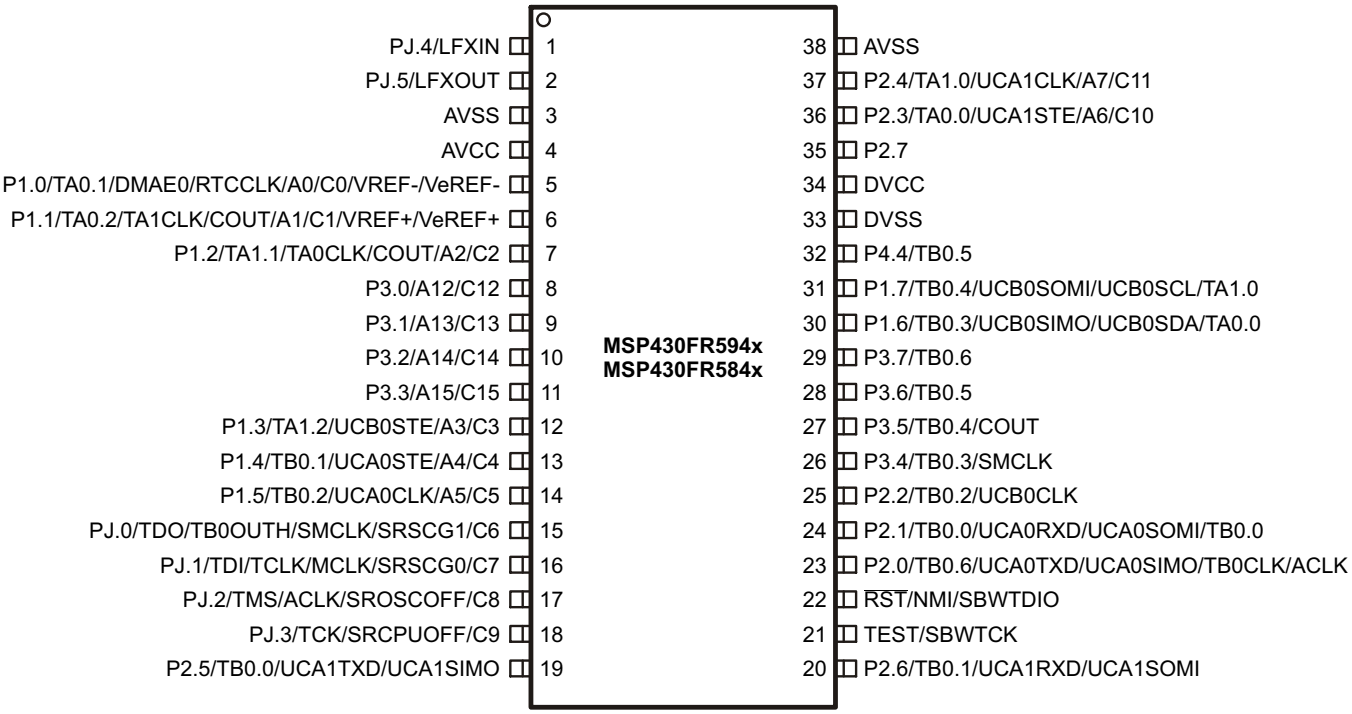
Pin Designation, RHA - MSP430FR594x and MSP430FR584x (LFXT Only)



NOTE: QFN package pad connection to V_{SS} recommended.

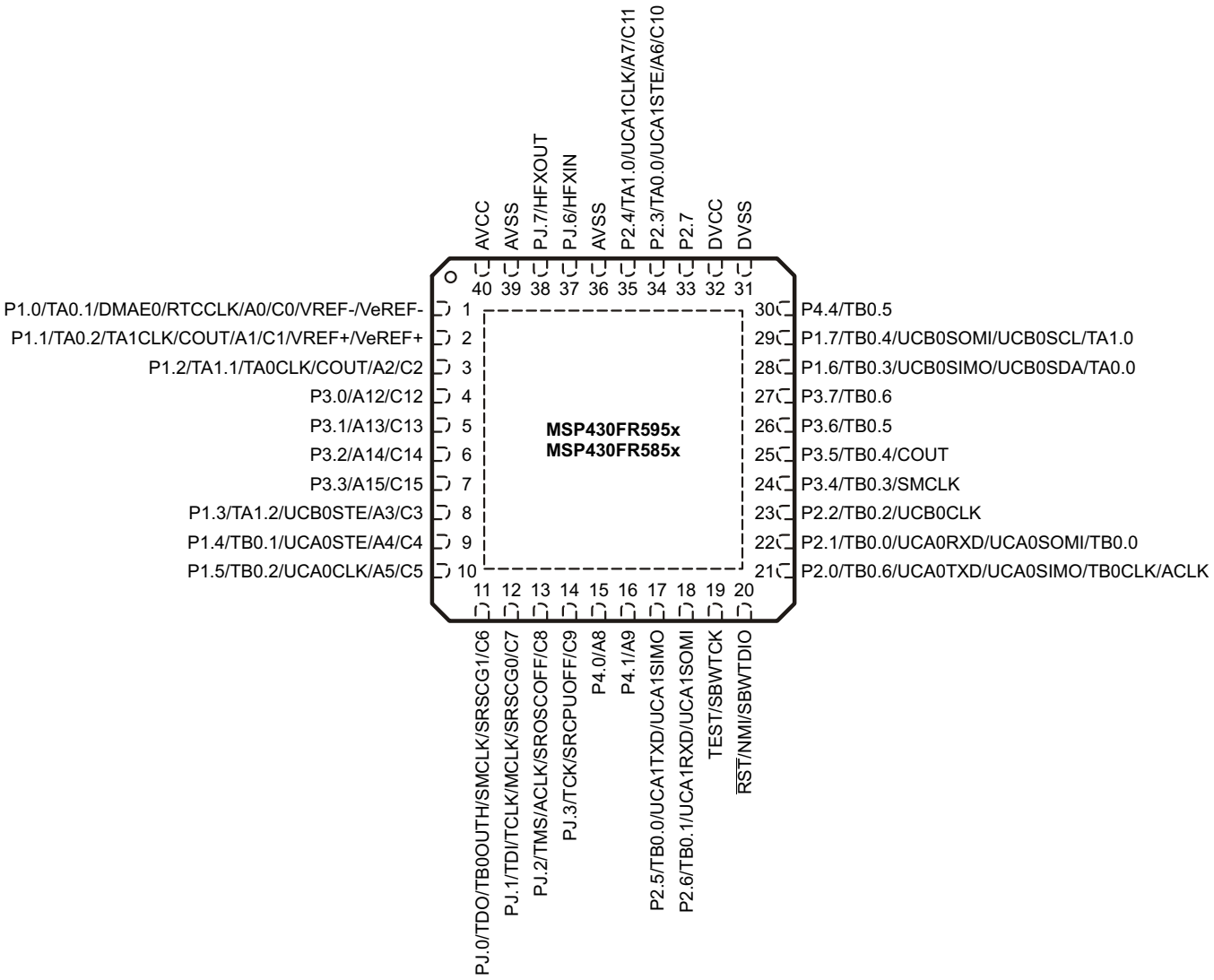
PRODUCT PREVIEW

Pin Designation, DA - MSP430FR594x and MSP430FR584x (LFXT Only)



PRODUCT PREVIEW

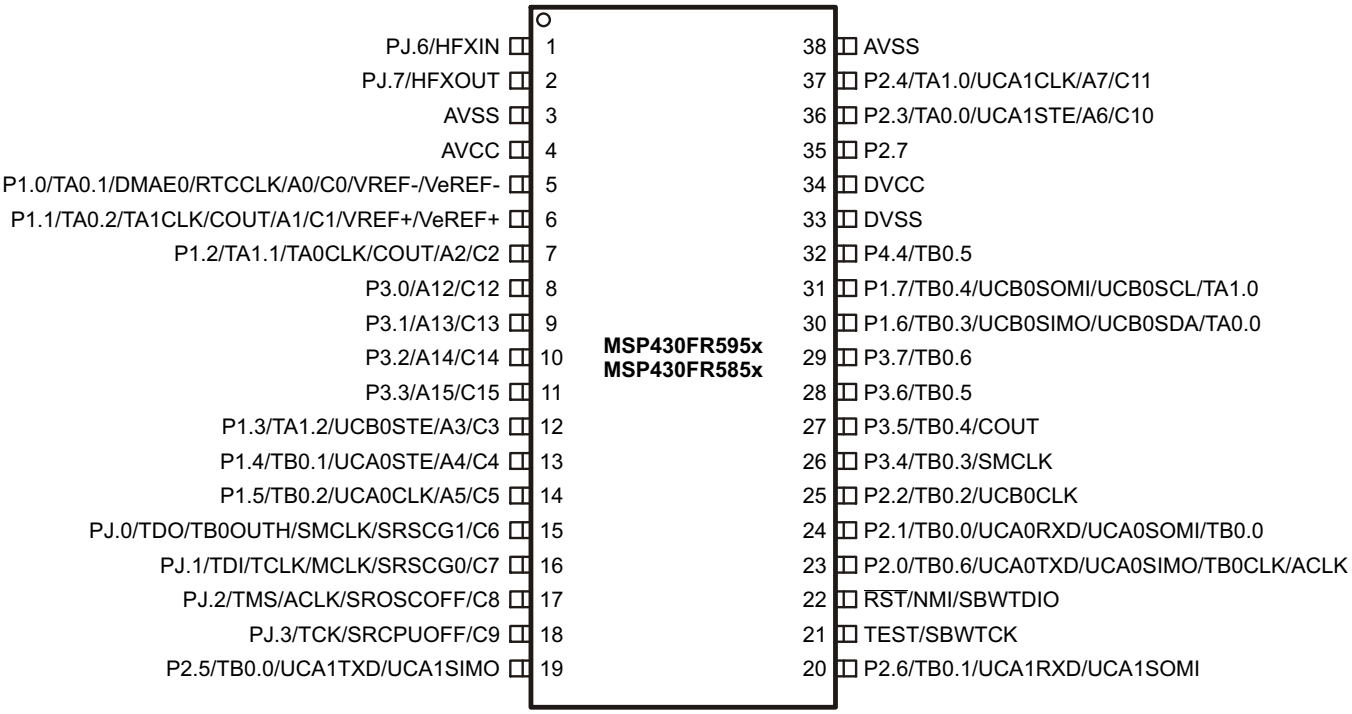
Pin Designation, RHA - MSP430FR595x and MSP430FR585x (HFXT Only)



NOTE: QFN package pad connection to V_{SS} recommended.

PRODUCT PREVIEW

Pin Designation, DA - MSP430FR595x and MSP430FR585x (HFXT Only)



PRODUCT PREVIEW

Table 4. Terminal Functions

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.[2]				
	RGZ	RHA	DA		
P1.0/TA0.1/DMAE0/ RTCCLK/A0/C0/VREF-/ VeREF-	1	1	5	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA0 CCR1 capture: CCI1A input, compare: Out1 External DMA trigger RTC clock calibration output Analog input A0 – ADC (not available on devices without ADC) Comparator input C0 Output of negative reference voltage (not available on devices without ADC) Input for an external negative reference voltage to the ADC (not available on devices without ADC)
P1.1/TA0.2/TA1CLK/ COUT/A1/C1/VREF+/ VeREF+	2	2	6	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA0 CCR2 capture: CCI2A input, compare: Out2 TA1 input clock Comparator output Analog input A1 – ADC (not available on devices without ADC) Comparator input C1 Output of positive reference voltage (not available on devices without ADC) Input for an external positive reference voltage to the ADC (not available on devices without ADC)
P1.2/TA1.1/TA0CLK/ COUT/A2/C2	3	3	7	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA1 CCR1 capture: CCI1A input, compare: Out1 TA0 input clock Comparator output Analog input A2 – ADC (not available on devices without ADC) Comparator input C2
P3.0/A12/C12	4	4	8	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A12 – ADC (not available on devices without ADC) Comparator input C12
P3.1/A13/C13	5	5	9	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A13 – ADC (not available on devices without ADC) Comparator input C13
P3.2/A14/C14	6	6	10	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A14 – ADC (not available on devices without ADC) Comparator input C14
P3.3/A15/C15	7	7	11	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A15 – ADC (not available on devices without ADC) Comparator input C15
P4.7	8	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
P1.3/TA1.2/UCB0STE/ A3/C3	9	8	12	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA1 CCR2 capture: CCI2A input, compare: Out2 Slave transmit enable – eUSCI_B0 SPI mode Analog input A3 – ADC (not available on devices without ADC) Comparator input C3

(1) I = input, O = output
(2) N/A = not available

Table 4. Terminal Functions (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.[2]				
	RGZ	RHA	DA		
P1.4/TB0.1/UCA0STE/ A4/C4	10	9	13	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR1 capture: CCI1A input, compare: Out1 Slave transmit enable – eUSCI_A0 SPI mode Analog input A4 – ADC (not available on devices without ADC) Comparator input C4
P1.5/TB0.2/UCA0CLK/ A5/C5	11	10	14	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR2 capture: CCI2A input, compare: Out2 Clock signal input – eUSCI_B0 SPI slave mode; Clock signal output – eUSCI_B0 SPI master mode Analog input A5 – ADC (not available on devices without ADC) Comparator input C5
PJ.0/TDO/TB0OUTH/ SMCLK/SRSCG1/C6	12	11	15	I/O	General-purpose digital I/O Test data output port Switch all PWM outputs high impedance input – TB0 SMCLK output **Low Power Debug:** CPU Status Register Bit SCG1 Comparator input C6
PJ.1/TDI/TCLK/MCLK/ SRSCG0/C7	13	12	16	I/O	General-purpose digital I/O Test data input or test clock input MCLK output **Low Power Debug:** CPU Status Register Bit SCG0 Comparator input C7
PJ.2/TMS/ACLK/ SROSCOFF/C8	14	13	17	I/O	General-purpose digital I/O Test mode select ACLK output **Low Power Debug:** CPU Status Register Bit OSCOFF Comparator input C8
PJ.3/TCK/SRCPUOFF/ C9	15	14	18	I/O	General-purpose digital I/O Test clock **Low Power Debug:** CPU Status Register Bit CPUOFF Comparator input C9
P4.0/A8	16	15	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A8 – ADC (not available on devices without ADC)
P4.1/A9	17	16	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A9 – ADC (not available on devices without ADC)
P4.2/A10	18	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A10 – ADC (not available on devices without ADC)
P4.3/A11	19	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A11 – ADC (not available on devices without ADC)
P2.5/TB0.0/UCA1TXD/ UCA1SIMO	20	17	19	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR0 capture: CCI0B input, compare: Out0 Transmit data – eUSCI_A1 UART mode Slave in, master out – eUSCI_A1 SPI mode

Table 4. Terminal Functions (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.[2]				
	RGZ	RHA	DA		
P2.6/TB0.1/UCA1RXD/ UCA1SOMI	21	18	20	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR1 compare: Out1 Receive data – eUSCI_A1 UART mode Slave out, master in – eUSCI_A1 SPI mode
TEST/SBWTCK	22	19	21	I	Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock
$\overline{\text{RST}}$/NMI/SBWTDIO	23	20	22	I/O	Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output
P2.0/TB0.6/UCA0TXD/ UCA0SIMO/TB0CLK/ ACLK	24	21	23	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR6 capture: CCI6B input, compare: Out6 Transmit data – eUSCI_A0 UART mode Slave in, master out – eUSCI_A0 SPI mode TB0 clock input ACLK output
P2.1/TB0.0/UCA0RXD/ UCA0SOMI/TB0.0	25	22	24	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR0 capture: CCI0A input, compare: Out0 Receive data – eUSCI_A0 UART mode Slave out, master in – eUSCI_A0 SPI mode TB0 CCR0 capture: CCI0A input, compare: Out0
P2.2/TB0.2/UCB0CLK	26	23	25	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR2 compare: Out2 Clock signal input – eUSCI_B0 SPI slave mode Clock signal output – eUSCI_B0 SPI master mode
P3.4/TB0.3/SMCLK	27	24	26	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR3 capture: CCI3A input, compare: Out3 SMCLK output
P3.5/TB0.4/COUT	28	25	27	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR4 capture: CCI4A input, compare: Out4 Comparator output
P3.6/TB0.5	29	26	28	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR5 capture: CCI5A input, compare: Out5
P3.7/TB0.6	30	27	29	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR6 capture: CCI6A input, compare: Out6
P1.6/TB0.3/UCB0SIMO/ UCB0SDA/TA0.0	31	28	30	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR3 capture: CCI3B input, compare: Out3 Slave in, master out – eUSCI_B0 SPI mode I2C data – eUSCI_B0 I2C mode TA0 CCR0 capture: CCI0A input, compare: Out0
P1.7/TB0.4/UCB0SOMI/ UCB0SCL/TA1.0	32	29	31	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR4 capture: CCI4B input, compare: Out4 Slave out, master in – eUSCI_B0 SPI mode I2C clock – eUSCI_B0 I2C mode TA1 CCR0 capture: CCI0A input, compare: Out0
P4.4/TB0.5	33	30	32	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0CCR5 capture: CCI5B input, compare: Out5

PRODUCT PREVIEW

Table 4. Terminal Functions (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.[2]				
	RGZ	RHA	DA		
P4.5	34	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
P4.6	35	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
DVSS	36	31	33		Digital ground supply
DVCC	37	32	34		Digital power supply
P2.7	38	33	35	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
P2.3/TA0.0/UCA1STE/ A6/C10	39	34	36	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA0 CCR0 capture: CCI0B input, compare: Out0 Slave transmit enable – eUSCI_A1 SPI mode Analog input A6 – ADC (not available on devices without ADC) Comparator input C10
P2.4/TA1.0/UCA1CLK/ A7/C11	40	35	37	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA1 CCR0 capture: CCI0B input, compare: Out0 Clock signal input – eUSCI_A1 SPI slave mode Clock signal output – eUSCI_A1 SPI master mode Analog input A7 – ADC (not available on devices without ADC) Comparator input C11
AVSS	41	36	38		Analog ground supply
PJ.6/HFXIN	42	37	1	I/O	General-purpose digital I/O Input for high-frequency crystal oscillator HFXT (in RHA and DA: MSP430FR595x and MSP430FR585x devices only)
PJ.7/HFXOUT	43	38	2	I/O	General-purpose digital I/O Output for high-frequency crystal oscillator HFXT (in RHA and DA: MSP430FR595x and MSP430FR585x devices only)
AVSS	44	N/A	N/A		Analog ground supply
PJ.4/LFXIN	45	37	1	I/O	General-purpose digital I/O Input for low-frequency crystal oscillator LFXT (in RHA and DA: MSP430FR594x and MSP430FR584x devices only)
PJ.5/LFXOUT	46	38	2	I/O	General-purpose digital I/O Output of low-frequency crystal oscillator LFXT (in RHA and DA: MSP430FR594x and MSP430FR584x devices only)
AVSS	47	39	3		Analog ground supply
AVCC	48	40	4		Analog power supply
QFN Pad	Pad	Pad	N/A		QFN package exposed thermal pad. Connection to V_{SS} is recommended.

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Operating Modes

The MSP430 has one active mode and seven software selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 through LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

Table 5. Operating Modes

Mode	AM		LPM0	LPM1	LPM2	LPM3	LPM4	LPM3.5	LPM4.5	
	Active	Active, FRAM Off(1)	CPU Off(2)	CPU Off	Standby	Standby	Off	RTC only	Shutdown with SVS	Shutdown without SVS
Maximum System Clock	16 MHz		16 MHz	16 MHz	50 kHz	50 kHz	0(3)	50 kHz	0(3)	
Typical Current Consumption, T_A = 25°C	100 µA/MHz					0.7 µA		0.5 µA		0.02 µA
Typical Wake-up Time	N/A		instant	6 µs	6 µs	7 µs	7 µs	250 µs	250 µs	1000 µs
Wake-Up Events	N/A		all	all	LF I/O Comp	LF I/O Comp	I/O Comp	RTC I/O	I/O	
CPU	**on**		off	off	off	off	off	reset	reset	
FRAM	**on**	off(1)	standby (or off(1))	off	off	off	off	off	off	
High-Frequency Peripherals	**available**		**available**	**available**	off	off	off	reset	reset	
Low-Frequency Peripherals	**available**		**available**	**available**	**available**	**available**(4)	off	RTC	reset	
Unclocked Peripherals(5)	**available**		**available**	**available**	**available**	**available**(4)	**available**(4)	reset	reset	
MCLK	**on**		**off**	off	off	off	off	off	off	
SMCLK	optional(6)		optional(6)	optional(6)	off	off	off	off	off	
ACLK	**on**		**on**	**on**	**on**	**on**	off	off	off	
Full Retention	**yes**		**yes**	**yes**	**yes**	**yes**	**yes**	no	no	
SVS	always		always	always	optional(7)	optional(7)	optional(7)	optional(7)	on(8)	off(9)
Brownout	**always**		**always**	**always**	**always**	**always**	**always**	**always**	**always**	

(1) FRAM disabled in FRAM controller
(2) Disabling the FRAM through the FRAM controller allows the application to lower the LPM current consumption but the wake-up time increases as soon as FRAM is accessed (for example, to fetch an interrupt vector). For a non-FRAM wake-up (for example, DMA transfer to RAM) the wake-up is not delayed.
(3) All clocks disabled
(4) See Peripherals in LPM3 and LPM4, which describes the use of peripherals in LPM3 and LPM4.
(5) "Unclocked peripherals" are peripherals that do not require a clock source to operate; for example, the comparator and REF, or the eUSCI when operated as an SPI slave.
(6) Controlled by SMCLKOFF.
(7) Activated SVS (SVSHE = 1) results in higher current consumption. SVS is not included in typical current consumption.
(8) SVSHE = 1
(9) SVSHE = 0

Peripherals in LPM3 and LPM4

Most peripherals can be activated to be operational in LPM3 if clocked by ACLK. Some modules are operational in LPM4, because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To limit the idle current adder, certain peripherals are group together. To achieve optimal current consumption, try to use modules within one group and try to limit the number of groups with active modules. The grouping is shown in Table 6. Modules not listed in this table are either already included in the standard LPM3 current consumption numbers or cannot be used in LPM3 or LPM4.

The idle current adder is negligible at room temperature (25°C) but can go up to TBD µA per group at high temperatures (85°C); see the electrical characteristics for details.

Table 6. Peripheral Groups

Group A	Group B
Timer TA1	Timer TA0
Timer TA2	Timer TA3
Timer TB0	Comparator
eUSCI_A0	ADC12_B
eUSCI_A1	REF_A
eUSCI_B0	

Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address and signatures are located in the address range 0FFFFh to 0FF80h. Table 7 summarizes the content of this address range.

The power-up start address or reset vector is located at 0FFFFh to 0FFFEh. It contains the 16-bit address pointing to the start address of the application program.

The interrupt vectors start at 0FFFDh extending to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as BSL password (if enabled by the corresponding signature).

The signatures are located at 0FF80h extending to higher addresses. Signatures are evaluated during device start-up. Starting from address 0FF88h extending to higher addresses a JTAG password can programmed. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password.

See the family user's guide chapter "System Resets, Interrupts, and Operating Modes, System Control Module (SYS)" for details.

Table 7. Interrupt Sources, Flags, Vectors, and Signatures

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up, Brownout, Supply Supervisor External Reset $\overline{RST}$ Watchdog Timeout (Watchdog mode) WDT, FRCTL MPU, CS, PMM Password Violation FRAM uncorrectable bit error detection MPU segment violation Software POR, BOR	SVSHIFG PMMRSTIFG WDTIFG WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW UBDIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG PMMPORIFG, PMMBORIFG (SYSRSTIV)(1) (2)	Reset	0FFFEh	highest
System NMI Vacant Memory Access JTAG Mailbox FRAM access time error FRAM bit error detection MPU segment violation	VMAIFG JMBNIFG, JMBOUTIFG ACCTEIFG CBDIFG, UBDIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG (SYSSNIV)(1) (3)	(Non)maskable	0FFFCh	
User NMI External NMI Oscillator Fault	NMIIFG, OFIFG (SYSUNIV)(1) (3)	(Non)maskable	0FFFAh	
Comparator_E	CEIFG, CEIIFG (CEIV)(1)	Maskable	0FFF8h	
TB0	TB0CCR0.CCIFG	Maskable	0FFF6h	
TB0	TB0CCR1.CCIFG ... TB0CCR6.CCIFG, TB0CTL.TBIFG (TB0IV)(1)	Maskable	0FFF4h	
Watchdog Timer (Interval Timer Mode)	WDTIFG	Maskable	0FFF2h	
eUSCI_A0 Receive or Transmit	UCA0IFG: UCRXIFG, UCTXIFG (SPI mode) UCA0IFG:UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA0IV)(1)	Maskable	0FFF0h	
eUSCI_B0 Receive or Transmit	UCB0IFG: UCRXIFG, UCTXIFG (SPI mode) UCB0IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I2C mode) (UCB0IV)(1)	Maskable	0FFEEh	
ADC12_B	ADC12IFG0 to ADC12IFG31 ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC21OVIFG, ADC12TOVIFG (ADC12IV)(1) (4)	Maskable	0FFECh	
TA0	TA0CCR0.CCIFG	Maskable	0FFEAh	
TA0	TA0CCR1.CCIFG, TA0CCR2.CCIFG, TA0CTL.TAIFG (TA0IV)(1)	Maskable	0FFE8h	
eUSCI_A1 Receive or Transmit	UCA1IFG: UCRXIFG, UCTXIFG (SPI mode) UCA1IFG: UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA1IV)(1)	Maskable	0FFE6h	
DMA	DMA0CTL.DMAIFG, DMA1CTL.DMAIFG, DMA2CTL.DMAIFG (DMAIV)(1)	Maskable	0FFE4h	
TA1	TA1CCR0.CCIFG	Maskable	0FFE2h	

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space
(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot disable it.
(4) Only on devices with ADC, otherwise reserved.

Table 7. Interrupt Sources, Flags, Vectors, and Signatures (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
TA1	TA1CCR1.CCIFG, TA1CCR2.CCIFG, TA1CTL.TAIFG (TA1IV)(1)	Maskable	0FFE0h	
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)	Maskable	0FFDEh	
TA2	TA2CCR0.CCIFG	Maskable	0FFDCh	
TA2	TA2CCR1.CCIFG TA2CTL.TAIFG (TA2IV)(1)	Maskable	0FFDAh	
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV)(1)	Maskable	0FFD8h	
TA3	TA3CCR0.CCIFG	Maskable	0FFD6h	
TA3	TA3CCR1.CCIFG TA3CTL.TAIFG (TA3IV)(1)	Maskable	0FFD4h	
I/O Port P3	P3IFG.0 to P3IFG.7 (P3IV)(1)	Maskable	0FFD2h	
I/O Port P4	P4IFG.0 to P4IFG.2 (P4IV)(5)	Maskable	0FFD0h	
RTC_B	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV)(5)	Maskable	0FFCEh	
AES (Reserved on MSP430FR58xx)	AESRDYIFG	Maskable	0FFCCh	lowest
Reserved	Reserved(6)		0FFCAh ⋮ 0FF8Ch	
Signatures(7)	IP Encapsulation Signature2(6)		0FF8Ah	
	IP Encapsulation Signature1(6)(8)		0FF88h	
	BSL Signature2		0FF86h	
	BSL Signature1		0FF84h	
	JTAG Signature2		0FF82h	
	JTAG Signature1		0FF80h	

(5) Multiple source flags
(6) May contain a JTAG password required to enable JTAG access to the device.
(7) Signatures are evaluated during device start-up. See the "System Resets, Interrupts, and Operating Modes, System Control Module (SYS)" chapter in the *MSP430FR59xx Family User's Guide* (SLAU367) for details.
(8) Must not contain 0AAAAh if used as JTAG password.

Memory Organization

Table 8. Memory Organization(1)

		MSP430FR59x9 MSP430FR58x9	MSP430FR59x8 MSP430FR58x8	MSP430FR59x7 MSP430FR58x7
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Total Size	63 KB 00FFFFh–00FF80h 013FFFh–004400h	47 KB 00FFFFh–00FF80h 00FF7Fh–004400h	32 KB 00FFFFh–00FF80h 00FF7Fh–008000h
RAM		2 KB 0023FFh–001C00h	2 KB 0023FFh–001C00h	1 KB 001FFFh–001C00h
Device Descriptor Info (TLV) (FRAM)		256 B 001AFFh–001A00h	256 B 001AFFh–001A00h	256 B 001AFFh–001A00h
Information memory (FRAM)	Info D	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h
	Info C	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h
	Info B	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info A	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootstrap loader (BSL) memory (ROM)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4 KB 000FFFh–0h	4 KB 000FFFh–0h	4 KB 000FFFh–0h

(1) All address space not listed is considered vacant memory.

PRODUCT PREVIEW

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory through the BSL is protected by an user-defined password. Use of the BSL requires four pins as shown in Table 9. BSL entry requires a specific entry sequence on the RST/NMI/SBWTDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 9. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
RST/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P2.0	Devices with UART BSL: Data transmit
P2.1	Devices with UART BSL: Data receive
VCC	Power supply
VSS	Ground supply

JTAG Operation

JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 10. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 10. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 11. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 11. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input and output
VCC		Power supply

Table 11. Spy-Bi-Wire Pin Requirements and Functions (continued)

DEVICE SIGNAL	DIRECTION	FUNCTION
VSS		Ground supply

FRAM Memory

The FRAM memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM memory include:

- Ultralow-power ultrafast-write nonvolatile memory
- Byte and word access capability
- Programmable and automated wait state generation
- Error correction coding (ECC)

Memory Protection Unit Including IP Encapsulation

The FRAM memory can be protected from inadvertent CPU execution, read access, or write access by the MPU. Features of the MPU include:

- IP encapsulation with programmable boundaries in steps of 1 KB (prevents reads from "outside"; for example, JTAG or non-IP software).
- Main memory partitioning programmable up to three segments in steps of 1 KB.
- Each segment's access rights can be individually selected (main and information memory).
- Access violation flags with interrupt capability for easy servicing of access violations.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430FR59xx Family User's Guide* (SLAU367).

Digital I/O

There are up to four 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wakeup input capability is available for all ports.
- Read and write access to port control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- CapSense functionality is supported on all pins of ports P1, P2, P3, P4, and PJ.

Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch crystal oscillator XT1 (LF), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2 (HF). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external low frequency (<50 kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal digitally-controlled oscillator DCO, a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.

Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary and core supplies.

Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

Real-Time Clock (RTC_B) (Only MSP430FR596x, MSP430FR594x, MSP430FR586x, and MSP430FR584x)

The RTC_B module contains an integrated real-time clock (RTC). It integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption.

Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart if a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Table 12. WDT_A Clocks

WDTSSELx	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	LFMODOSC

System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 13. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog timeout (PUC)	16h	

PRODUCT PREVIEW

Table 13. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		MPUPW MPU password violation (PUC)	22h	
		CSPW CS password violation (PUC)	24h	
		MPUSEGPIFG encapsulated IP memory segment violation (PUC)	26h	
		MPUSEGIIFG information memory segment violation (PUC)	28h	
		MPUSEG1IFG segment 1 memory violation (PUC)	2Ah	
		MPUSEG2IFG segment 2 memory violation (PUC)	2Ch	
		MPUSEG3IFG segment 3 memory violation (PUC)	2Eh	
		Reserved	30h	
		Reserved	32h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVS low-power reset entry	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		ACCTEIFG access time error	06h	
		MPUSEGPIFG encapsulated IP memory segment violation	08h	
		MPUSEGIIFG information memory segment violation	0Ah	
		MPUSEG1IFG segment 1 memory violation	0Ch	
		MPUSEG2IFG segment 2 memory violation	0Eh	
		MPUSEG3IFG segment 3 memory violation	10h	
		VMAIFG Vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIFG NMI pin	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 14. DMA Trigger Assignments(1)

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2 CCR0 CCIFG	TA2 CCR0 CCIFG	TA2 CCR0 CCIFG
6	TA3 CCR0 CCIFG	TA3 CCR0 CCIFG	TA3 CCR0 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	AES Trigger 0(2)	AES Trigger 0(2)	AES Trigger 0(2)
12	AES Trigger 1(2)	AES Trigger 1(2)	AES Trigger 1(2)
13	AES Trigger 2(2)	AES Trigger 2(2)	AES Trigger 2(2)
14	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
15	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
16	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
17	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
18	UCB0RXIFG0	UCB0RXIFG0	UCB0RXIFG0
19	UCB0TXIFG0	UCB0TXIFG0	UCB0TXIFG0
20	UCB0RXIFG1	UCB0RXIFG1	UCB0RXIFG1
21	UCB0TXIFG1	UCB0TXIFG1	UCB0TXIFG1
22	UCB0RXIFG2	UCB0RXIFG2	UCB0RXIFG2
23	UCB0TXIFG2	UCB0TXIFG2	UCB0TXIFG2
24	UCB0RXIFG3	UCB0RXIFG3	UCB0RXIFG3
25	UCB0TXIFG3	UCB0TXIFG3	UCB0TXIFG3
26	ADC12 end of conversion(3)	ADC12 end of conversion(3)	ADC12 end of conversion(3)
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) If a reserved trigger source is selected, no trigger is generated.
(2) Only on devices with AES Accelerator. Reserved on MSP430FR58xx devices without AES.
(3) Only on devices with ADC. Reserved on devices without ADC.

Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The eUSCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3 pin or 4 pin) and I2C.

Two eUSCI_A modules and one eUSCI_B module are implemented.

TA0, TA1

TA0 and TA1 are 16-bit timers and counters (Timer_A type) with three capture/compare registers each. Each can support multiple captures or compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 15. TA0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.2	TA0CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.2	$\overline{\text{TA0CLK}}$	INCLK				
P1.6	TA0.0	CCI0A	CCR0	TA0	TA0.0	P1.6
P2.3	TA0.0	CCI0B				P2.3
	DVSS	GND				
	DVCC	V_{CC}				
P1.0	TA0.1	CCI1A	CCR1	TA1	TA0.1	P1.0
	COUT (internal)	CCI1B				ADC12(internal)(1) ADC12SHSx = {1}
	DVSS	GND				
	DVCC	V_{CC}				
P1.1	TA0.2	CCI2A	CCR2	TA2	TA0.2	P1.1
	ACLK (internal)	CCI2B				
	DVSS	GND				
	DVCC	V_{CC}				

(1) Only on devices with ADC.

Table 16. TA1 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.1	TA1CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.1	$\overline{\text{TA0CLK}}$	INCLK				
P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	P1.7
P2.4	TA1.0	CCI0B				P2.4
	DVSS	GND				
	DVCC	V_{CC}				
P1.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	P1.2
	COUT (internal)	CCI1B				ADC12(internal)(1) ADC12SHSx = {4}
	DVSS	GND				
	DVCC	V_{CC}				
P1.3	TA1.2	CCI2A	CCR2	TA2	TA1.2	P1.3
	ACLK (internal)	CCI2B				
	DVSS	GND				
	DVCC	V_{CC}				

(1) Only on devices with ADC.

PRODUCT PREVIEW

TA2, TA3

TA2 and TA3 are 16-bit timers and counters (Timer_A type) with two capture/compare registers each and with internal connections only. Each can support multiple captures or compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 17. TA2 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From CapSenseIO0 (internal)	INCLK			
TA3 CCR0 output (internal)	CCI0A	CCR0	TA0	TA3 CCI0A input
ACLK (internal)	CCI0B			
DVSS	GND			
DVCC	V_{CC}			
From CapSenseIO0 (internal)	CCI1A	CCR1	TA1	ADC12(internal)(1) ADC12SHSx = {5}
COUT (internal)	CCI1B			
DVSS	GND			
DVCC	V_{CC}			

(1) Only on devices with ADC

Table 18. TA3 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From CapSenseIO1 (internal)	INCLK			
TA2 CCR0 output (internal)	CCI0A	CCR0	TA0	TA2 CCI0A input
ACLK (internal)	CCI0B			
DVSS	GND			
DVCC	V_{CC}			
From CapSenseIO1 (internal)	CCI1A	CCR1	TA1	ADC12(internal)(1) ADC12SHSx = {6}
COUT (internal)	CCI1B			
DVSS	GND			
DVCC	V_{CC}			

(1) Only on devices with ADC

TB0

TB0 is a 16-bit timer and counter (Timer_B type) with seven capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 19. TB0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.0	TB0CLK	TBCLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.0	$\overline{\text{TB0CLK}}$	INCLK				
P2.1	TB0.0	CCI0A	CCR0	TB0	TB0.0	P2.1
P2.5	TB0.0	CCI0B				P2.5
	DVSS	GND				ADC12 (internal)(1) ADC12SHSx = {2}
	DVCC	V_{CC}				
P1.4	TB0.1	CCI1A	CCR1	TB1	TB0.1	P1.4
	COUT (internal)	CCI1B				P2.6
	DVSS	GND				ADC12 (internal)(1) ADC12SHSx = {3}
	DVCC	V_{CC}				
P1.5	TB0.2	CCI2A	CCR2	TB2	TB0.2	P1.5
	ACLK (internal)	CCI2B				P2.2
	DVSS	GND				
	DVCC	V_{CC}				
P3.4	TB0.3	CCI3A	CCR3	TB3	TB0.3	P3.4
P1.6	TB0.3	CCI3B				P1.6
	DVSS	GND				
	DVCC	V_{CC}				
P3.5	TB0.4	CCI4A	CCR4	TB4	TB0.4	P3.5
P1.7	TB0.4	CCI4B				P1.7
	DVSS	GND				
	DVCC	V_{CC}				
P3.6	TB0.5	CCI5A	CCR5	TB5	TB0.5	P3.6
P4.4	TB0.5	CCI5B				P4.4
	DVSS	GND				
	DVCC	V_{CC}				
P3.7	TB0.6	CCI6A	CCR6	TB6	TB0.6	P3.7
P2.0	TB0.6	CCI6B				P2.0
	DVSS	GND				
	DVCC	V_{CC}				

(1) Only on devices with ADC.

ADC12_B

The ADC12_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with a lower and upper limit allows CPU-independent result monitoring with three window comparator interrupt flags.

The external trigger sources available are summarized in Table 20.

The available multiplexing between internal and external analog inputs is listed in Table 21.

Table 20. ADC12_B Trigger Signal Connections

ADC12SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC12SC)
001	1	TA0 CCR1 output
010	2	TB0 CCR0 output
011	3	TB0 CCR1 output
100	4	TA1 CCR1 output
101	5	TA2 CCR1 output
110	6	TA3 CCR1 output
111	7	Reserved (DVSS)

Table 21. ADC12_B External and Internal Signal Mapping

CONTROL BIT	EXTERNAL (CONTROL BIT = 0)	INTERNAL (CONTROL BIT = 1)
ADC12BATMAP	A31	Battery Monitor
ADC12TCMAP	A30	Temperature Sensor
ADC12CH0MAP	A29	N/A(1)
ADC12CH1MAP	A28	N/A(1)
ADC12CH2MAP	A27	N/A(1)
ADC12CH3MAP	A26	N/A(1)

(1) N/A = No internal signal is available on this device.

Comparator_E

The primary function of the Comparator_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

AES256 Accelerator (Only MSP430FR59xx)

The AES accelerator module performs encryption and decryption of 128-bit data with 128-bit, 192-bit, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

True Random Seed (Only MSP430FR59xx)

The Device Descriptor Information (TLV) section contains a 128-bit true random seed that can be used to implement a Deterministic Random Number Generator.

Shared Reference (REF)

The REF module is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

Embedded Emulation Module (EEM)

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The S version of the EEM implemented on all devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

Peripheral File Map

Table 22. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 23)	0100h	000h-01Fh
PMM (see Table 24)	0120h	000h-01Fh
FRAM Control (see Table 25)	0140h	000h-00Fh
CRC16 (see Table 26)	0150h	000h-007h
Watchdog (see Table 27)	015Ch	000h-001h
CS (see Table 28)	0160h	000h-00Fh
SYS (see Table 29)	0180h	000h-01Fh
Shared Reference (see Table 30)	01B0h	000h-001h
Port P1, P2 (see Table 31)	0200h	000h-01Fh
Port P3, P4 (see Table 32)	0220h	000h-01Fh
Port PJ (see Table 33)	0320h	000h-01Fh
TA0 (see Table 34)	0340h	000h-02Fh
TA1 (see Table 35)	0380h	000h-02Fh
TB0 (see Table 36)	03C0h	000h-02Fh
TA2 (see Table 37)	0400h	000h-02Fh
CapSenseIO0 (see Table 38)	0430h	000h-00Fh
TA3 (see Table 39)	0440h	000h-02Fh
CapSenseIO1 (see Table 40)	0470h	000h-00Fh
Real-Time Clock (RTC_B) (see Table 41)	04A0h	000h-01Fh
32-Bit Hardware Multiplier (see Table 42)	04C0h	000h-02Fh
DMA General Control (see Table 43)	0500h	000h-00Fh
DMA Channel 0 (see Table 43)	0510h	000h-00Fh
DMA Channel 1 (see Table 43)	0520h	000h-00Fh
DMA Channel 2 (see Table 43)	0530h	000h-00Fh
MPU Control (see Table 44)	05A0h	000h-00Fh
eUSCI_A0 (see Table 45)	05C0h	000h-01Fh
eUSCI_A1 (see Table 46)	05E0h	000h-01Fh
eUSCI_B0 (see Table 47)	0640h	000h-02Fh
ADC12_B (see Table 48)	0800h	000h-09Fh
Comparator_E (see Table 49)	08C0h	000h-00Fh
AES (see Table 50)	09C0h	000h-00Fh

Table 23. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 24. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM interrupt flags	PMMIFG	0Ah
PM5 Control 0	PM5CTL0	10h

Table 25. FRAM Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTLCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

Table 26. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 27. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 28. CS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch

Table 29. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch

Table 29. SYS Registers (Base Address: 0180h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Reset vector generator	SYSRSTIV	1Eh

Table 30. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 31. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 32. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 selection 0	P3SEL0	0Ah
Port P3 selection 1	P3SEL1	0Ch
Port P3 interrupt vector word	P3IV	0Eh
Port P3 complement selection	P3SELC	16h
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h

Table 32. Port P3, P4 Registers (Base Address: 0220h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh
Port P4 selection 1	P4SEL1	0Dh
Port P4 complement selection	P4SELC	17h
Port P4 interrupt vector word	P4IV	1Eh
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

Table 33. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ selection 0	PJSEL0	0Ah
Port PJ selection 1	PJSEL1	0Ch
Port PJ complement selection	PJSELC	16h

Table 34. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 35. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h

Table 35. TA1 Registers (Base Address: 0380h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 interrupt vector	TA1IV	2Eh

Table 36. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 register	TB0R	10h
Capture/compare register 0	TB0CCR0	12h
Capture/compare register 1	TB0CCR1	14h
Capture/compare register 2	TB0CCR2	16h
Capture/compare register 3	TB0CCR3	18h
Capture/compare register 4	TB0CCR4	1Ah
Capture/compare register 5	TB0CCR5	1Ch
Capture/compare register 6	TB0CCR6	1Eh
TB0 expansion register 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 37. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
TA2 register	TA2R	10h
Capture/compare register 0	TA2CCR0	12h
Capture/compare register 1	TA2CCR1	14h
TA2 expansion register 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 38. CapSenseIO0 Registers (Base Address: 0430h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CapSenseIO 0 control	CAPSIO0CTL	0Eh

Table 39. TA3 Registers (Base Address: 0440h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA3 control	TA3CTL	00h
Capture/compare control 0	TA3CCTL0	02h
Capture/compare control 1	TA3CCTL1	04h
TA3 register	TA3R	10h
Capture/compare register 0	TA3CCR0	12h
Capture/compare register 1	TA3CCR1	14h
TA3 expansion register 0	TA3EX0	20h

Table 39. TA3 Registers (Base Address: 0440h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA3 interrupt vector	TA3IV	2Eh

Table 40. CapSenseIO1 Registers (Base Address: 0470h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CapSenseIO 1 control	CAPSIO1CTL	0Eh

Table 41. RTC_B Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds	RTCSEC/RTCNT1	10h
RTC minutes	RTCMIN/RTCNT2	11h
RTC hours	RTCHOUR/RTCNT3	12h
RTC day of week	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh
Binary-to-BCD conversion register	BIN2BCD	1Ch
BCD-to-binary conversion register	BCD2BIN	1Eh

Table 42. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h

Table 42. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

Table 43. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

Table 44. MPU Control Registers (Base Address: 05A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
MPU control 0	MPUCTL0	00h
MPU control 1	MPUCTL1	02h
MPU Segmentation Boarder 2	MPUSEGB2	04h
MPU Segmentation Boarder 1	MPUSEGB1	06h
MPU access management	MPUSAM	08h
MPU IP control 0	MPUIPC0	0Ah

Table 44. MPU Control Registers (Base Address: 05A0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
MPU IP Encapsulation Segment Boarder 2	MPUIPSEGB2	0Ch
MPU IP Encapsulation Segment Boarder 1	MPUIPSEGB1	0Eh

Table 45. eUSCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI _A control word 1	UCA0CTLW1	02h
eUSCI_A baud rate 0	UCA0BR0	06h
eUSCI_A baud rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status word	UCA0STATW	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	UCA0IRTCTL	12h
eUSCI_A IrDA receive control	UCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

Table 46. eUSCI_A1 Registers (Base Address:05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA1CTLW0	00h
eUSCI _A control word 1	UCA1CTLW1	02h
eUSCI_A baud rate 0	UCA1BR0	06h
eUSCI_A baud rate 1	UCA1BR1	07h
eUSCI_A modulation control	UCA1MCTLW	08h
eUSCI_A status word	UCA1STATW	0Ah
eUSCI_A receive buffer	UCA1RXBUF	0Ch
eUSCI_A transmit buffer	UCA1TXBUF	0Eh
eUSCI_A LIN control	UCA1ABCTL	10h
eUSCI_A IrDA transmit control	UCA1IRTCTL	12h
eUSCI_A IrDA receive control	UCA1IRRCTL	13h
eUSCI_A interrupt enable	UCA1IE	1Ah
eUSCI_A interrupt flags	UCA1IFG	1Ch
eUSCI_A interrupt vector word	UCA1IV	1Eh

Table 47. eUSCI_B0 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh

Table 47. eUSCI_B0 Registers (Base Address: 0640h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B received address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI I2C slave address	UCB0I2CSA	20h
eUSCI interrupt enable	UCB0IE	2Ah
eUSCI interrupt flags	UCB0IFG	2Ch
eUSCI interrupt vector word	UCB0IV	2Eh

Table 48. ADC12_B Registers (Base Address: 0800h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B Control 0	ADC12CTL0	00h
ADC12_B Control 1	ADC12CTL1	02h
ADC12_B Control 2	ADC12CTL2	04h
ADC12_B Control 3	ADC12CTL3	06h
ADC12_B Window Comparator Low Threshold Register	ADC12LO	08h
ADC12_B Window Comparator High Threshold Register	ADC12HI	0Ah
ADC12_B Interrupt Flag Register 0	ADC12IFGR0	0Ch
ADC12_B Interrupt Flag Register 1	ADC12IFGR1	0Eh
ADC12_B Interrupt Flag Register 2	ADC12IFGR2	10h
ADC12_B Interrupt Enable Register 0	ADC12IER0	12h
ADC12_B Interrupt Enable Register 1	ADC12IER1	14h
ADC12_B Interrupt Enable Register 2	ADC12IER2	16h
ADC12_B Interrupt Vector	ADC12IV	18h
ADC12_B Memory Control 0	ADC12MCTL0	20h
ADC12_B Memory Control 1	ADC12MCTL1	22h
ADC12_B Memory Control 2	ADC12MCTL2	24h
ADC12_B Memory Control 3	ADC12MCTL3	26h
ADC12_B Memory Control 4	ADC12MCTL4	28h
ADC12_B Memory Control 5	ADC12MCTL5	2Ah
ADC12_B Memory Control 6	ADC12MCTL6	2Ch
ADC12_B Memory Control 7	ADC12MCTL7	2Eh
ADC12_B Memory Control 8	ADC12MCTL8	30h
ADC12_B Memory Control 9	ADC12MCTL9	32h
ADC12_B Memory Control 10	ADC12MCTL10	34h
ADC12_B Memory Control 11	ADC12MCTL11	36h
ADC12_B Memory Control 12	ADC12MCTL12	38h
ADC12_B Memory Control 13	ADC12MCTL13	3Ah
ADC12_B Memory Control 14	ADC12MCTL14	3Ch
ADC12_B Memory Control 15	ADC12MCTL15	3Eh
ADC12_B Memory Control 16	ADC12MCTL16	40h
ADC12_B Memory Control 17	ADC12MCTL17	42h
ADC12_B Memory Control 18	ADC12MCTL18	44h
ADC12_B Memory Control 19	ADC12MCTL19	46h
ADC12_B Memory Control 20	ADC12MCTL20	48h

Table 48. ADC12_B Registers (Base Address: 0800h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B Memory Control 21	ADC12MCTL21	4Ah
ADC12_B Memory Control 22	ADC12MCTL22	4Ch
ADC12_B Memory Control 23	ADC12MCTL23	4Eh
ADC12_B Memory Control 24	ADC12MCTL24	50h
ADC12_B Memory Control 25	ADC12MCTL25	52h
ADC12_B Memory Control 26	ADC12MCTL26	54h
ADC12_B Memory Control 27	ADC12MCTL27	56h
ADC12_B Memory Control 28	ADC12MCTL28	58h
ADC12_B Memory Control 29	ADC12MCTL29	5Ah
ADC12_B Memory Control 30	ADC12MCTL30	5Ch
ADC12_B Memory Control 31	ADC12MCTL31	5Eh
ADC12_B Memory 0	ADC12MEM0	60h
ADC12_B Memory 1	ADC12MEM1	62h
ADC12_B Memory 2	ADC12MEM2	64h
ADC12_B Memory 3	ADC12MEM3	66h
ADC12_B Memory 4	ADC12MEM4	68h
ADC12_B Memory 5	ADC12MEM5	6Ah
ADC12_B Memory 6	ADC12MEM6	6Ch
ADC12_B Memory 7	ADC12MEM7	6Eh
ADC12_B Memory 8	ADC12MEM8	70h
ADC12_B Memory 9	ADC12MEM9	72h
ADC12_B Memory 10	ADC12MEM10	74h
ADC12_B Memory 11	ADC12MEM11	76h
ADC12_B Memory 12	ADC12MEM12	78h
ADC12_B Memory 13	ADC12MEM13	7Ah
ADC12_B Memory 14	ADC12MEM14	7Ch
ADC12_B Memory 15	ADC12MEM15	7Eh
ADC12_B Memory 16	ADC12MEM16	80h
ADC12_B Memory 17	ADC12MEM17	82h
ADC12_B Memory 18	ADC12MEM18	84h
ADC12_B Memory 19	ADC12MEM19	86h
ADC12_B Memory 20	ADC12MEM20	88h
ADC12_B Memory 21	ADC12MEM21	8Ah
ADC12_B Memory 22	ADC12MEM22	8Ch
ADC12_B Memory 23	ADC12MEM23	8Eh
ADC12_B Memory 24	ADC12MEM24	90h
ADC12_B Memory 25	ADC12MEM25	92h
ADC12_B Memory 26	ADC12MEM26	94h
ADC12_B Memory 27	ADC12MEM27	96h
ADC12_B Memory 28	ADC12MEM28	98h
ADC12_B Memory 29	ADC12MEM29	9Ah
ADC12_B Memory 30	ADC12MEM30	9Ch
ADC12_B Memory 31	ADC12MEM31	9Eh

Table 49. Comparator_E Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator_E control register 0	CECTL0	00h
Comparator_E control register 1	CECTL1	02h
Comparator_E control register 2	CECTL2	04h
Comparator_E control register 3	CECTL3	06h
Comparator_E interrupt register	CEINT	0Ch
Comparator_E interrupt vector word	CEIV	0Eh

Table 50. AES Accelerator Registers (Base Address: 09C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
AES accelerator control register 0	AESACTL0	00h
Reserved		02h
AES accelerator status register	AESASTAT	04h
AES accelerator key register	AESAKEY	06h
AES accelerator data in register	AESADIN	008h
AES accelerator data out register	AESADOUT	00Ah
AES accelerator XORed data in register	AESAXDIN	00Ch
AES accelerator XORed data in register (no trigger)	AESAXIN	00Eh

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

Voltage applied at DVCC and AVCC pins to V_{SS}	–0.3 V to 4.1 V
Voltage applied to any pin(2)	–0.3 V to (V_{CC} + 0.3 V), 4.1 V Max
Diode current at any device pin	±2 mA
Storage temperature range, T_{stg} (3)	-55°C to 125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
The devices can retain programmed information in all sections of memory following exposure to solder reflow temperatures. However a yield drop in the order of <200 DPPM can be expected. It is recommended to account for this DPPM at the time of production testing and exercise caution when programming the device prior to reflow.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins(1)(2)(3)		1.8(4)		3.6	
V_{SS}	Supply voltage applied at all DVSS and AVSS pins			0		V
T_A	Operating free-air temperature		–40	25	85	°C
C_{DVCC}	Recommended capacitor at DVCC(5)			1		µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(6)	No FRAM wait states (NWAITSx = 0)	0		8	MHz
		With FRAM wait states (NWAITSx = 1)(7)	0		16(8)	
f_{ACLK}	Maximum ACLK frequency				50	kHz
f_{SMCLK}	Maximum SMCLK frequency				16(8)	MHz

(1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
(2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. The circuitry is less sensitive for rising than for falling supply voltage changes. For rising voltages, the slope must be greater than approximately 5 V/µs to cause a BOR reset; for falling voltages, the slope must be less than approximately -0.05 V/µs. Following the datasheet recommendation the capacitor C_{DVCC} should limit the slopes accordingly.
(3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(4) The minimum supply voltage is defined by the SVS levels.
(5) A decoupling capacitor for each supply pin pair (DVCC and DVSS, AVCC and AVSS) is required. Place a low-ESR ceramic capacitor of 100 nF (minimum) as close as possible to the respective pin pairs (within a few millimeters).
(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(7) Wait states only occur on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always executed without wait states.
(8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

Low-Frequency Crystal Oscillator, LFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFXT}	LFXT oscillator crystal frequency	LFXTBYPASS = 0		32768		Hz
$f_{LFXT,SW}$	LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 (1) (2)	10.5	32.768	50	kHz
$C_{L,eff}$	Integrated effective load capacitance (3) (4)			1		pF

(1) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-Trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT, SW}$.
(2) Maximum frequency of operation of the entire device cannot be exceeded.
(3) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
(4) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 3.7 pF, 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF. Because the PCB adds additional capacitance, it must be considered as part of the total capacitance.

High-Frequency Crystal Oscillator, HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{HFXT}	HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 1 (1) (2)	4		8	MHz
		HFXTBYPASS = 0, HFFREQ = 2 (2)	8.01		16	
		HFXTBYPASS = 0, HFFREQ = 3 (2)	16.01		24	
$f_{HFXT,SW}$	HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1, HFFREQ = 0 (3) (2)	0.9		4	MHz
		HFXTBYPASS = 1, HFFREQ = 1 (3) (2)	4.01		8	
		HFXTBYPASS = 1, HFFREQ = 2 (3) (2)	8.01		16	
		HFXTBYPASS = 1, HFFREQ = 3 (3) (2)	16.01		24	
$C_{L,eff}$	Integrated effective load capacitance (4) (5)			1		pF

(1) HFFREQ = {0} is not supported for HFXT crystal mode of operation.
(2) Maximum frequency of operation of the entire device cannot be exceeded.
(3) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-Trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{HFXT, SW}$.
(4) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the oscillator frequency via MCLK or SMCLK. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(5) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF.

DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{DCO1}	DCO frequency range 1 MHz, trimmed	Measured at SMCLK, DCORSEL = 0, DCOFSEL = 0, DCORSEL = 1, DCOFSEL = 0			1		MHz
$f_{DCO2.7}$	DCO frequency range 2.7 MHz, trimmed	Measured at SMCLK, DCORSEL = 0, DCOFSEL = 1			2.667		MHz
$f_{DCO3.5}$	DCO frequency range 3.5 MHz, trimmed	Measured at SMCLK, DCORSEL = 0, DCOFSEL = 2			3.5		MHz
f_{DCO4}	DCO frequency range 4 MHz, trimmed	Measured at SMCLK, DCORSEL = 0, DCOFSEL = 3			4		MHz
$f_{DCO5.3}$	DCO frequency range 5.3 MHz, trimmed	Measured at SMCLK, DCORSEL = 0, DCOFSEL = 4, DCORSEL = 1, DCOFSEL = 1			5.333		MHz
f_{DCO7}	DCO frequency range 7 MHz, trimmed	Measured at SMCLK, DCORSEL = 0, DCOFSEL = 5, DCORSEL = 1, DCOFSEL = 2			7		MHz
f_{DCO8}	DCO frequency range 8 MHz, trimmed	Measured at SMCLK, DCORSEL = 0, DCOFSEL = 6, DCORSEL = 1, DCOFSEL = 3			8		MHz
f_{DCO16}	DCO frequency range 16 MHz, trimmed	Measured at SMCLK, DCORSEL = 1, DCOFSEL = 4			16		MHz
f_{DCO21}	DCO frequency range 21 MHz, trimmed	Measured at SMCLK, DCORSEL = 1, DCOFSEL = 5			21		MHz
f_{DCO24}	DCO frequency range 24 MHz, trimmed	Measured at SMCLK, DCORSEL = 1, DCOFSEL = 6			24		MHz

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK			9		kHz

Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{MODOSC}	MODOSC frequency			4.4	5	5.6	MHz

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ± 10%	2.2 V, 3.0 V			16	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ± 10%	2.2 V, 3.0 V			16	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, Minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

12-Bit ADC

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{(Ax)}$	Analog input voltage range(1)	All ADC12 analog input pins Ax	0		AVCC	V
	Resolution	No missing codes		12		bits
	Data rate				200	ksps
$f_{ADC12OSC}$	Internal oscillator(2)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODOSC	4.4	5.0	5.6	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODOSC	2.5		3.2	µs

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The ADC12OSC is sourced directly from MODOSC inside the UCS.

REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = 1	2.7 V		2.5		V
		REFVSEL = {1} for 2.0 V, REFON = 1	2.2 V		2.0		
		REFVSEL = {0} for 1.2 V, REFON = 1	1.8 V		1.2		
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
t_{SETTLE}	Settling time of reference voltage(1)	$AV_{CC} = AV_{CC\ (min)} - AV_{CC(max)}$ REFVSEL = {0, 1, 2}, REFON = 0 → 1			75		µs

(1) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

PRODUCT PREVIEW

Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage level	CERSx = 11, CEREFLx = 01, CEREFACC = 0	1.8 V		1.2		V
		CERSx = 11, CEREFLx = 10, CEREFACC = 0	2.2 V		2.0		V
		CERSx = 11, CEREFLx = 11, CEREFACC = 0	2.7 V		2.5		V
		CERSx = 11, CEREFLx = 01, CEREFACC = 1	1.8 V		1.2		V
		CERSx = 11, CEREFLx = 10, CEREFACC = 1	2.2 V		2.0		V
		CERSx = 11, CEREFLx = 11, CEREFACC = 1	2.7 V		2.5		V
V_{IC}	Common mode input range			0		V_{CC}-1	V
V_{CE_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31			VIN × (n+1) / 32		V

FRAM Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

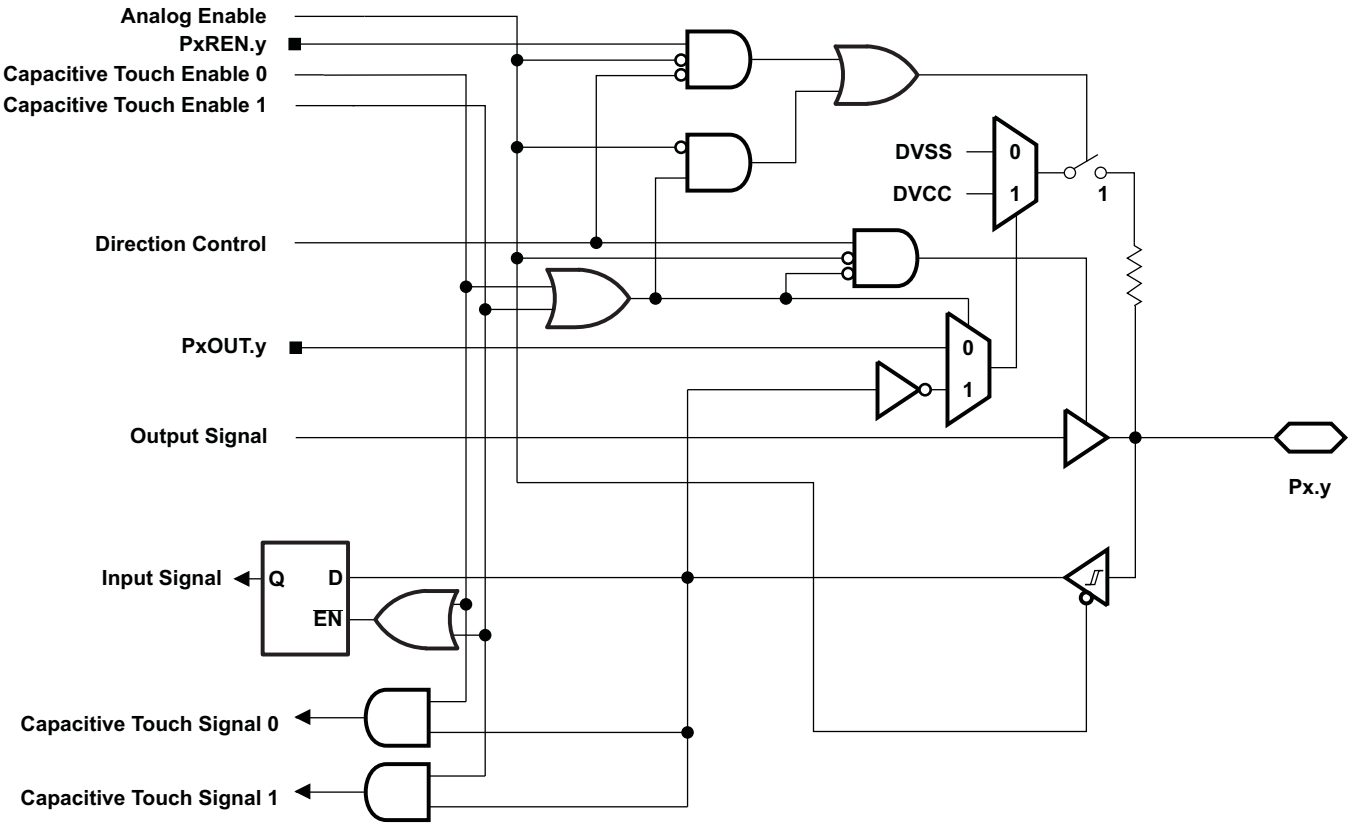
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Read and write endurance		10^{15}			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
		T_J = 70°C	40			
		T_J = 85°C	10			

PRODUCT PREVIEW

INPUT/OUTPUT SCHEMATICS

CapSenseIO Functionality Ports P1, P2, P3, P4, and PJ

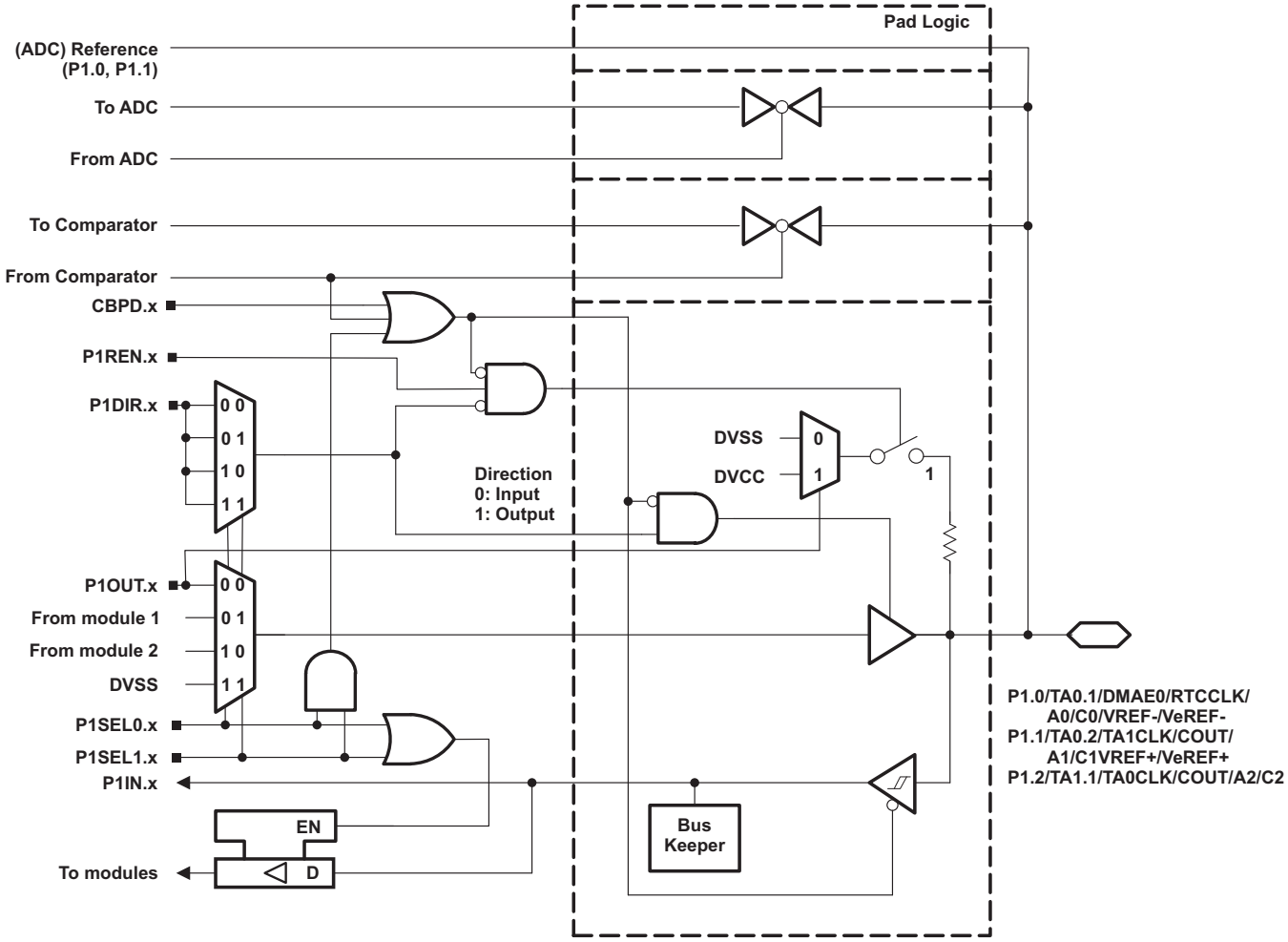
All port pins provide the CapSenseIO functionality as shown in the following figure. The CapSenseIO functionality is controlled using the CapSenseIO control registers CAPSIO0CTL and CAPSIO1CTL as described in the *MSP430FR59xx Family User's Guide* (SLAU367). The CapSenseIO functionality is not shown in the individual pin schematics in the following sections.



NOTE: Functional representation only.

PRODUCT PREVIEW

Port P1, P1.0 to P1.2, Input/Output With Schmitt Trigger



NOTE: Functional representation only.

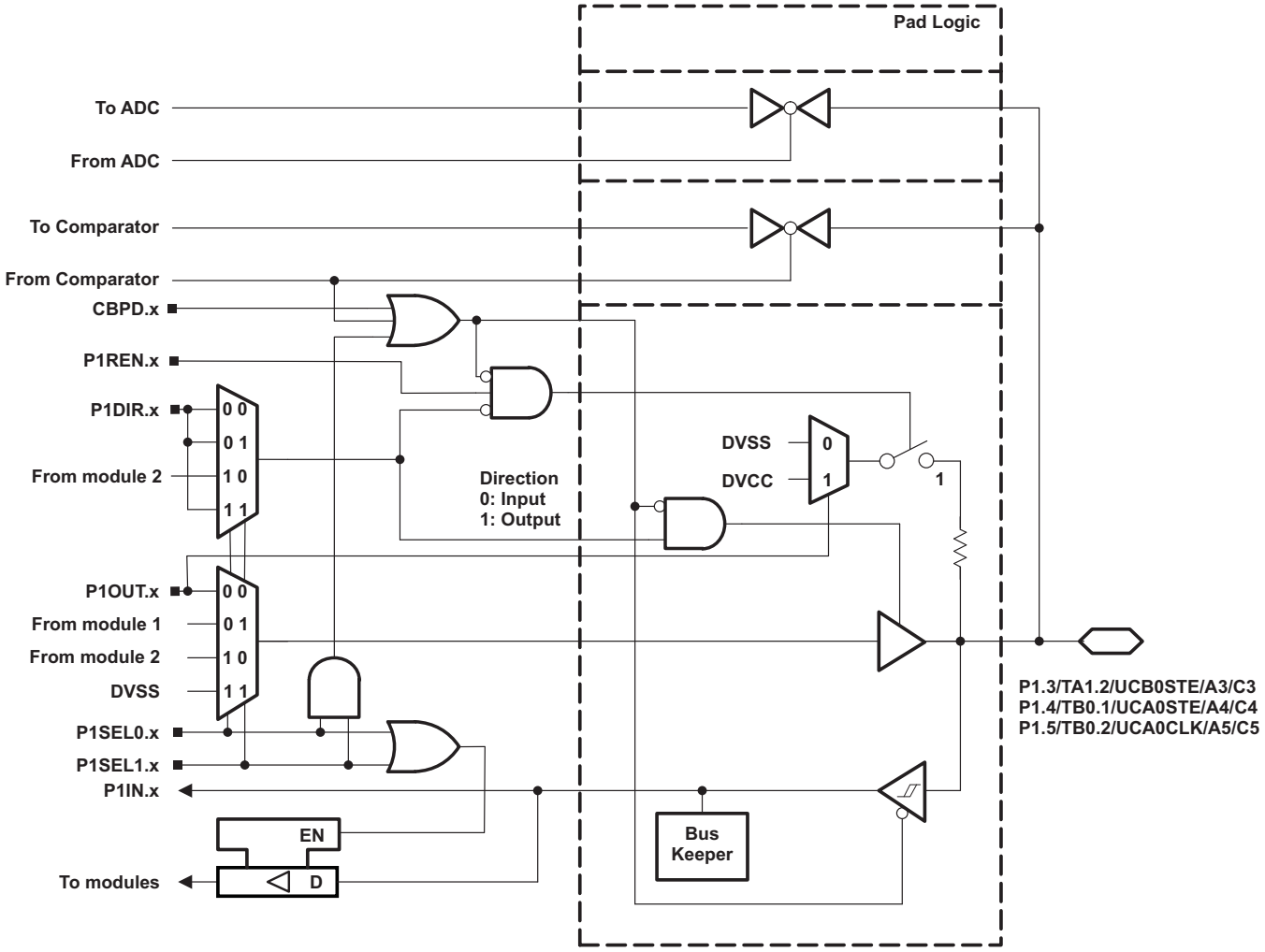
PRODUCT PREVIEW

Table 51. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/ VREF-/VeREF-	0	P1.0 (I/O)	I: 0; O: 1	0	0
		TA0.CCI1A	0	0	1
		TA0.1	1		
		DMAE0	0	1	0
		RTCCLK	1		
		A0, C0, VREF-, VeREF-(2)(3)	X	1	1
P1.1/TA0.2/TA1CLK/COUT/A1/C1/ VREF+/VeREF+	1	P1.1 (I/O)	I: 0; O: 1	0	0
		TA0.CCI2A	0	0	1
		TA0.2	1		
		TA1CLK	0	1	0
		COUT	1		
		A1, C1, VREF+, VeREF+(2)(3)	X	1	1
P1.2/TA1.1/TA0CLK/COUT/A2/C2	2	P1.2 (I/O)	I: 0; O: 1	0	0
		TA1.CCI1A	0	0	1
		TA1.1	1		
		TA0CLK	0	1	0
		COUT	1		
		A2, C2(2)(3)	X	1	1

(1) X = Don't care
(2) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.

Port P1, P1.3 to P1.5, Input/Output With Schmitt Trigger



NOTE: Functional representation only.

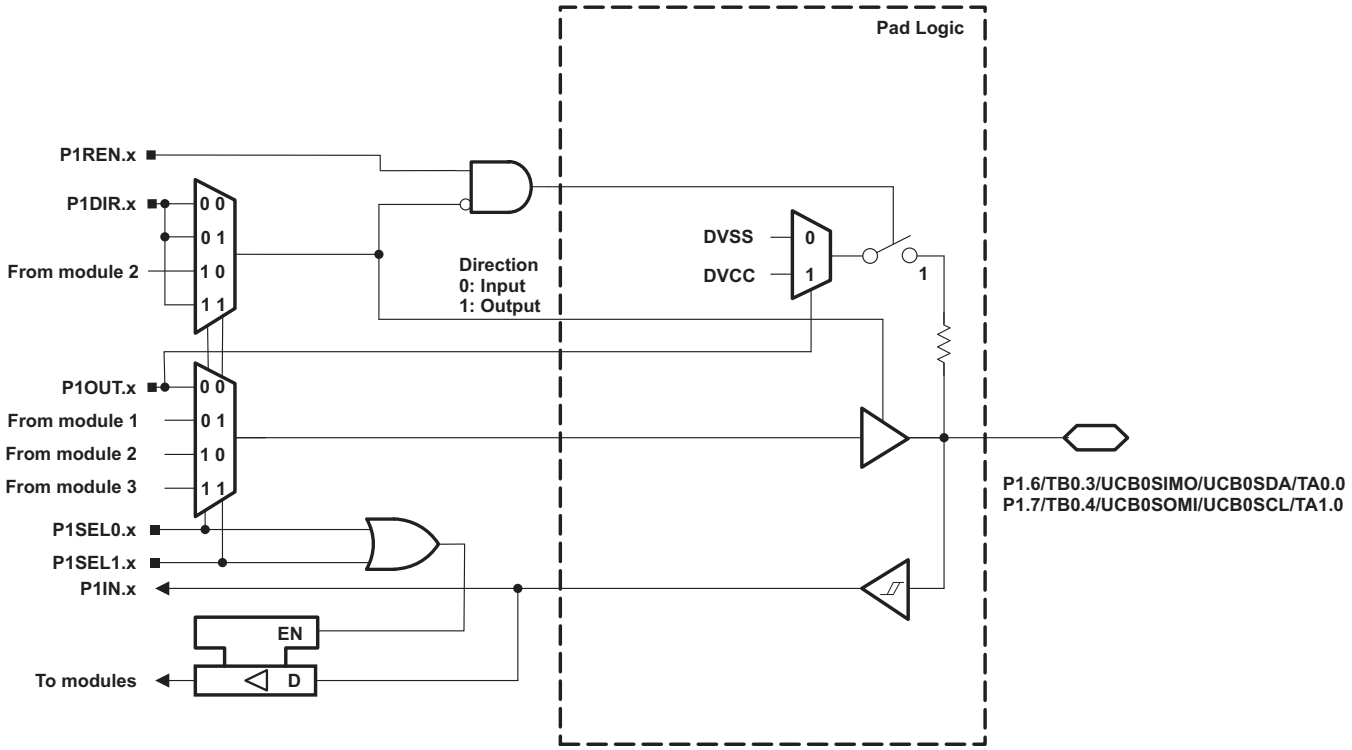
PRODUCT PREVIEW

Table 52. Port P1 (P1.3 to P1.5) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.3/TA1.2/UCB0STE/A3/C3	3	P1.3 (I/O)	I: 0; O: 1	0	0
		TA1.CCI2A	0	0	1
		TA1.2	1		
		UCB0STE	X(2)	1	0
		A3, C3(3)(4)	X	1	1
P1.4/TB0.1/UCA0STE/A4/C4	4	P1.4 (I/O)	I: 0; O: 1	0	0
		TB0.CCI1A	0	0	1
		TB0.1	1		
		UCA0STE	X(5)	1	0
		A4, C4(3)(4)	X	1	1
P1.5/TB0.2/UCA0CLK/A5/C5	5	P1.5(I/O)	I: 0; O: 1	0	0
		TB0.CCI2A	0	0	1
		TB0.2	1		
		UCA0CLK	X(5)	1	0
		A5, C5(3)(4)	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B0 module.
(3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.
(5) Direction controlled by eUSCI_A0 module.

Port P1, P1.6 to P1.7, Input/Output With Schmitt Trigger



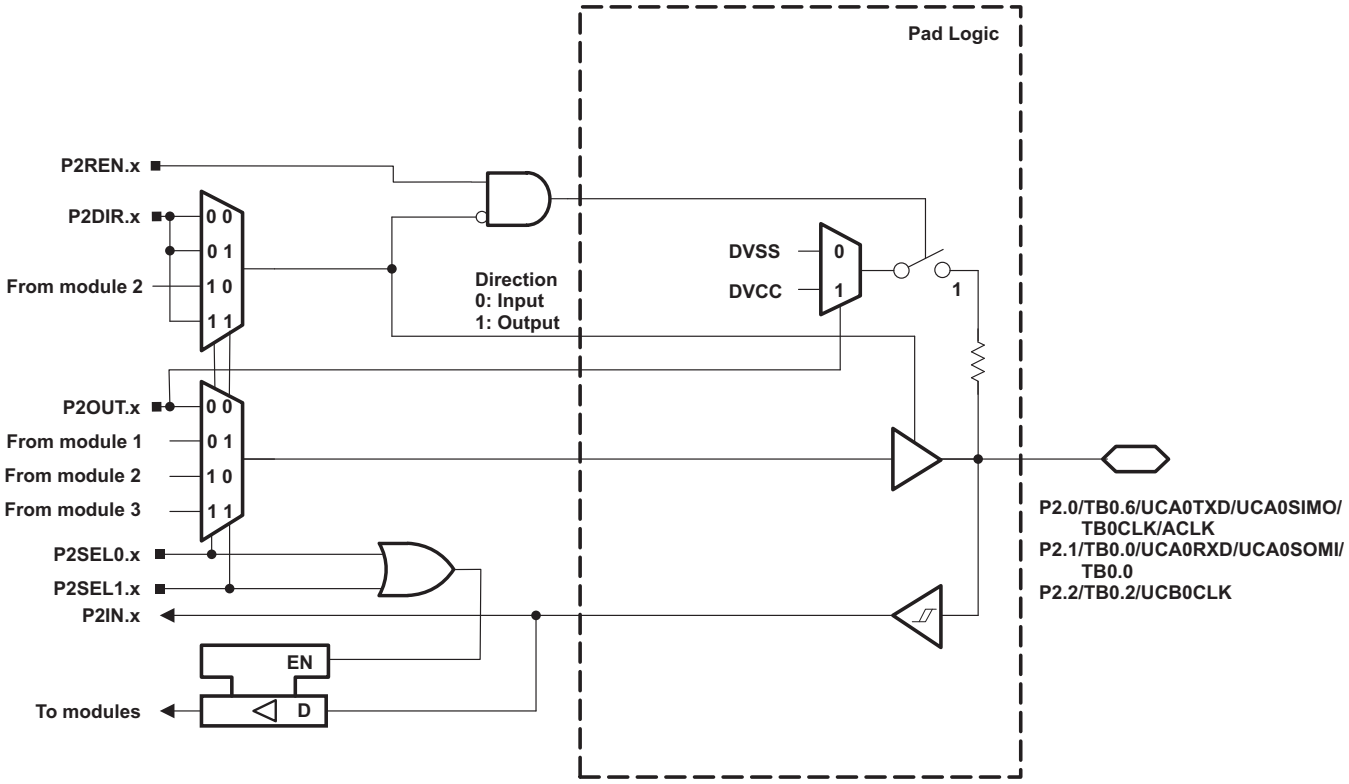
NOTE: Functional representation only.

Table 53. Port P1 (P1.6 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.6/TB0.3/UCB0SIMO/UCB0SDA/ TA0.0	6	P1.6 (I/O)	I: 0; O: 1	0	0
		TB0.CCI3B	0	0	1
		TB0.3	1		
		UCB0SIMO/UCB0SDA	X(2)	1	0
		TA0.CCI0A	0	1	1
		TA0.0	1		
P1.7/TB0.4/UCB0SOMI/UCB0SCL/ TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0	0
		TB0.CCI4B	0	0	1
		TB0.4	1		
		UCB0SOMI/UCB0SCL	X(3)	1	0
		TA1.CCI0A	0	1	1
		TA1.0	1		

(1) X = Don't care
(2) Direction controlled by eUSCI_B0 module.
(3) Direction controlled by eUSCI_A0 module.

Port P2, P2.0 to P2.2, Input/Output With Schmitt Trigger



NOTE: Functional representation only.

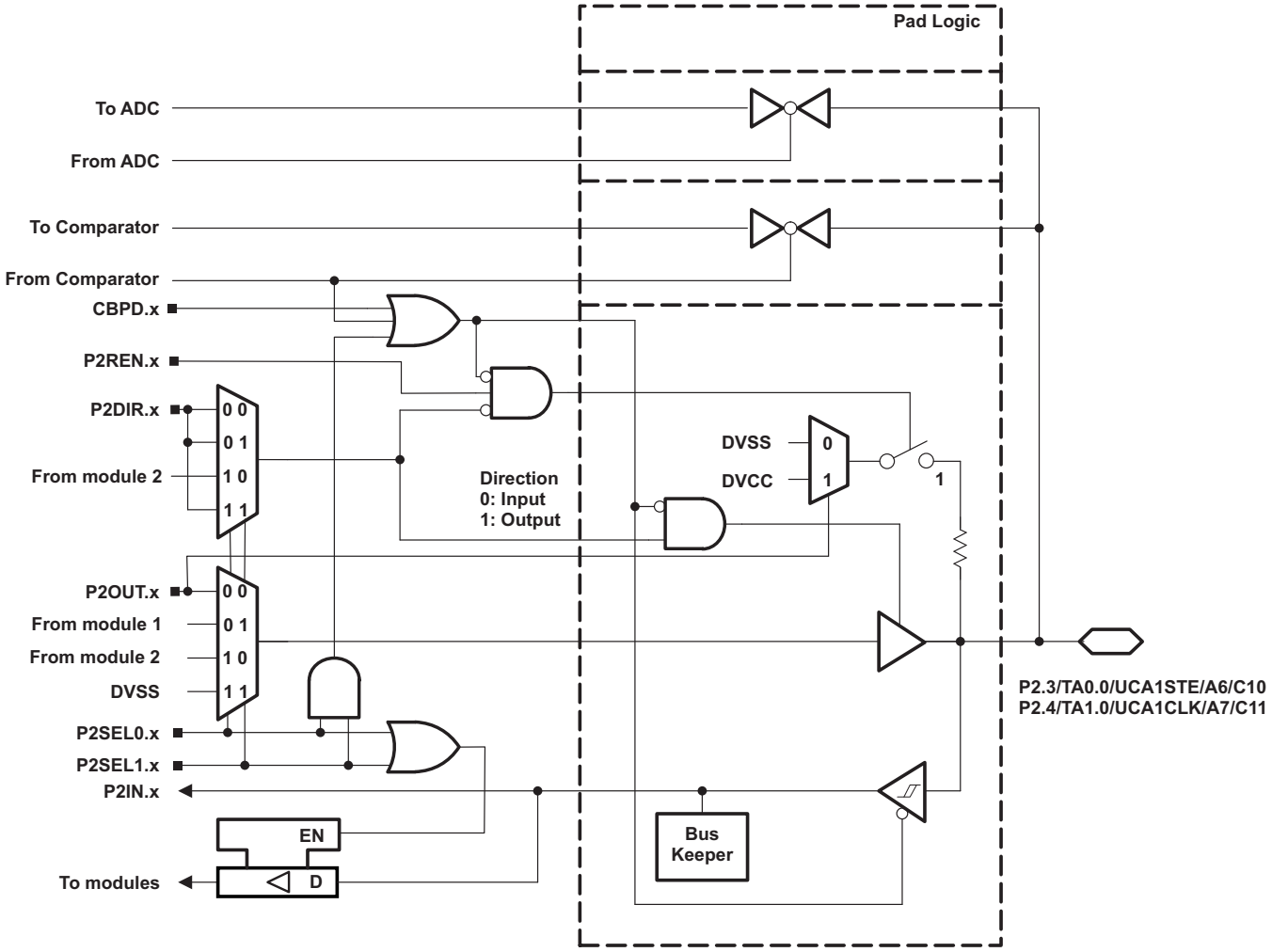
Table 54. Port P2 (P2.0 to P2.2) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.0/TB0.6/UCA0TXD/UCA0SIMO/ TB0CLK/ACLK	0	P2.0 (I/O)	I: 0; O: 1	0	0
		TB0.CCI6B	0	0	1
		TB0.6	1		
		UCA0TXD/UCA0SIMO	X(2)	1	0
		TB0CLK	0	1	1
		ACLK	1		
P2.1/TB0.0/UCA0RXD/UCA0SOMI/ TB0.0	1	P2.1 (I/O)	I: 0; O: 1	0	0
		TB0.CCI0A	0	X	1
		TB0.0	1		
		UCA0RXD/UCA0SOMI	X(2)	1	0
P2.2/TB0.2/UCB0CLK	2	P2.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		TB0.2	1		
		UCB0CLK	X (3)	1	0
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care
(2) Direction controlled by eUSCI_A0 module.
(3) Direction controlled by eUSCI_B0 module.

PRODUCT PREVIEW

Port P2, P2.3 to P2.4, Input/Output With Schmitt Trigger



NOTE: Functional representation only.

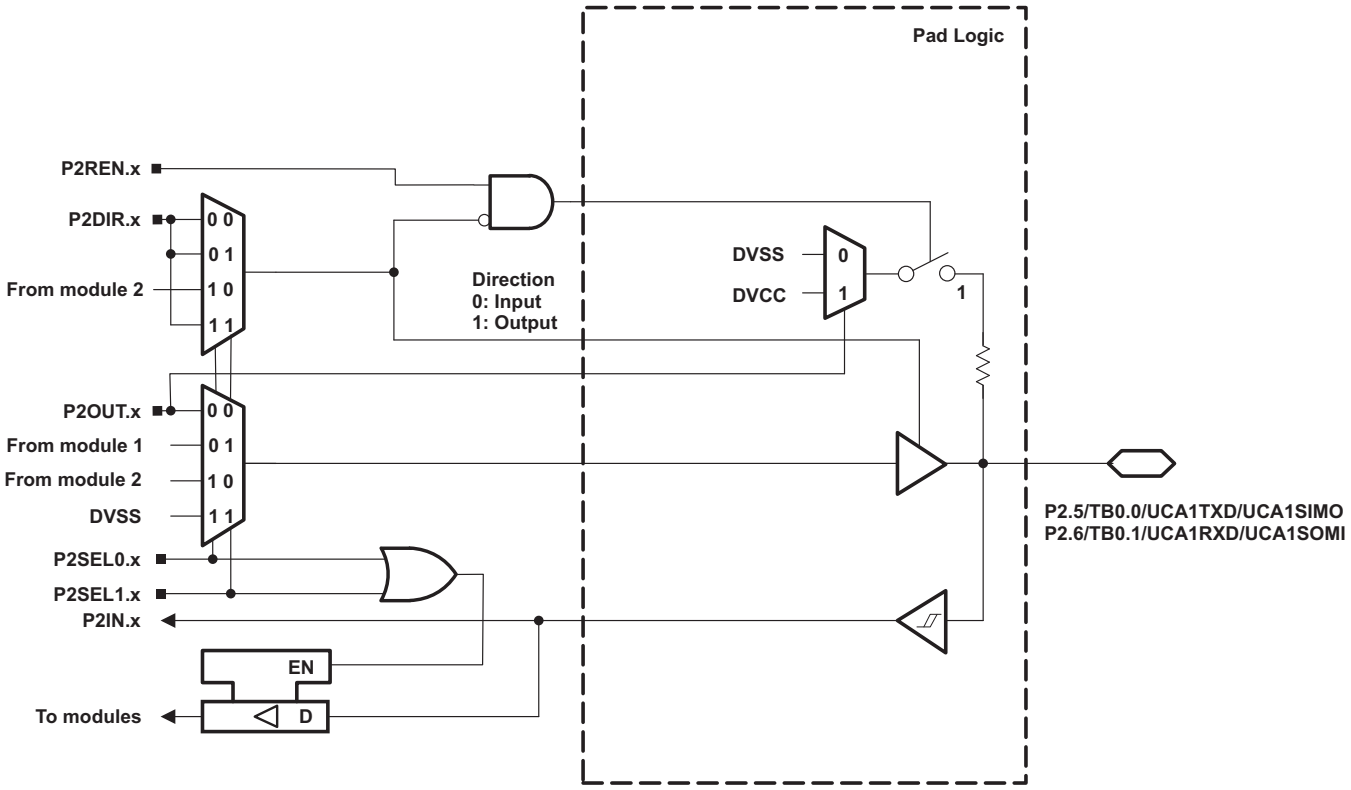
PRODUCT PREVIEW

Table 55. Port P2 (P2.3 to P2.4) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.3/TA0.0/UCA1STE/A6/C10	3	P2.3 (I/O)	I: 0; O: 1	0	0
		TA0.CCI0B	0	0	1
		TA0.0	1		
		UCA1STE	X (2)	1	0
		A6, C10(3)(4)	X	1	1
P2.4/TA1.0/UCA1CLK/A7/C11	4	P2.4 (I/O)	I: 0; O: 1	0	0
		TA1.CCI0B	0	0	1
		TA1.0	1		
		UCA1CLK	X (2)	1	0
		A7, C11(3)(4)	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.

Port P2, P2.5 to P2.6, Input/Output With Schmitt Trigger



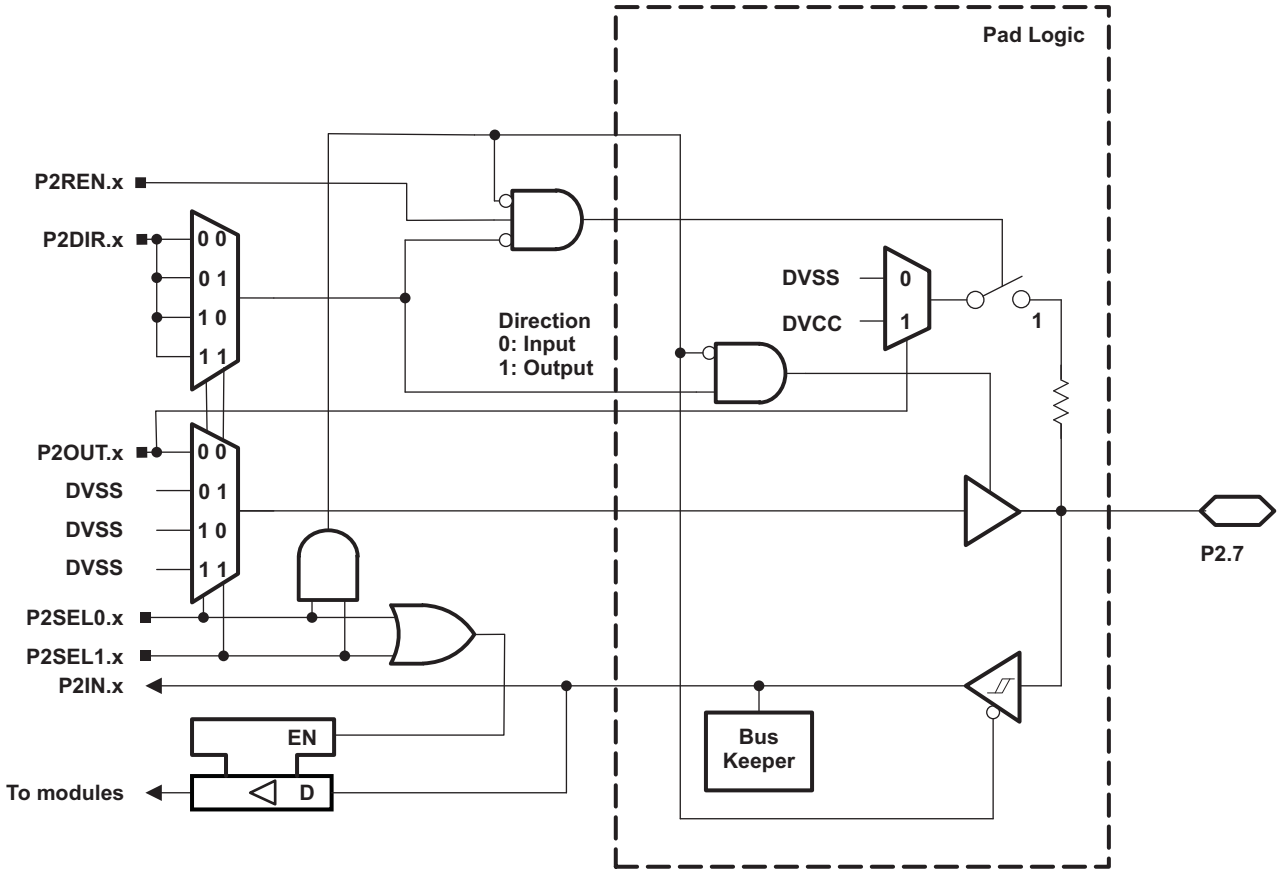
NOTE: Functional representation only.

Table 56. Port P2 (P2.5 to P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.5/TB0.0/UCA1TXD/UCA1SIMO	5	P2.5(I/O)	I: 0; O: 1	0	0
		TB0.CCI0B	0	0	1
		TB0.0	1		
		UCA1TXD/UCA1SIMO	X[2]	1	0
		N/A	0	1	1
		Internally tied to DVSS	1		
P2.6/TB0.1/UCA1RXD/UCA1SOMI	6	P2.6(I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		TB0.1	1		
		UCA1RXD/UCA1SOMI	X[2]	1	0
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.

Port P2, P2.7, Input/Output With Schmitt Trigger



NOTE: Functional representation only.

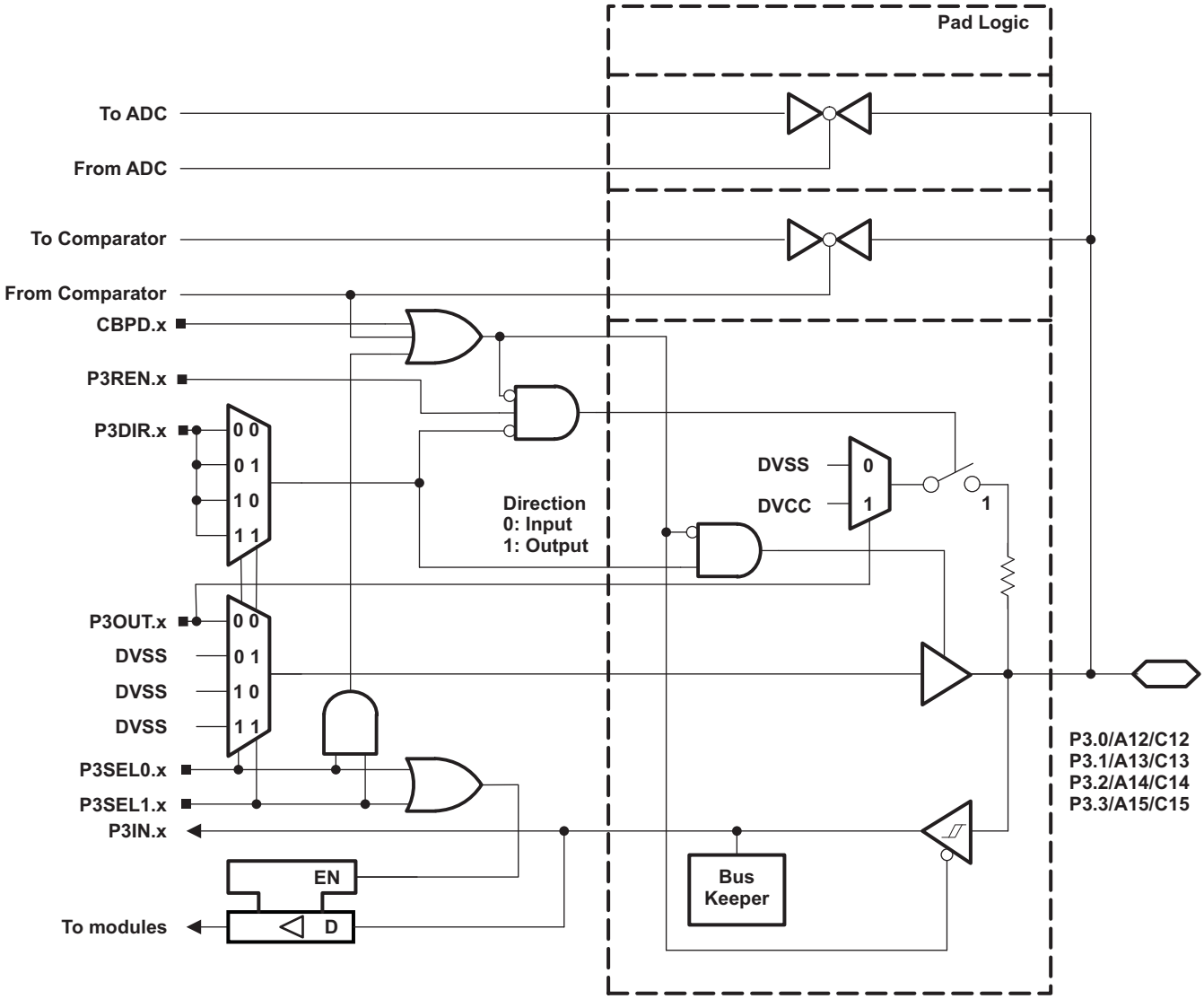
Table 57. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.7	7	P2.7(I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	X
		Internally tied to DVSS	1		

(1) X = Don't care

PRODUCT PREVIEW

Port P3, P3.0 to P3.3, Input/Output With Schmitt Trigger



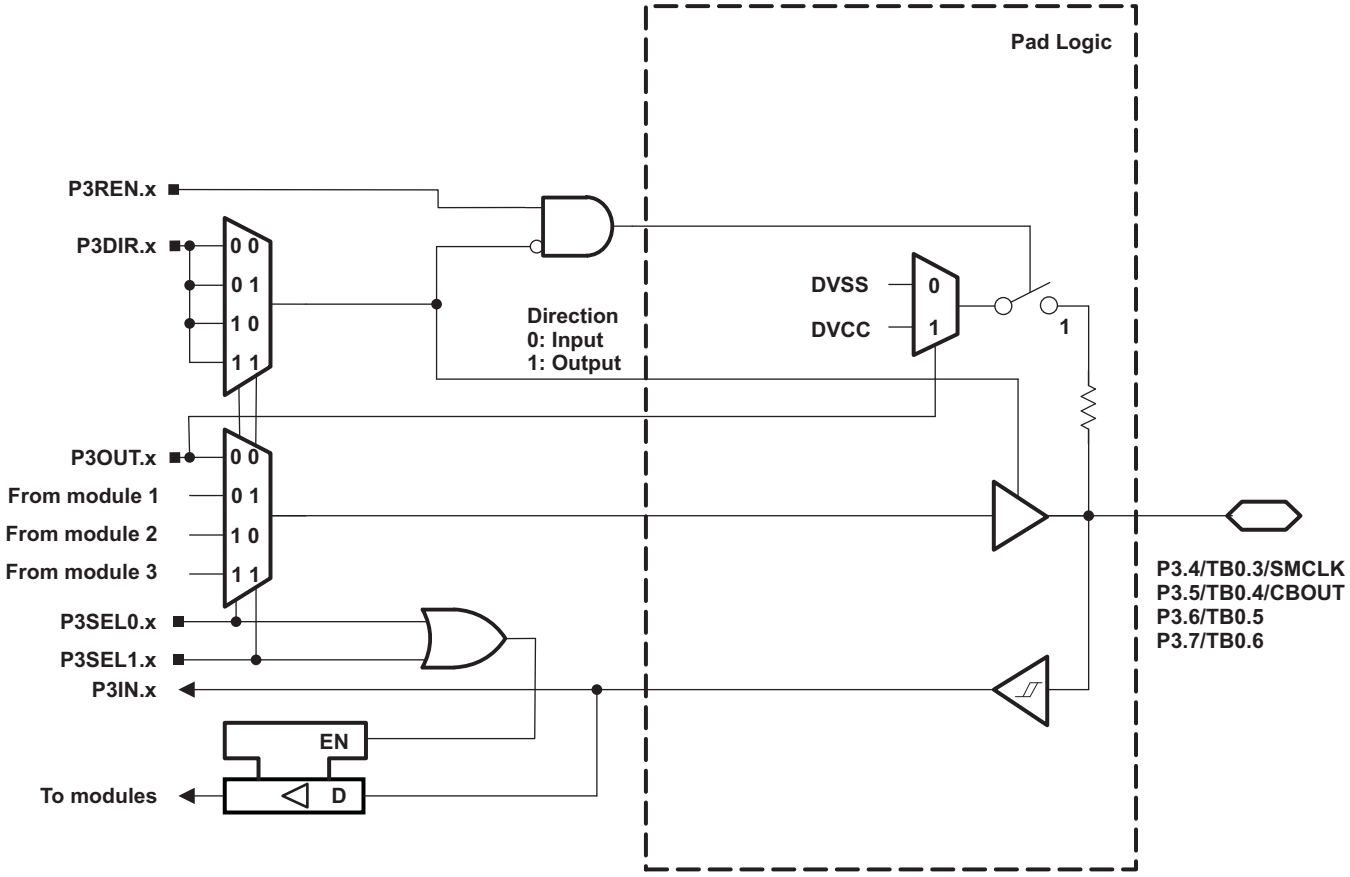
NOTE: Functional representation only.

Table 58. Port P3 (P3.0 to P3.3) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.0/A12/C12	0	P3.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A12/C12(2)(3)	X	1	1
P3.1/A13/C13	1	P3.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A13/C13(2)(3)	X	1	1
P3.2/A14/C14	2	P3.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A14/C14(2)(3)	X	1	1
P3.3/A15/C15	3	P3.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A15/C15(2)(3)	X	1	1

(1) X = Don't care
(2) Setting P3SEL1.x and P3SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.

Port P3, P3.4 to P3.7, Input/Output With Schmitt Trigger



NOTE: Functional representation only.

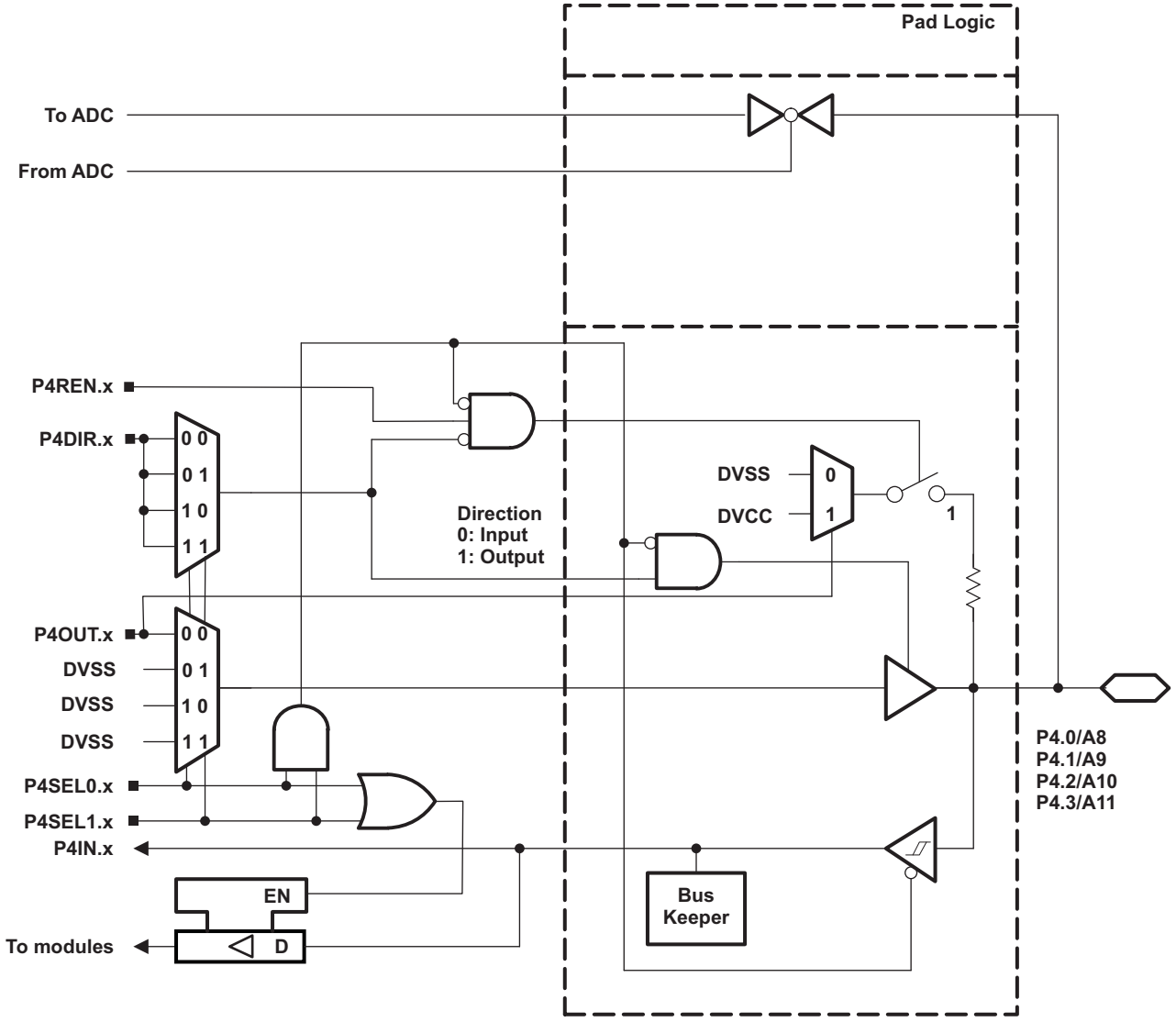
PRODUCT PREVIEW

Table 59. Port P3 (P3.4 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.4/TB0.3/SMCLK	4	P3.4 (I/O)	I: 0; O: 1	0	0
		TB0.CCI3A	0	0	1
		TB0.3	1		
		N/A	0	1	X
		SMCLK	1		
P3.5/TB0.4/COUT	5	P3.5 (I/O)	I: 0; O: 1	0	0
		TB0.CCI4A	0	0	1
		TB0.4	1		
		N/A	0	1	X
		COUT	1		
P3.6/TB0.5	6	P3.6 (I/O)	I: 0; O: 1	0	0
		TB0.CCI5A	0	0	1
		TB0.5	1		
		N/A	0	1	X
		Internally tied to DVSS	1		
P3.7/TB0.6	7	P3.7 (I/O)	I: 0; O: 1	0	0
		TB0.CCI6A	0	0	1
		TB0.6	1		
		N/A	0	1	X
		Internally tied to DVSS	1		

(1) X = Don't care

Port P4, P4.0 to P4.3, Input/Output With Schmitt Trigger



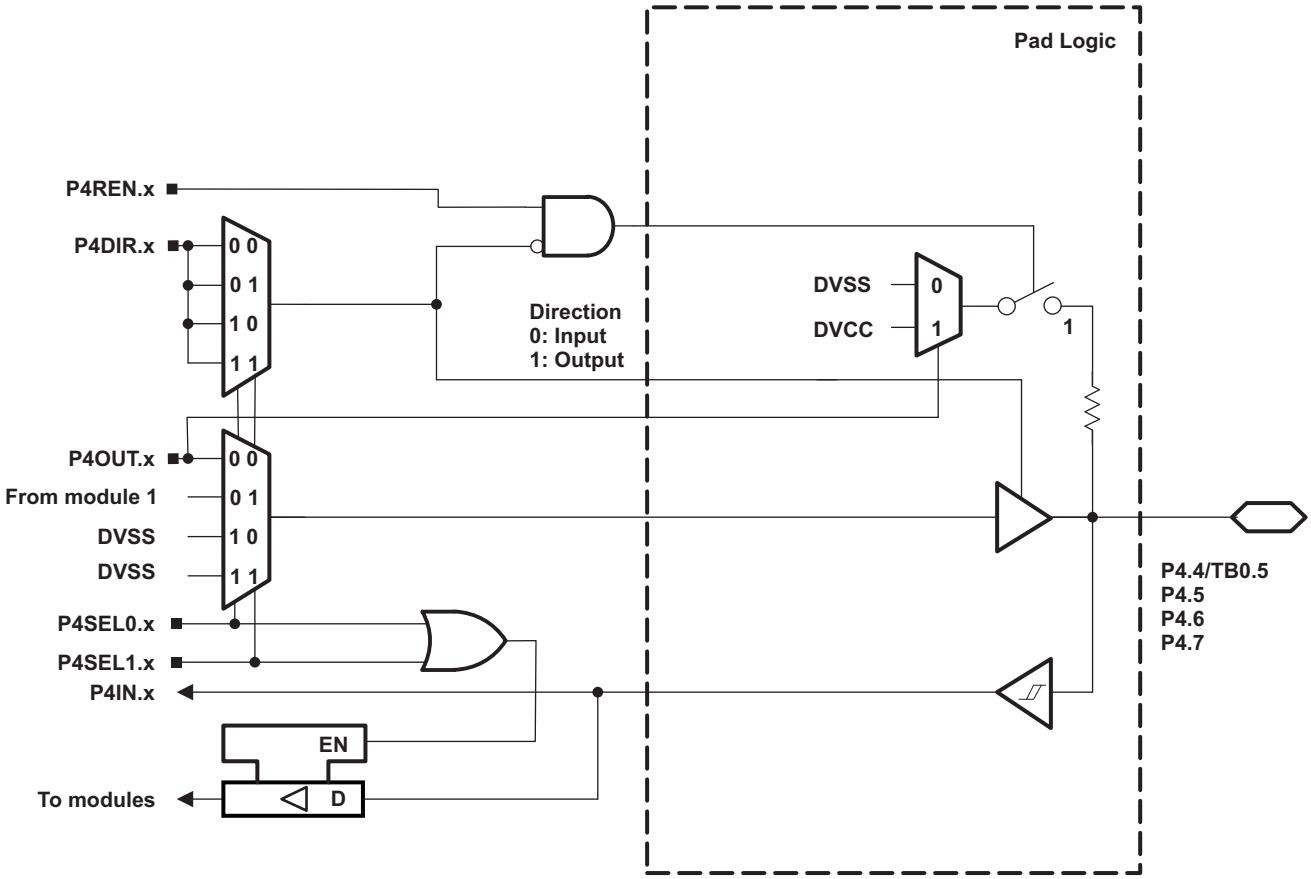
NOTE: Functional representation only.

Table 60. Port P4 (P4.0 to P4.3) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.0/A8	0	P4.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A8(2)	X	1	1
P4.1/A9	1	P4.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A9(2)	X	1	1
P4.2/A10	2	P4.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A10(2)	X	1	1
P4.3/A11	3	P4.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A11(2)	X	1	1

(1) X = Don't care
(2) Setting P4SEL1.x and P4SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4, P4.4 to P4.7, Input/Output With Schmitt Trigger



NOTE: Functional representation only.

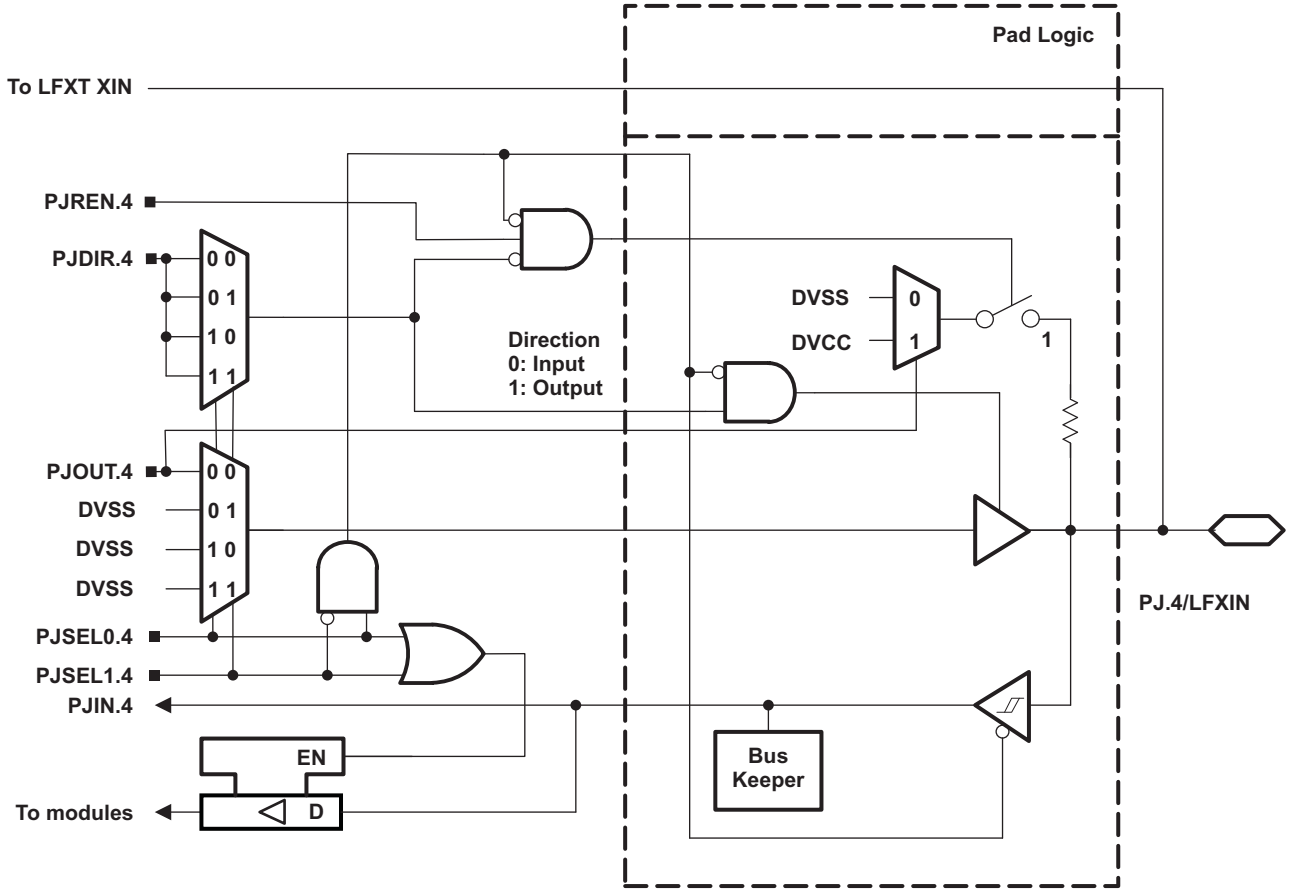
Table 61. Port P4 (P4.4 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.4/TB0.5	4	P4.4 (I/O)	I: 0; O: 1	0	0
		TB0.CCI5B	0	0	1
		TB0.5	1		
		N/A	0	1	X
		Internally tied to DVSS	1		
P4.5	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	X
		Internally tied to DVSS	1		
P4.6	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	X
		Internally tied to DVSS	1		
P4.7	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	X
		Internally tied to DVSS	1		

(1) X = Don't care

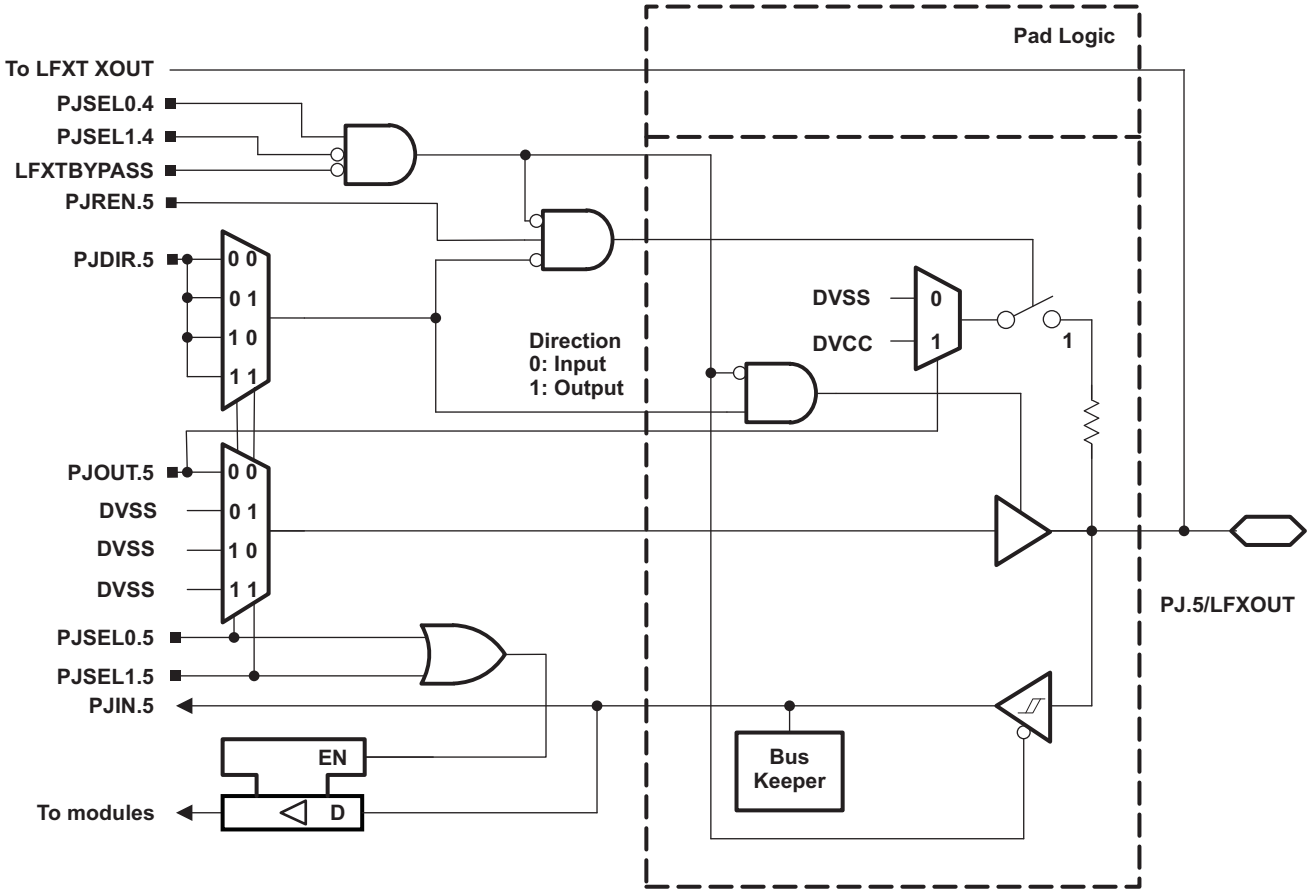
PRODUCT PREVIEW

Port PJ, PJ.4 and PJ.5 Input/Output With Schmitt Trigger



NOTE: Functional representation only.

PRODUCT PREVIEW



NOTE: Functional representation only.

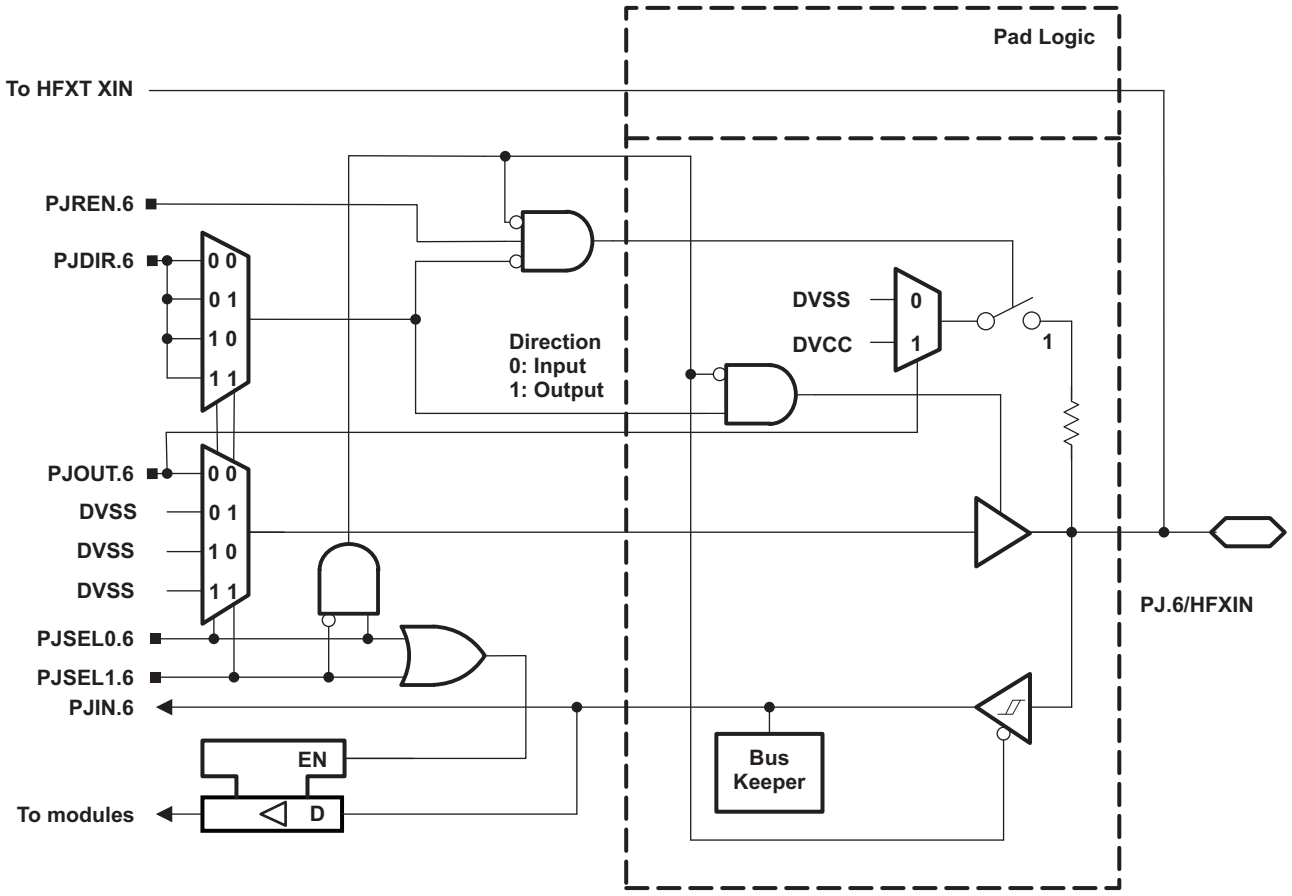
PRODUCT PREVIEW

Table 62. Port PJ (PJ.4 and PJ.5) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			PJDIR.x	PJSEL1.5	PJSEL0.5	PJSEL1.4	PJSEL0.4	LFXT BYPASS
PJ.4/LFXIN	4	PJ.4 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		LFXIN crystal mode[2]	X	X	X	0	1	0
		LFXIN bypass mode[2]	X	X	X	0	1	1
PJ.5/LFXOUT	5	PJ.5 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1[3]
		N/A	0	see[4]	see[4]	0	0	0
						1	X	
						X	X	1[3]
		Internally tied to DVSS	1	see[4]	see[4]	0	0	0
						1	X	
						X	X	1[3]
		LFXOUT crystal mode[2]	X	X	X	0	1	0

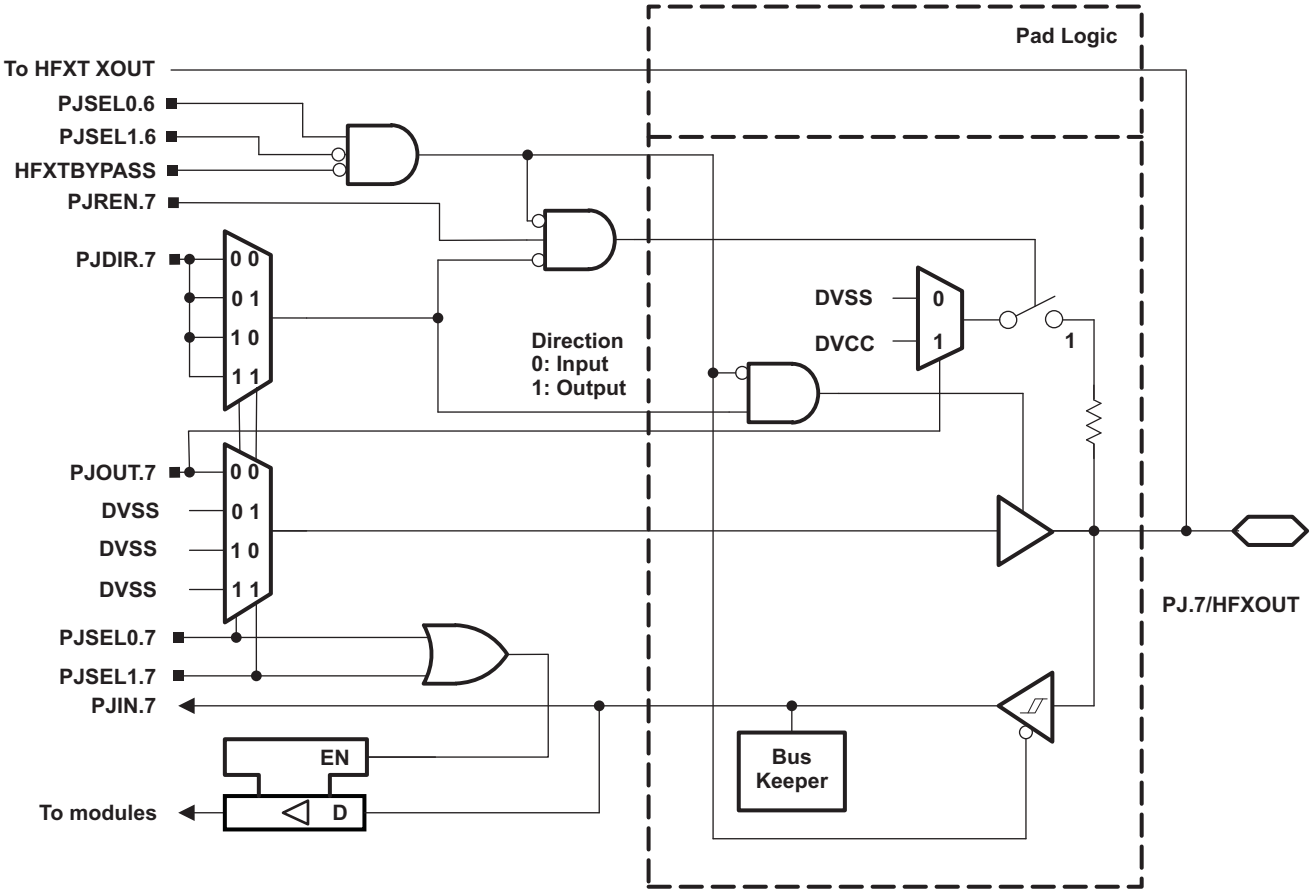
(1) X = Don't care
(2) If PJSEL1.4 = 0 and PJSEL0.4 = 1, the general-purpose I/O is disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.
(4) If PJSEL0.5 = 1 or PJSEL1.5 = 1, the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.

Port PJ, PJ.6 and PJ.7 Input/Output With Schmitt Trigger



NOTE: Functional representation only.

PRODUCT PREVIEW



NOTE: Functional representation only.

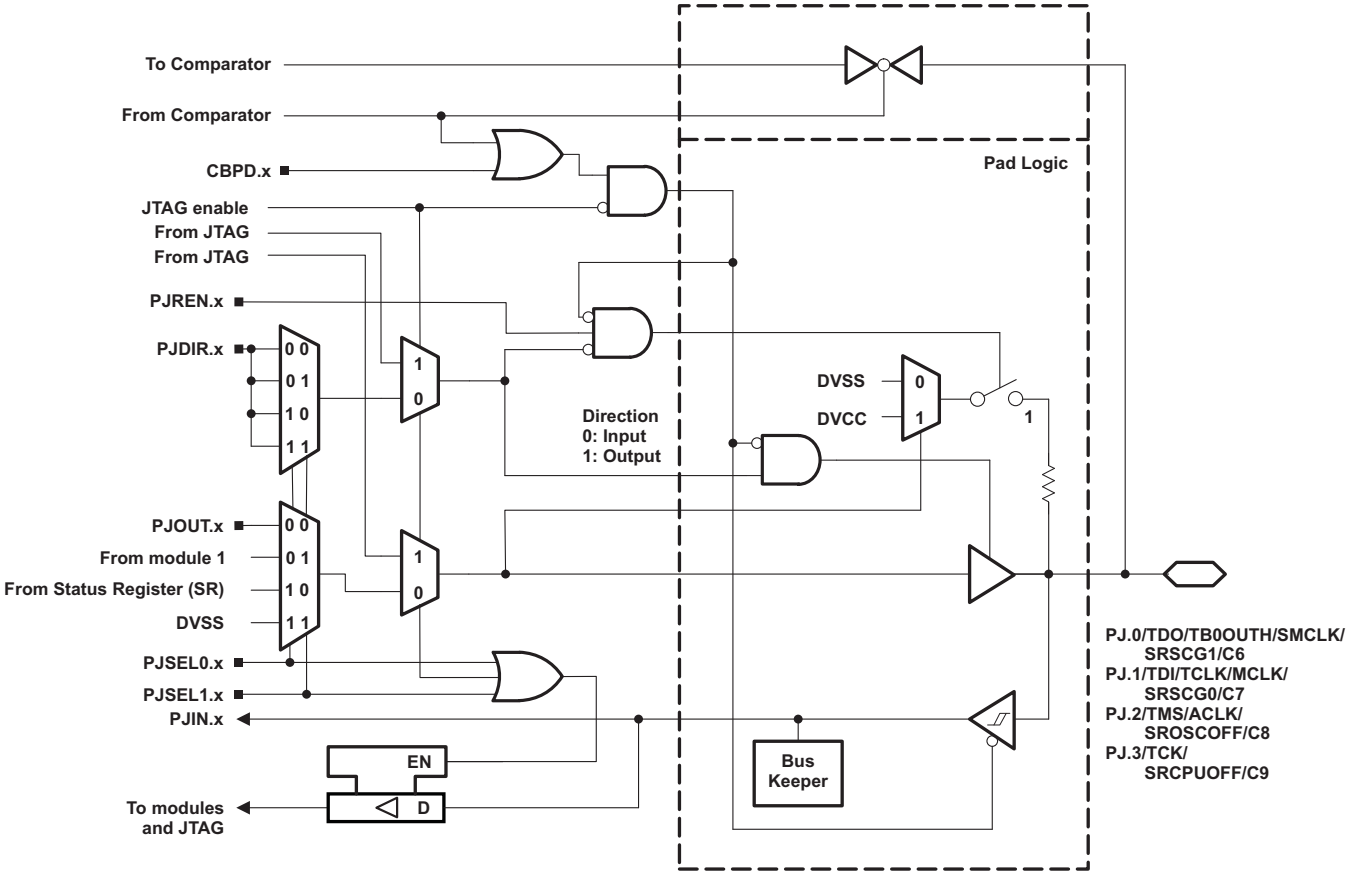
PRODUCT PREVIEW

Table 63. Port PJ (PJ.6 and PJ.7) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			PJDIR.x	PJSEL1.7	PJSEL0.7	PJSEL1.6	PJSEL0.6	HFXT BYPASS
PJ.6/HFXIN	6	PJ.6 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		HFXIN crystal mode[2]	X	X	X	0	1	0
		HFXIN bypass mode[2]	X	X	X	0	1	1
PJ.7/HFXOUT	5	PJ.7 (I/O)[3]	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1[4]
		N/A	0	see [3]	see [3]	0	0	0
						1	X	
						X	X	1[4]
		Internally tied to DVSS	1	see [3]	see [3]	0	0	0
						1	X	
						X	X	1[4]
		HFXOUT crystal mode[2]	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.6 and PJSEL0.7 are do not care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation and PJ.7 is configured as general-purpose I/O.
(3) With PJSEL0.7 = 1 or PJSEL1.7 =1 the general-purpose I/O functionality is disabled. No input function is available. Configured as output the pin is actively pulled to zero.
(4) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.

Port J, J.0 to J.3 JTAG pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger



NOTE: Functional representation only.

PRODUCT PREVIEW

Table 64. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS[1]			
			PJDIR.x	PJSEL1.x	PJSEL0.x	CEPD.x (Cx)
PJ.0/TDO/TB0OUTH/ SMCLK/SRSCG1/C6	0	PJ.0 (I/O)[2]	I: 0; O: 1	0	0	0
		TDO[3]	X	X	X	0
		TB0OUTH	0	0	1	0
		SMCLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit SCG1	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		C6[4]	X	X	X	1
PJ.1/TDI/TCLK/MCLK/ SRSCG0/C7	1	PJ.1 (I/O)[2]	I: 0; O: 1	0	0	0
		TDI/TCLK[3] [5]	X	X	X	0
		N/A	0	0	1	0
		MCLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit SCG0	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		C7[4]	X	X	X	1
PJ.2/TMS/ACLK/ SROSCOFF/C8	2	PJ.2 (I/O)[2]	I: 0; O: 1	0	0	0
		TMS[3] [5]	X	X	X	0
		N/A	0	0	1	0
		ACLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit OSCOFF	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		C8[4]	X	X	X	1
PJ.3/TCK/SRCPUOFF/C9	3	PJ.3 (I/O)[2]	I: 0; O: 1	0	0	0
		TCK[3] [5]	X	X	X	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		CPU Status Register Bit CPUOFF	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		C9[4]	X	X	X	1

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made via the SYS module or by the Spy-Bi-Wire four-wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPD.x bits have an effect in these cases.
(4) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.
(5) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

DEVICE DESCRIPTORS (TLV)

Table 66 lists the contents of the device descriptor tag-length-value (TLV) structure for MSP430FR59xx devices including AES. Table 65 summarizes the Device IDs of the corresponding MSP430FR59xx devices.

Table 68 lists the contents of the device descriptor tag-length-value (TLV) structure for MSP430FR58xx devices without AES. Table 67 summarizes the Device IDs of the corresponding MSP430FR58xx devices.

Table 65. Device IDs for MSP430FR59xx Devices With AES

Device	Device ID	
	01A05h	01A04h
MSP430FR5969	081h	069h
MSP430FR5968	081h	068h
MSP430FR5967	081h	067h
MSP430FR5949	081h	061h
MSP430FR5948	081h	060h
MSP430FR5947	081h	05Fh
MSP430FR5959	081h	065h
MSP430FR5958	081h	064h
MSP430FR5957	081h	063h

Table 66. Device Descriptor Table MSP430FR59xx(1)

	Description	MSP430FR59xx	
		Address	Value
Info Block	Info length	01A01h	06h
	CRC length	01A01h	06h
	CRC value	01A02h	per unit
		01A03h	per unit
	Device ID	01A04h	see Table 65
		01A05h	
	Hardware revision	01A06h	per unit
	Firmware revision	01A07h	per unit
Die Record	Die Record Tag	01A08h	08h
	Die Record length	01A09h	0Ah
	Lot/Wafer ID	01A0Ah	per unit
		01A0Bh	per unit
		01A0Ch	per unit
		01A0Dh	per unit
	Die X position	01A0Eh	per unit
		01A0Fh	per unit
	Die Y position	01A10h	per unit
		01A11h	per unit
	Test results	01A12h	per unit
		01A13h	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	11h
	ADC12 Calibration length	01A15h	10h
	ADC Gain Factor(2)	01A16h	per unit
		01A17h	per unit

(1) NA = Not applicable, per unit = content can differ from device to device
(2) ADC Gain: the gain correction factor is measured using the internal voltage reference with REFOUT=0. Other settings (for example, with REFOUT = 1) can result in different correction factors.

Table 66. Device Descriptor Table MSP430FR59xx(1) (continued)

	Description	MSP430FR59xx	
		Address	Value
	ADC Offset(3)	01A18h	per unit
		01A19h	per unit
	ADC 1.2-V Reference Temp. Sensor 30°C	01A1Ah	per unit
		01A1Bh	per unit
	ADC 1.2-V Reference Temp. Sensor 85°C	01A1Ch	per unit
		01A1Dh	per unit
	ADC 2.0-V Reference Temp. Sensor 30°C	01A1Eh	per unit
		01A1Fh	per unit
	ADC 2.0-V Reference Temp. Sensor 85°C	01A20h	per unit
		01A21h	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	per unit
		01A23h	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	per unit
		01A25h	per unit
REF Calibration	REF Calibration Tag	01A26h	12h
	REF Calibration length	01A27h	06h
	REF 1.2-V Reference	01A28h	per unit
		01A29h	per unit
	REF 2.0-V Reference	01A2Ah	per unit
		01A2Bh	per unit
	REF 2.5-V Reference	01A2Ch	per unit
		01A2Dh	per unit
Random Number	128-bit Random Number Tag	01A2Eh	15h
	Random Number Length	01A2Fh	10h
	128-bit Random Number(4)	01A30h	per unit
		01A31h	per unit
		01A32h	per unit
		01A33h	per unit
		01A34h	per unit
		01A35h	per unit
		01A36h	per unit
		01A37h	per unit
		01A38h	per unit
		01A39h	per unit
		01A3Ah	per unit
		01A3Bh	per unit
		01A3Ch	per unit
		01A3Dh	per unit
		01A3Eh	per unit
		01A3Fh	per unit

(3) ADC Offset: the offset correction factor is measured using the internal 2.5V reference.
(4) 128-bit Random Number: The random number is generated during production test.

PRODUCT PREVIEW

Table 67. Device IDs for MSP430FR58xx Devices Without AES

Device	Device ID	
	01A05h	01A04h
MSP430FR5869	081h	05Dh
MSP430FR5868	081h	05Ch
MSP430FR5867	081h	05Bh
MSP430FR5849	081h	055h
MSP430FR5848	081h	054h
MSP430FR5847	081h	053h
MSP430FR5859	081h	059h
MSP430FR5858	081h	058h
MSP430FR5857	081h	057h

Table 68. Device Descriptor Table MSP40FR58xx(1)

	Description	MSP430FR58xx	
		Address	Value
Info Block	Info length	01A01h	06h
	CRC length	01A01h	06h
	CRC value	01A02h	per unit
		01A03h	per unit
	Device ID	01A04h	see Table 67
	Device ID	01A05h	
	Hardware revision	01A06h	per unit
	Firmware revision	01A07h	per unit
Die Record	Die Record Tag	01A08h	08h
	Die Record length	01A09h	0Ah
	Lot/Wafer ID	01A0Ah	per unit
		01A0Bh	per unit
		01A0Ch	per unit
		01A0Dh	per unit
	Die X position	01A0Eh	per unit
		01A0Fh	per unit
	Die Y position	01A10h	per unit
		01A11h	per unit
	Test results	01A12h	per unit
		01A13h	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	11h
	ADC12 Calibration length	01A15h	10h
	ADC Gain Factor(2)	01A16h	per unit
		01A17h	per unit
	ADC Offset(3)	01A18h	per unit
		01A19h	per unit
	ADC 1.2-V Reference Temp. Sensor 30°C	01A1Ah	per unit
		01A1Bh	per unit
	ADC 1.2-V Reference Temp. Sensor 85°C	01A1Ch	per unit
		01A1Dh	per unit

(1) NA = Not applicable, per unit = content can differ from device to device
(2) ADC Gain: the gain correction factor is measured using the internal voltage reference with REFOUT=0. Other settings (for example, with REFOUT = 1) can result in different correction factors.
(3) ADC Offset: the offset correction factor is measured using the internal 2.5V reference.

Table 68. Device Descriptor Table MSP40FR58xx(1) (continued)

	Description	MSP430FR58xx	
		Address	Value
	ADC 2.0-V Reference Temp. Sensor 30°C	01A1Eh	per unit
		01A1Fh	per unit
	ADC 2.0-V Reference Temp. Sensor 85°C	01A20h	per unit
		01A21h	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	per unit
		01A23h	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	per unit
		01A25h	per unit
REF Calibration	REF Calibration Tag	01A26h	12h
	REF Calibration length	01A27h	06h
	REF 1.2-V Reference	01A28h	per unit
		01A29h	per unit
	REF 2.0-V Reference	01A2Ah	per unit
		01A2Bh	per unit
	REF 2.5-V Reference	01A2Ch	per unit
		01A2Dh	per unit
Random Number	128-bit Random Number Tag	01A2Eh	15h
	Random Number Length	01A2Fh	10h
	128-bit Random Number(4)	01A30h	per unit
		01A31h	per unit
		01A32h	per unit
		01A33h	per unit
		01A34h	per unit
		01A35h	per unit
		01A36h	per unit
		01A37h	per unit
		01A38h	per unit
		01A39h	per unit
		01A3Ah	per unit
		01A3Bh	per unit
		01A3Ch	per unit
		01A3Dh	per unit
		01A3Eh	per unit
		01A3Fh	per unit

(4) 128-bit Random Number: The random number is generated during production test.

PRODUCT PREVIEW

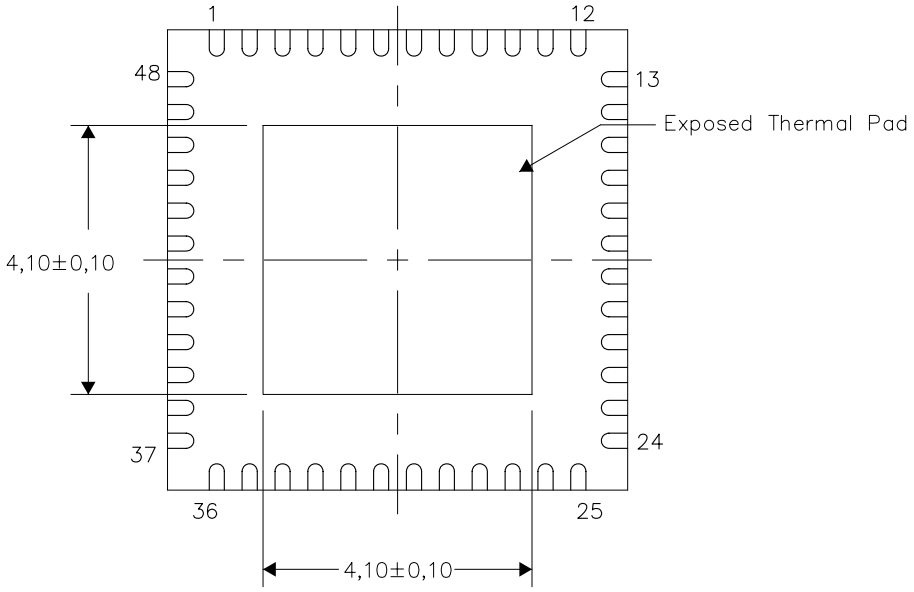
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



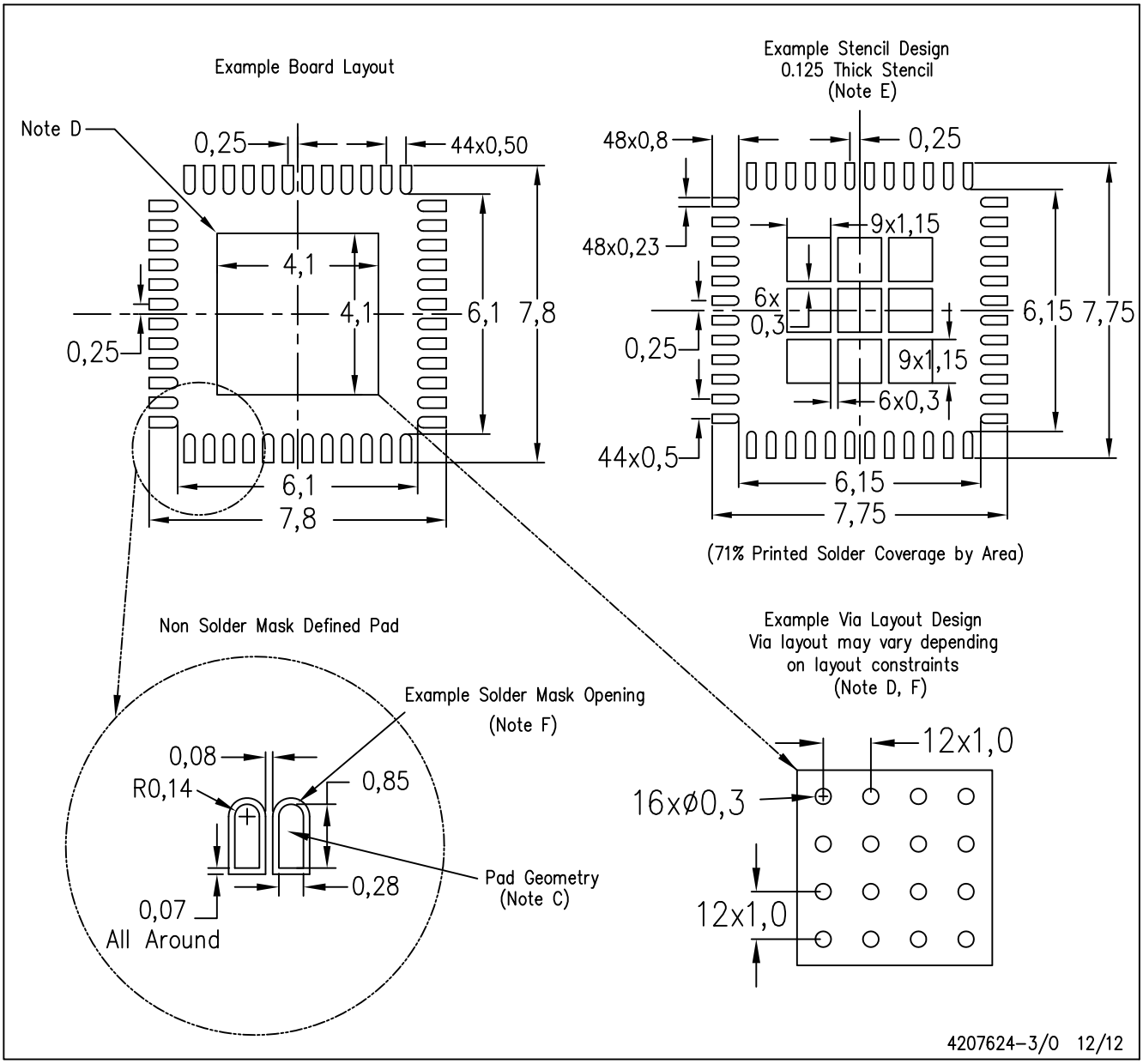
Bottom View

Exposed Thermal Pad Dimensions

4206354–3/R 08/11

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

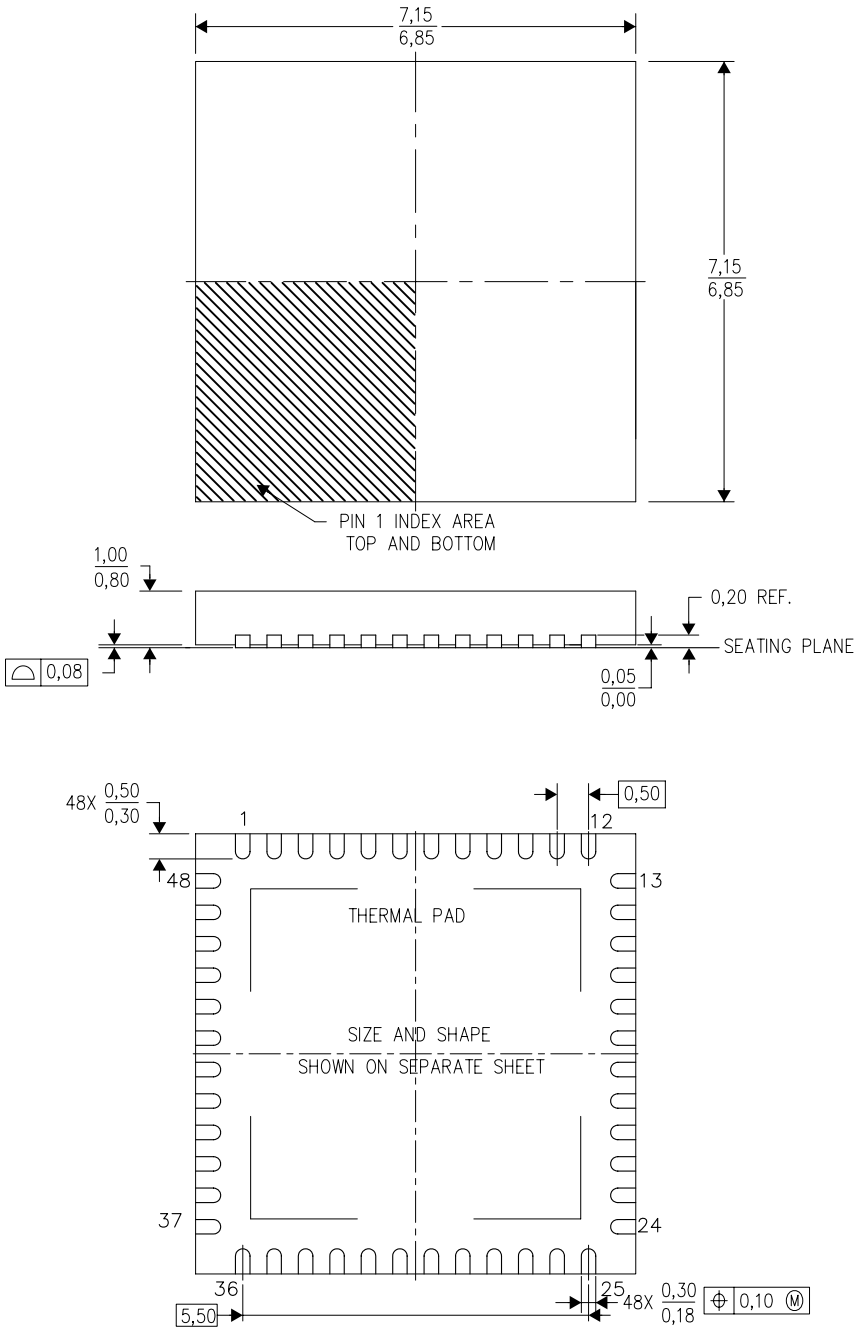
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
XMS430FR5969IRGZR	ACTIVE	VQFN	RGZ	48	2500	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265