MAXIM

CMOS 8-Bit μP Compatible 12-Bit DAC

MX7548

General Description

The MX7548 is a 12-bit CMOS, current output, multiplying digital-to-analog converter (DAC) with a versatile interface for microprocessors using 8-bit busses. The MX7548 accepts data into its input-registers in two bytes in either left- or right-justified format, least significant byte or most significant byte first. Standard $\overline{WR}$ and $\overline{CSLSB}$ or $\overline{CSMSB}$ inputs control the data load operation. A separate $\overline{LDAC}$ input controls transfer of data from the input register to the DAC register allowing for simultaneous update of all DACs in multi-DAC systems. A data override input forces the DAC output to full-scale or zero-code without altering the contents of the input registers. This permits the user to perform DAC calibration conveniently without having to load calibration data into the DAC.

The MX7548 works with a single +5V, +12V or +15V power supply, and the electrical characteristics are specified at all of these supply voltages. All digital inputs are TTL and +5V-CMOS compatible with any of these supply voltages.

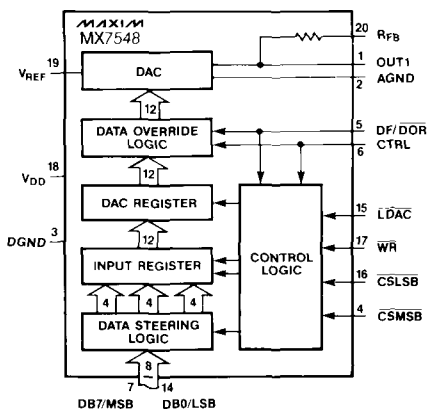
Maxim MX7548 uses low tempco thin-film resistors which are laser trimmed to ±¼LSB linearity and better than ±1LSB gain accuracy. The digital inputs are designed with improved ESD protection and can typically withstand over 5,000V of ESD voltages.

The MX7548 is supplied in 20-lead narrow DIP, PLCC, and Small Outline packages.

Applications

Process Control
Digitally Controlled Filters
Motion Control Systems
Automatic Test Equipment
μP Controlled Systems
Programmable Gain Amplifiers
Programmable Power Supplies

Functional Diagram



Features

- **8-Bit Bus Compatible**
- **Versatile μP interface with Selectable Data Format and Data Override**
- **Fast Interface Timing—120ns min Write Pulse Width**
- **All Grades 12-Bit Monotonic Over Temperature**
- **±1LSB max Gain Accuracy**
- **Operation specified at +5V, +12V or +15V Supply Voltages**
- **Small Footprint Packages**
- **High ESD Resistance**

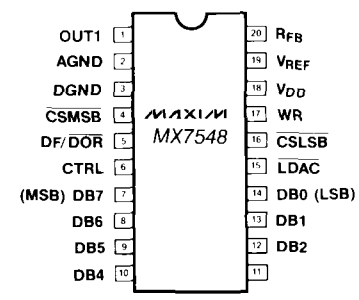
Ordering Information

PART	TEMP. RANGE	PACKAGE*	LINEARITY
MX7548JN	0°C to +70°C	Plastic DIP	±1 LSB
MX7548KN	0°C to +70°C	Plastic DIP	±½ LSB
MX7548JCWP	0°C to +70°C	Wide SO	±1 LSB
MX7548KCWP	0°C to +70°C	Wide SO	±½ LSB
MX7548JP	0°C to +70°C	PLCC	±1 LSB
MX7548KP	0°C to +70°C	PLCC	±½ LSB
MX7548J/D	0°C to +70°C	Dice	±1 LSB
MX7548AQ	-25°C to +85°C	CERDIP	±1 LSB
MX7548BQ	-25°C to +85°C	CERDIP	±½ LSB
MX7548SD	-55°C to +125°C	Ceramic	±1 LSB
MX7548TD	-55°C to +125°C	Ceramic	±½ LSB
MX7548SQ	-55°C to +125°C	CERDIP	±1 LSB
MX7548TQ	-55°C to +125°C	CERDIP	±½ LSB

Maxim reserves the right to ship Ceramic in lieu of CERDIP packages.

Pin Configuration

Top View



See page 11 for Plastic Chip Carrier Pin Configuration

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... +17V
V_{REF} to AGND ..... ±25V
V_{RFB} to AGND ..... ±25V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{OUT1} to DGND ..... -0.3V, V_{DD}
AGND to DGND ..... -0.3V, V_{DD}
Power Dissipation to +75°C (any package) 450mW
Derate above 75°C by ..... 6mW/°C

Operating Temperature Ranges
MX7548J/K ..... 0°C to +70°C
MX7548A/B ..... -25°C to +85°C
MX7548S/T ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, +12V or +15V; V_{REF} = +10V; V_{OUT1} = AGND = DGND = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N				12			Bits
Integral Nonlinearity	INL		J,A,S K,B,T				±1 ±½	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic to 12 bits	J,A,S K,B,T				±1 ±½	LSB
Gain Error	FSE	Using internal feedback resistor	J,A,S	T_A = +25°C T_A = T_{MIN} to T_{MAX}			±2 ±3	LSB
			K,B,T	T_A = +25°C T_A = T_{MIN} to T_{MAX}			+1 ±2	
Gain Tempco ΔGain/ΔTemp. (Note 1)	TCFS					2	+5	ppm/°C
DC Supply Rejection ΔGain/ΔSupply	PSR	ΔV_{DD} = ±5%		T_A = +25°C T_A = T_{MIN} to T_{MAX}			±0.001 +0.002	%/%
DYNAMIC PERFORMANCE (Note 1)								
Current Settling Time	tS	To ½LSB. OUT1 load: R_L = 100Ω; CL= 13pF; T_A = +25°C DAC register alternately loaded with all 1s and all 0s.					1	μs
Digital to Analog Glitch Impulse	Q	V_{REF} = 0V. OUT1 load: R_L = 100Ω; C_L = 13pF DAC register alternately loaded with all 1s and all 0s.					200	nV-s
AC Feedthrough at OUT1 (Note 2)	FTE	V_{REF} = ± 10V_{P-P} at 10kHz. DAC register loaded with all 0s.					5	mV_{p-p}
Total Harmonic Distortion	THD	V_{REF} = 6V_{RMS} at 1kHz. DAC register loaded with all 1s.					-90	dB
Output Noise Voltage Density	en	10Hz to 100kHz. Measured between R_{FB} and OUT1.				13	15	nV/Hz
REFERENCE INPUT								
Input Resistance	R_{REF}	V_{REF} pin to OUT1			7	11	15	kΩ
Input Resistant Tempco (Note 1)	TCR					-200		ppm/°C
ANALOG OUTPUT								
OUT1 Leakage Current	ILKG	DAC register loaded with all 0s.		T_A = +25°C		±0.5	±5	nA
			J,K,A,B S,T	T_A = T_{MIN} to T_{MAX}			±25 ±100	
OUT1 Capacitance (Note 1)	C_{OUT1}	DAC register loaded with all 0s.				40	70	pF
		DAC register loaded with all 1s.				100	140	

ELECTRICAL CHARACTERISTICS (continued)

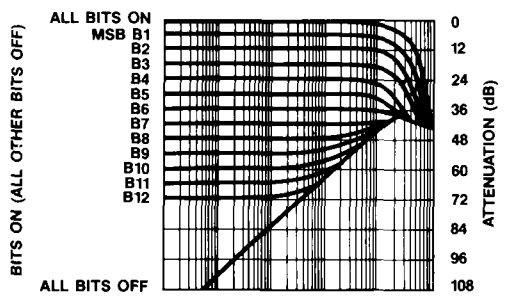
(V_{DD} = +5V, +12V or +15V; V_{REF} = +10V; V_{OUT1} = AGND = DGND = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input High Voltage	V_H			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	Digital Inputs at 0V or V_{DD}				±1	μA
Input Capacitance (Note 1)	C_{IN}	Digital Inputs at 0V or V_{DD}				7	pF
SWITCHING CHARACTERISTICS (Notes 1, 3)							
Data Valid Setup	t_{DS}			160			ns
Data Valid Hold	t_{DH}			10			ns
$\overline{CS}$MSB or $\overline{CS}$LSB to $\overline{WR}$ Setup	t_{CWS}			0			ns
$\overline{CS}$MSB or $\overline{CS}$LSB to $\overline{WR}$ Hold	t_{CWH}			0			ns
$\overline{LDAC}$ to $\overline{WR}$ Setup	t_{LWS}			0			ns
$\overline{LDAC}$ to $\overline{WR}$ Hold	t_{LWH}			0			ns
$\overline{WR}$ Pulse Width	t_{WR}			120			ns
POWER SUPPLY							
V_{DD} Range	V_{DD}	Specifications are guaranteed over these ranges.	V_{DD} = +12V or +15V V_{DD} = +5V	+11.4 +4.75		+15.75 +5.25	V V
I_{DD} Range	I_{DD}	All digital inputs at V_{IL} or V_{IH}	V_{DD} = +12V or +15V V_{DD} = +5V			3 2	mA
		All digital inputs at 0V or V_{DD}	V_{DD} = +12V or +15V V_{DD} = +5V		100	1 300	mA μA

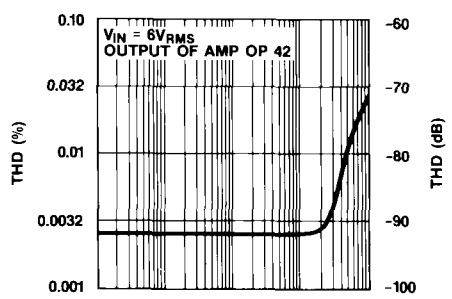
Note 1: Guaranteed by design and not subject to test.
Note 2: Feedthrough can be further reduced by connecting the metal lid to DGND on the ceramic package.
Note 3: See Figure 5 Timing Diagram.

Typical Operating Characteristics

MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE

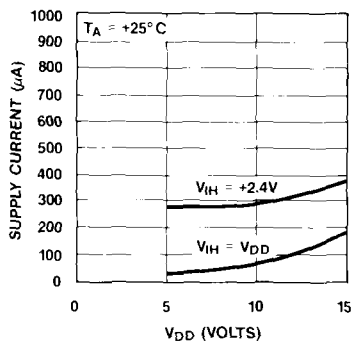


MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY

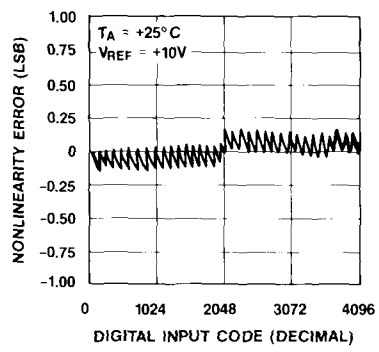


Typical Operating Characteristics (continued)

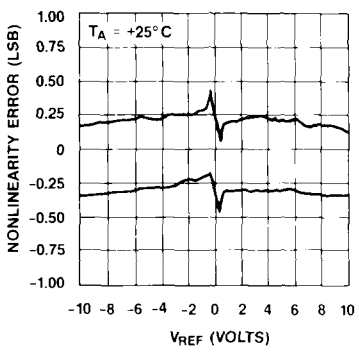
SUPPLY CURRENT vs SUPPLY VOLTAGE



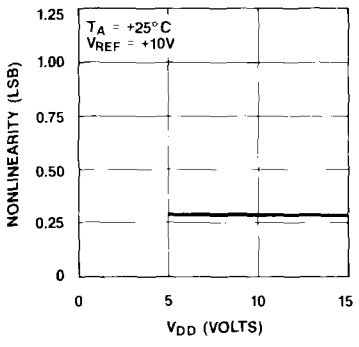
NONLINEARITY ERROR vs DIGITAL CODE (V_{DD} = +5V OR +15V)



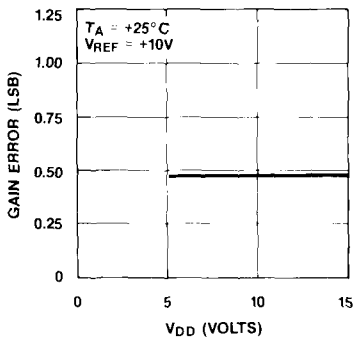
NONLINEARITY ERROR vs REFERENCE VOLTAGE (V_{DD} = +5V OR +15V)



NONLINEARITY vs SUPPLY VOLTAGE



GAIN ERROR vs SUPPLY VOLTAGE



Detailed Description

D/A Converter

The basic MX7548 DAC circuit consists of a laser trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or AGND depending on the status of each input bit. Although the current at OUT1 and AGND depends on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF}.

The current output can be converted into a voltage by adding an external output amplifier (Figure 6). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a

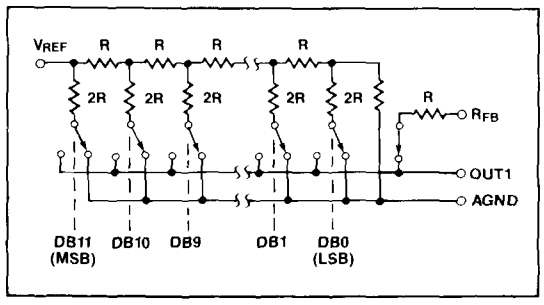


Figure 1. Simplified D/A Circuit of MX7548

current source is used for the reference input, then a low tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

The internal feedback resistor R_{FB} is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The OUT1 pin output capacitance, C_{OUT1}, is code dependent and is typically 40pF to 100pF, with all switches to AGND and OUT1 respectively.

Equivalent Circuit Analysis

Figure 2 shows the equivalent circuits for the MX7548 analog section. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents. The *equivalent output resistor of the DAC is* R_O, which varies with digital input code from 0.8R to 2R (infinite at zero code), where R is typically 11kΩ. Capacitor C_{OUT1} represents the capacitances of the switches used in the R-2R ladder. When inputs are switched from low to high, the capacitance at OUT1 changes from about 40pF to 100pF. This capacitance is code-*dependent and is a function of the number of ON* switches that are connected to the output. $V_T(V_{REF},D)$ is the equivalent voltage source controlled by V_{REF} and the digital input code (D).

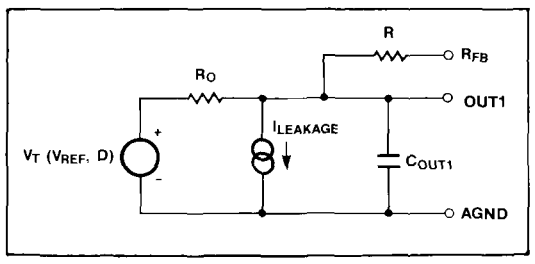


Figure 2. MX7548 Equivalent Analog Output Circuit

Digital Circuit

The input buffer inverters act as level shifters converting TTL levels into CMOS logic levels. The MX7548 uses an internal voltage regulator for the input buffer inverters to assure TTL compatibility with +5V to +15V power supplies. This regulator also results in exceptional PSRR, and digital interface times that are independent of the supply voltage.

The MX7548 digital circuitry contains a data steering logic, input registers, DAC register with data-override features that together form a versatile interface between the DAC switches and an 8-bit wide data bus.

All digital inputs are ruggedized against electrostatic-discharge (ESD) sensitivity and can typically withstand ESD voltages of over 5kV.

Digital Interface Information

Interface Inputs

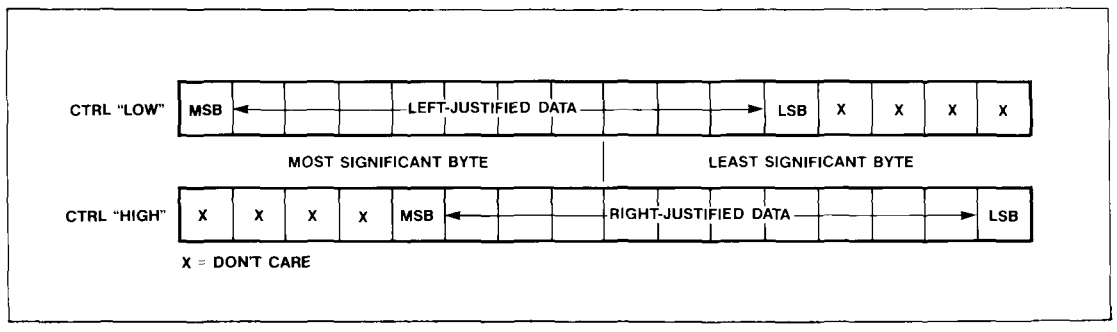
DF/$\overline{\text{DOR}}$ (Pin 5)—Data Format/Data Override. This input works together with the CTRL input to select *either right or left justified data format, or select either* zero-scale or full-scale override of DAC output. Use of Data Override does not affect data held in the DAC register.

CTRL (Pin 6) — Control Input. See DF/$\overline{\text{DOR}}$ description.

Table 1. Data Format and Override Control

DF/$\overline{\text{DOR}}$	CTRL	Function
0	0	DAC forced to zero scale (all zeros)
0	1	DAC forced to full scale (all ones)
1	0	Left-justified data format selected
1	1	Right-justified data format selected

CTRL (Pin 6)—Control Input (Refer also to DF/$\overline{\text{DOR}}$)



$\overline{\text{CSMSB}}$ (Pin 4)—Chip Select Most Significant Byte. Active low input. Loads input data into the Input Register when used in combination with $\overline{\text{WR}}$, or into both Input and DAC Registers when used in combination with $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$.

$\overline{\text{CSLSB}}$ (Pin 16)—Chip Select Least Significant Byte. Active low input. Loads input data into the Input Register when used in combination with $\overline{\text{WR}}$, or into both Input and DAC Registers when used in combination with $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$.

$\overline{\text{WR}}$ (Pin 17)—Write Input. Active low input. Loads input data into the Input Register or into both Input and DAC Registers when used in combination with $\overline{\text{CSMSB}}$, $\overline{\text{CSLSB}}$ and $\overline{\text{LDAC}}$.

$\overline{\text{LDAC}}$ (Pin 15)—Load DAC Input. Active low input. Loads DAC Register with either the contents of the Input Register or with the external input data.

Table 2. Data Load and Transfer Control

$\overline{\text{WR}}$	$\overline{\text{CSMSB}}$	$\overline{\text{CSLSB}}$	$\overline{\text{LDAC}}$	Function
0	1	0	1	Load LS Byte into Input Register
0	1	0	0	Load LS Byte into Input and DAC Registers
0	0	1	1	Load MS Byte into Input Register
0	0	1	0	Load MS Byte into Input and DAC Registers
0	1	1	0	Load Input Register contents into DAC Register
1	X	X	X	No data transfer

Automatic Transfer Mode

In this mode the data is transferred to the DAC Register automatically when the Input Register is loaded with the external input data. As shown in Figure 9, the $\overline{\text{LDAC}}$ is either connected to the $\overline{\text{CSMSB}}$ or the $\overline{\text{CSLSB}}$ in this mode and transfers data in 8+4-bit format into the DAC register automatically. The first write cycle (Figure 3) loads the first byte of data into the Input Register, and the second write cycle loads the second byte. As the second byte is loaded into the Input Register, the contents of the Input Register is also transferred into the DAC Register.

Strobed Transfer Mode

If several MX7548s are used in a system, they can be updated simultaneously by using the Strobed Transfer Mode. As shown in Figure 13, a master strobe signal connected to the $\overline{\text{LDAC}}$ input of each MX7548 transfers the contents of the Input Registers to the DAC Registers.

Three write cycles (Figure 4) are required to transfer 8+4-bit data to the DAC registers. The first two cycles load the Input Registers with high and low bytes of the input data sequentially. The third cycle loads the DAC Registers with the contents of the Input Registers. If there are multiple MX7548s in the system, each DAC needs to be loaded individually with data before the $\overline{\text{LDAC}}$ signal is activated.

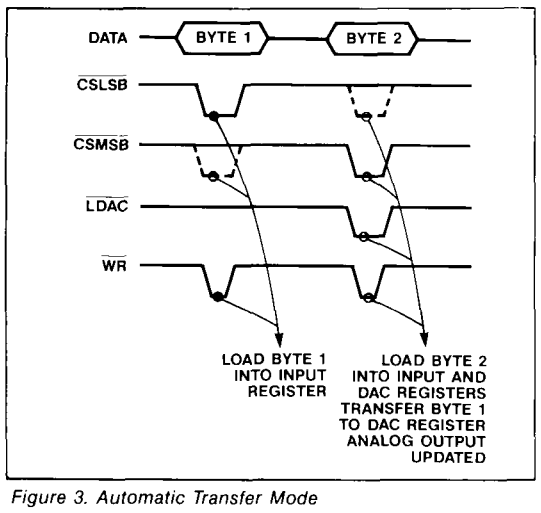


Figure 3. Automatic Transfer Mode

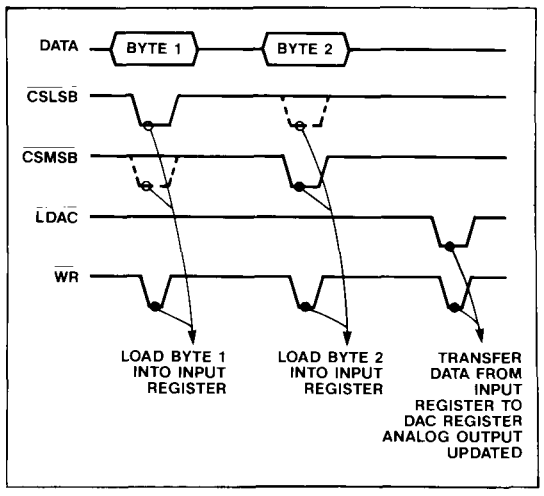
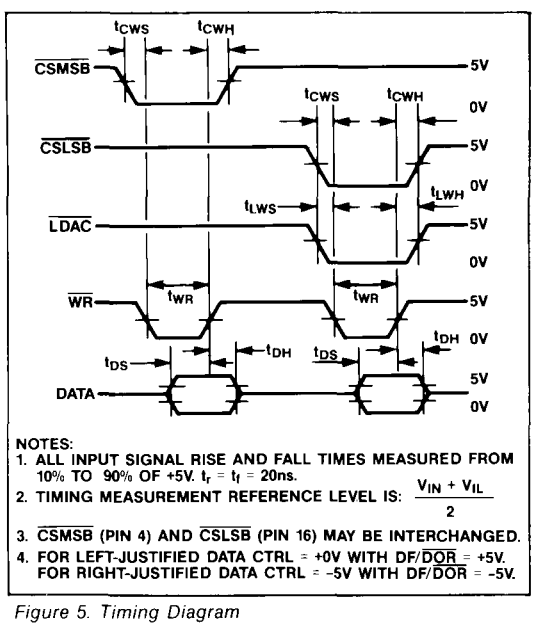


Figure 4. Strobed Transfer Mode



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS: $\frac{V_{IH} + V_{IL}}{2}$
3. $\overline{CSMSB}$ (PIN 4) AND $\overline{CSLSB}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/$\overline{DOR}$ = +5V. FOR RIGHT-JUSTIFIED DATA CTRL = -5V WITH DF/$\overline{DOR}$ = -5V.

Figure 5. Timing Diagram

Data Override

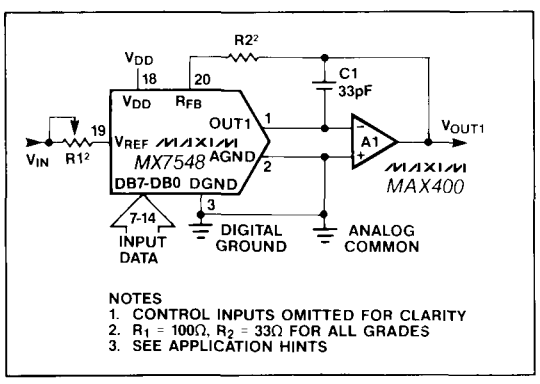
The MX7548 output can be forced to zero-scale (all 0s) or full-scale (all 1s) codes by using the DF/$\overline{DOR}$ and CTRL inputs (Table 1). When the override function is used, the DAC Register contents remain unchanged. The DAC output reflects the value of the DAC Register contents when the override function is removed. This is a convenience for the user since the MX7548 can be calibrated without having to load calibration codes into the DAC.

Circuit Configurations

Unipolar Operation

The most common configuration for the MX7548 is shown in Figure 6. This circuit is used for unipolar binary operation or 2-quadrant multiplication. The code table for this mode is given in Table 3. Note that the polarity of the output is the inverse of the reference voltage, V_{REF}.

In many applications the gain adjustment will not be necessary, especially with versions that guarantee maximum ±1LSB gain errors. In these cases and also when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 5 can be omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2. The full scale is adjusted by loading the DAC with all 1s code (using the override function) and adjusting R1 for $V_{OUT1} = -V_{IN}(4095/4096)$.



NOTES
1. CONTROL INPUTS OMITTED FOR CLARITY
2. $R_1 = 100\Omega$, $R_2 = 33\Omega$ FOR ALL GRADES
3. SEE APPLICATION HINTS

Figure 6. Unipolar Binary Operation

Table 3. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0

The capacitor C1 provides phase compensation and helps reduce the overshoot and ringing when using fast amplifiers at the output of the DACs.

Bipolar Operation

With the circuit configuration shown in Figure 7, the MX7548 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors, R3, R4 and R5, are required. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature characteristics, and they should match to 0.01% or better for 12-bit performance. The code table for the output, which is 2's complement is listed in Table 4. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude. The U1 inverter on the MSB line converts the 2's complement input code to offset-binary code. If this inversion is done in software using an exclusive-OR instruction or the input code is in offset binary, the U1 inverter can be omitted. Table 5 shows the code relationships to output voltage for the offset binary operation.

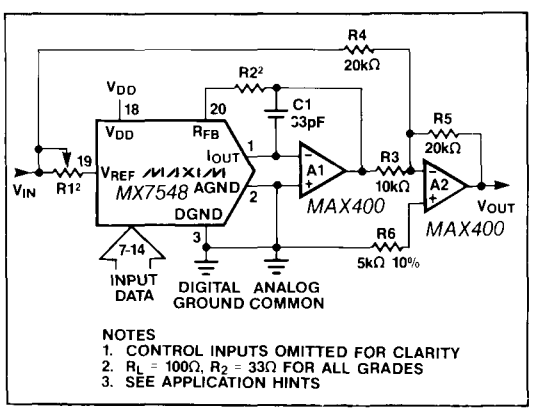


Figure 7. Bipolar Operation (Offset Binary Coding)

Table 4. 2's Complement Code Table for Circuit of Figure 4

DIGITAL INPUT MSB		LSB	ANALOG OUTPUT
0111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
0000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	0
1111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for V_{OUT1} = 0V. Full scale can be trimmed by loading the DAC with all 0s or all 1s and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. In many applications the gain adjustment will not be necessary, especially when using parts with guaranteed maximum ±1LSB gain errors. In those cases and also when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 7 can be omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

Table 5. Offset Binary Code Table

DIGITAL INPUT MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000	0000	0000	0
0111	1111	1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Single Supply Operation (Voltage Mode)

Figure 8 shows the MX7548 connected as a voltage output DAC. Note that with this circuit the MX7548 operates with a single supply and generates a positive voltage output without an output amplifier and without having to use a negative reference. OUT1 is connected to the reference input and AGND is grounded. V_{REF} pin, now the DAC output, is a voltage source with a constant impedance equal to the reference input resistance (typically 11kΩ). This output should be buffered with an op amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

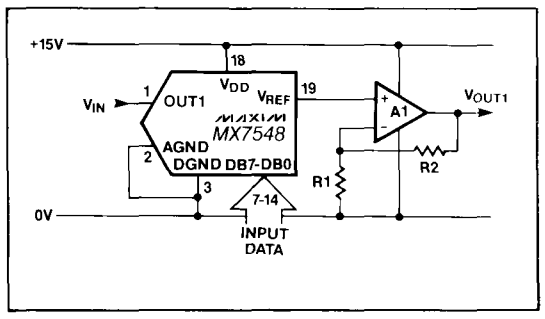


Figure 8. Single Supply Operation Using Voltage Switching Mode

The input impedance of the reference input (OUT1) for this mode is code dependent, and the response time of the circuit depends on the behavior of the reference source with changing load conditions.

It should also be noted that the reference input (the voltage at OUT1) must always be positive with respect to AGND and is limited to no more than 2.5V when V_{DD} is +12V to +15V. If the reference voltage is greater

than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral (INL) and differential nonlinearity (DNL).

The output voltage of this circuit is:

$$V_{OUT1} = (V_{IN})\ (D)\ \frac{(R1 + R2)}{(R1)}$$

where D is a fractional representation of the digital input word.

Microprocessor Interfacing

MX7548 to MC6809 Interface

Figure 9 shows the MX7548 interface circuit for the MC6809 microprocessor, using the automatic transfer mode (8+4-bit data). LDD and STD instructions are used to fetch and store the high-byte first, then the low-byte data. The even-order address selects the CSMSB input to load the high-byte data first.

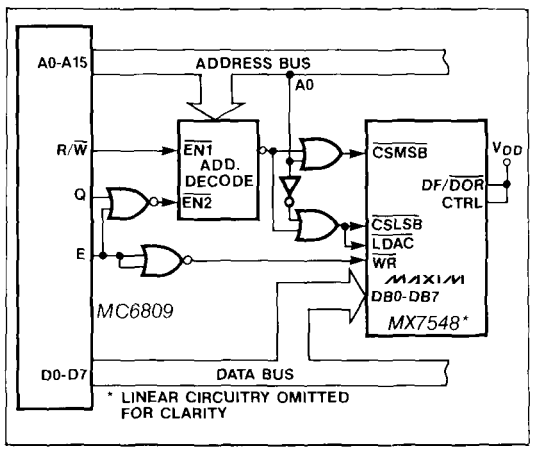


Figure 9. MX7548-MC6809 Interface (Automatic Transfer Mode)

Figure 10 shows the strobed transfer configuration with a dedicated decoder output assigned to each chip select input. The LDAC signal is common to both MX7548s and updates the DAC Registers simultaneously.

MX7548 to 8085A Interface

Figure 11 shows a typical MX7548 interface circuit to the 8085A microprocessor. Only two instructions are required to both fetch and load the 12-bit data word to the MX7548:

```
LHLD XXXX   Fetch 12-bit data
SHLD PPPP   Load 12-bit data
```

This code sequence automatically transfers 8+4-bit right-justified data, PPPP and PPPP+1, from addresses XXXX and XXXX+1. The four most significant bits occupy the lower half of XXXX+1. Address PPPP selects CSLSB, and PPPP+1 selects both CSMSB and LDAC control inputs transferring data into the AD7548 using the automatic transfer mode.

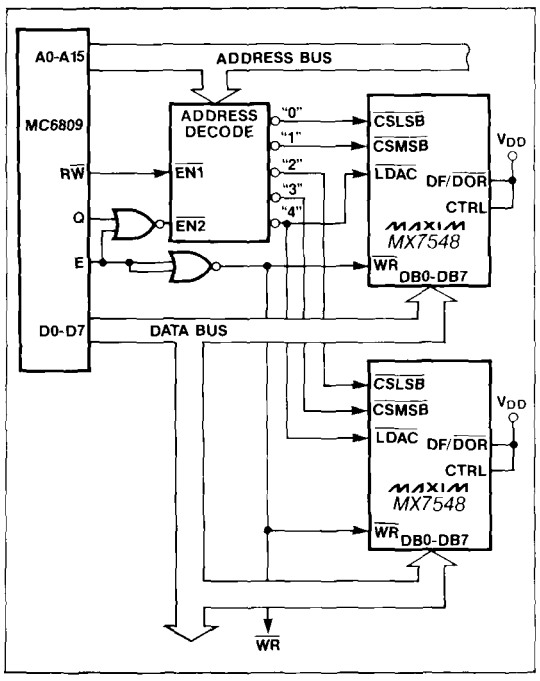


Figure 10. MX7548-MC6809 Interface (Strobed Transfer Mode)

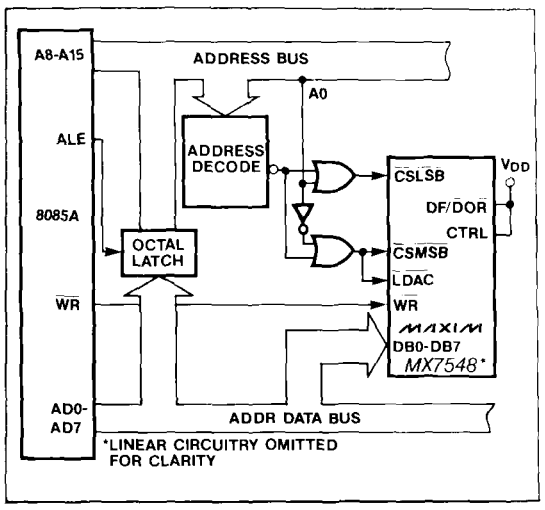


Figure 11. MX7548-8085A Interface (Automatic Transfer Mode)

Application Information

Output Amplifier Offset

For best linearity, OUT1 and AGND should be terminated at exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\ (1 + R_{FB}/R_o)$$

where V_{os} is the op amp's offset voltage and R_o is the output resistance of the DAC. R_o is a function of the digital input code and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will, therefore, degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule-of-thumb is that V_{OS} should be no more than 1/10LSBs.

The output amplifier input bias current (IB) can also limit performance since IB × R_{FB} generates an offset error. IB should, therefore, be much less than the DAC output current for 1LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended (MAX400 has 2nA max). Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor". This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic signal coupling from the V_{REF} pin to OUT1. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and OUT1 pins.

Compensation

A compensation capacitor, C1, will be needed when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT1} and the internal feedback resistor, R_{FB}. Its value depends on the type of op amp used but typically ranges from 10pF to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at OUT1 as small as possible.

Grounding and Bypassing

Since OUT1, AGND and noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low resistance (less than 0.2Ω) connection. The current at OUT1 and AGND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected as close to the DAC V_{DD} and DGND pins as possible.

The MX7548 has high impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or DGND when not used. It is also a good practice to connect active inputs to V_{DD} or DGND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

It is also recommended that two back-to-back diodes be connected between the DGND and AGND pins in those systems where these pins tie on the backplane, or these pins must be tied together to avoid AC or transient voltages between AGND and DGND from injecting noise into the analog output, OUT1.

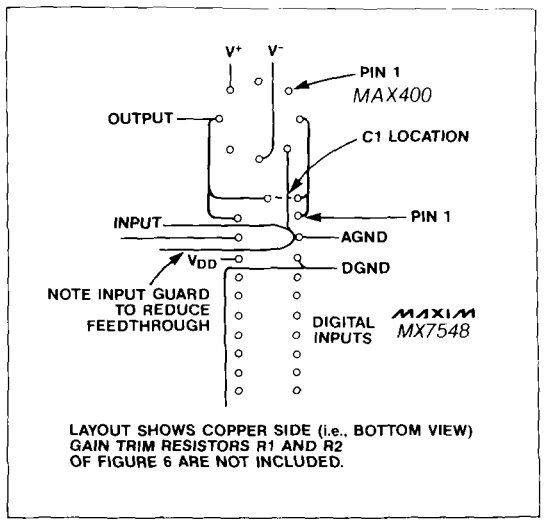
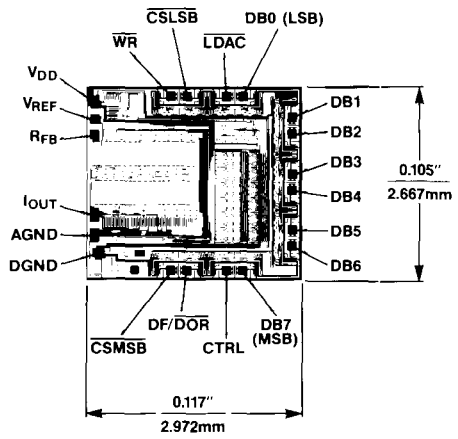
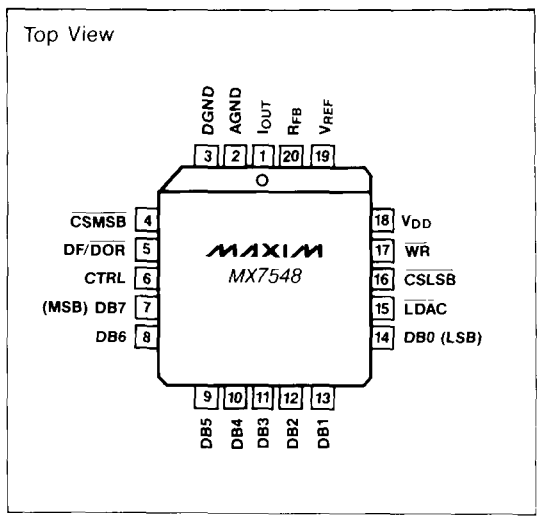


Figure 14. Suggested Layout for MX7548 and Op Amp

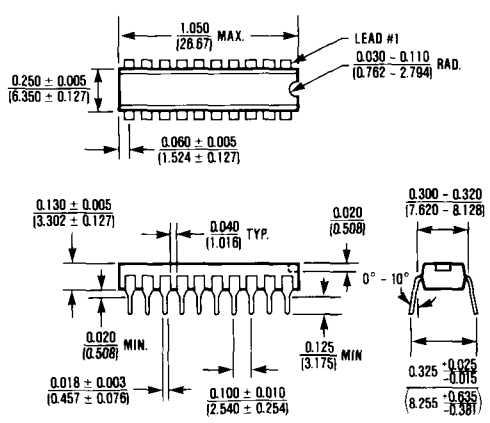
Chip Topography



Pin Configuration (continued)



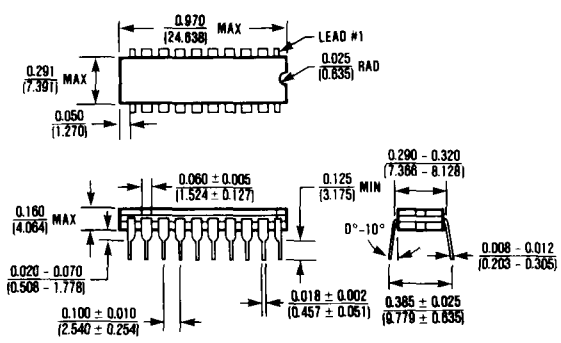
Package Information



20 Lead Plastic DIP (PP)

θ_{JA} = 125°C/W

θ_{JC} = 60°C/W

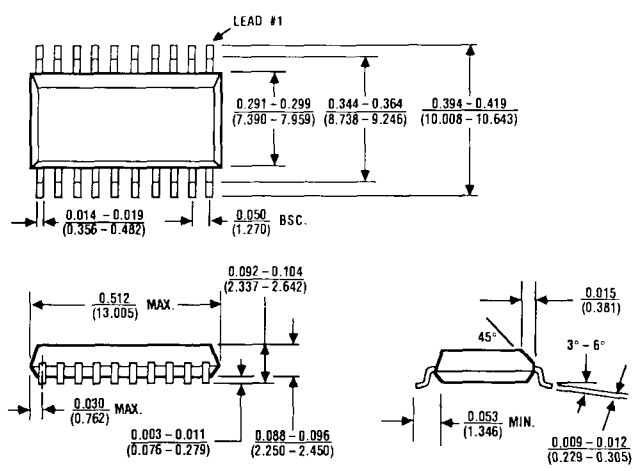


20 Lead CERDIP (JP)

θ_{JA} = 90°C/W

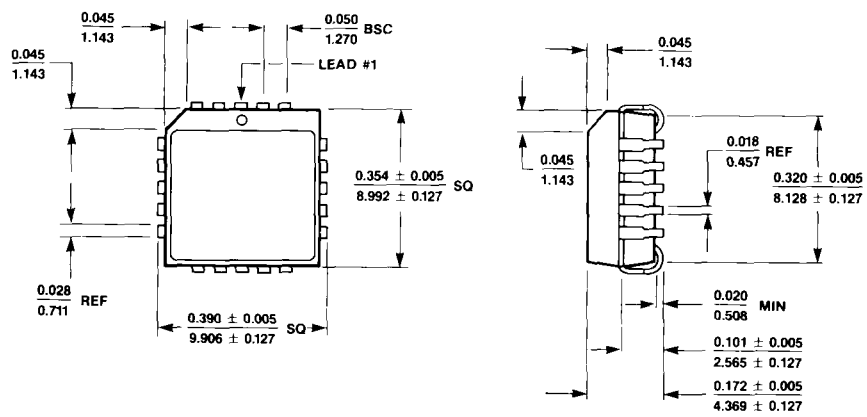
θ_{JC} = 40°C/W

Package Information (continued)



20 Lead Small Outline, Wide (WP)

θ_{JA} = 100°C/W
θ_{JC} = 50° C/W



20 Lead Plastic Chip Carrier (Quad Pak) (QP)

θ_{JA} = 110°C/W
θ_{JC} = 50° C/W

 Printed USA 19-827 1/89