DESCRIPTION

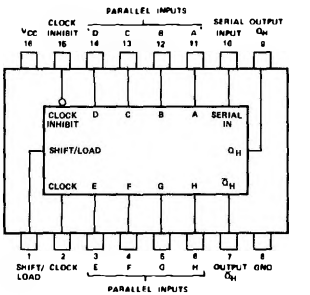
The S54165 and N74165 are 8-bit serial shift registers that shift data to the right when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

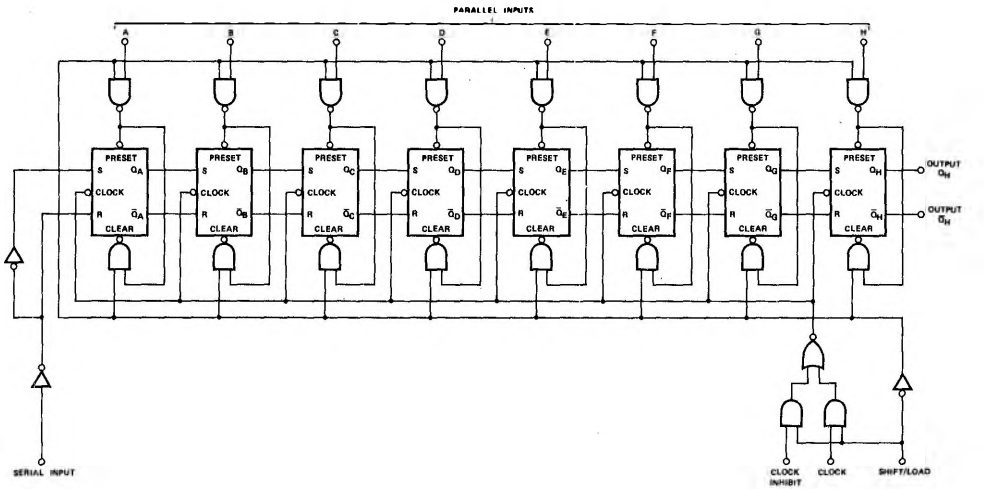
All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 210 milliwatts and maximum input clock frequency is typically 26 megahertz. The S54165 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74165 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		S54165			N74165			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	High logic level			20			20	
	Low logic level			10			10	
Input Clock Frequency, f_{clock}		0		20	0		20	MHz
Width of Clock Input Pulse, $t_{w(clock)}$		25			25			ns
Width of Load Input Pulse, $t_{w(load)}$		15			15			ns
Clock-Enable Setup Time, t_{setup}		30			30			ns
Parallel Input Setup Time, t_{setup}		10			10			ns
Serial Input Setup Time, t_{setup}		20			20			ns
Shift Setup Time, t_{setup}		45			45			ns
Hold Time at any Input, t_{hold}		0			0			ns
Operating Free-Air Temperature, T_A		−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER			TEST CONDITIONS *	S54165			N74165			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			− 1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	Load Input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Load input	V_{CC} = MAX, V_I = 0.4 V			-3.2			-3.2	mA
		Other inputs				-1.6			-1.6	
I_{OS}	Short-circuit output current †		V_{CC} = MAX	-20		-55	-18		-55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note		42	63		42	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω,	20	26		MHz
t_{PLH}	Load	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any			16	27	ns
t_{PHL}					21	34	
t_{PLH}	H	Q_H			11	20	ns
t_{PHL}					24	36	
t_{PLH}	H	$\overline{Q}_H$			18	27	ns
t_{PHL}					18	27	

NOTE : With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5 V, T_A = 25°C.

† Not more than one output should be shorted at a time.

f_{max} ≡ Maximum input count frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output