

S54H74
N74H74

DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS

These circuits are fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify systems design. A full fan-out to 10 normalized Series 54H/74H loads is available from each of the outputs in the low-level condition. In the high-level state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 35 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

LOGIC

NOTES:

1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

H = High Level, L = Low Level

The timing diagram shows the following signal levels over 7 clock cycles:

Signal	1	2	3	4	5	6	7
PRESET	14	13	12	11	10	9	8
Q	14	13	12	11	10	9	8
GND	14	13	12	11	10	9	8
CLEAR	14	13	12	11	10	9	8

The diagram also shows the internal state of the ALU (Q, Q-bar, G, G-bar) and the output of the ALU (Q, Q-bar) over 7 clock cycles. The ALU is initialized to 14 (1111) and then cleared to 0 (0000) at clock cycle 4. The output of the ALU is shown as Q and Q-bar, which are the complement of each other.

Timing diagram for the 74181 ALU. The diagram shows two 74181 chips. The first chip has CLEAR (pin 14) connected to input 14, CLOCK (pin 10) connected to input 10, and PRESET (pin 9) connected to input 9. The second chip has PRESET (pin 14) connected to input 14, CLOCK (pin 10) connected to input 10, and CLEAR (pin 9) connected to input 9. The GND pin (pin 7) is connected to input 7.

- Low input to preset sets Q to high level
- Low input to clear sets Q to low level
- Preset and clear are independent of clock

NOTE: Component values shown are nominal.

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RECOMMENDED OPERATING CONDITIONS

	S54H74			N74H74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N							
Low Logic Level			10			10	
High Logic Level			20			20	
Clock Frequency, f_{clock}	0		35 [†]	0		35	MHz
Width of Clock Pulse, $t_w(clock)$	15 [†]			15 [†]			ns
Width of Preset Pulse, $t_w(preset)$	25 [†]			25 [†]			ns
Width of Clear Pulse, $t_w(clear)$	25 [†]			25 [†]			ns
Input Setup Time, t_{setup} (See Note 3):							
High-level data	10 [†]			10 [†]			ns
Low-level data	15 [†]			15 [†]			ns
Input Hold Time, t_{hold} (See Note 4)	0			0			ns
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

NOTES:

3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

[†] These conditions are recommended for use at $V_{CC} = 5V$, $T_A = 25^\circ C$.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	$V_{CC} = MIN$, $I_{OH} = -1mA$	2.4	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = MIN$, $I_{OL} = 20mA$		0.22	0.4	V
I_{IH} High-level input current into D	$V_{CC} = MAX$, $V_I = 2.4V$			50	μA
I_{IH} High-level input current	$V_{CC} = MAX$, $V_I = 5.5V$			1	mA
I_{IH} High-level input current into preset or clock	$V_{CC} = MAX$, $V_I = 2.4V$			100	μA
I_{IH} High-level input current	$V_{CC} = MAX$, $V_I = 5.5V$			1	mA
I_{IH} High-level input current into clear	$V_{CC} = MAX$, $V_I = 2.4V$			150	μA
I_{IH} Low-level input current into preset or D	$V_{CC} = MAX$, $V_I = 5.5V$			1	mA
I_{IL} Low-level input current into preset or D	$V_{CC} = MAX$, $V_I = 0.4V$			-2	mA
I_{IL} Low-level input current into clear or clock	$V_{CC} = MAX$, $V_I = 0.4V$			-4	mA
I_{OS} Short circuit output current [†]	$V_{CC} = MAX$	-40		-100	mA
I_{CC} Supply current	$V_{CC} = MAX$, S54H74		30	42	mA
	N74H74		30	50	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		35	43		MHz
t_{PLH} Propagation delay time, low-to-high-level output, from clear or preset inputs				20	ns
t_{PHL} Propagation delay time, high-to-low-level output, from clear or preset inputs	$C_L = 25pF$, $R_L = 280\Omega$			30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock input		4	8.5	15	ns
t_{PHL} Propagation delay time, high-to-low-level output, from clock input		7	13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

[†] Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.