

8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5018

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to $\pm 1/2$ LSB (.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 6800 and many other μ P's

APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

BLOCK DIAGRAM

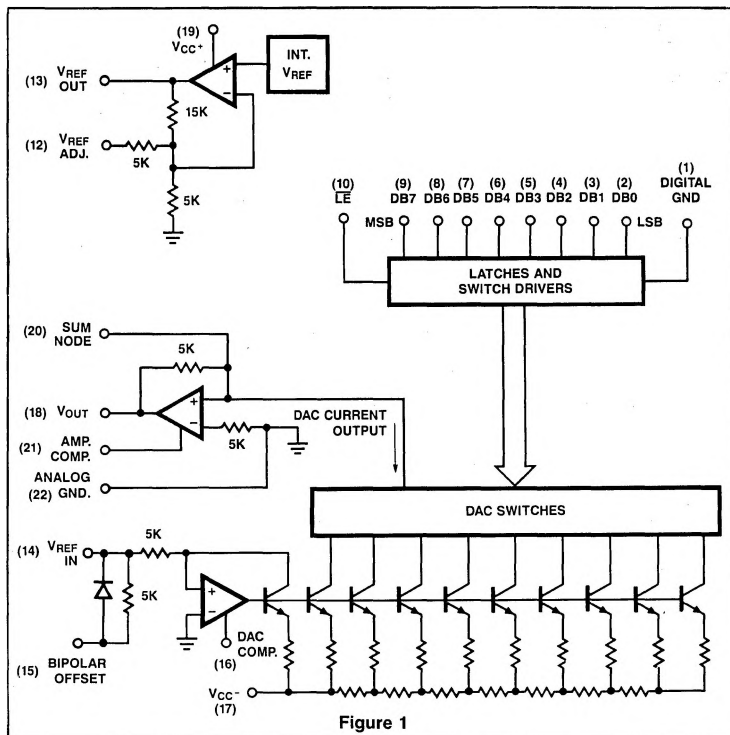
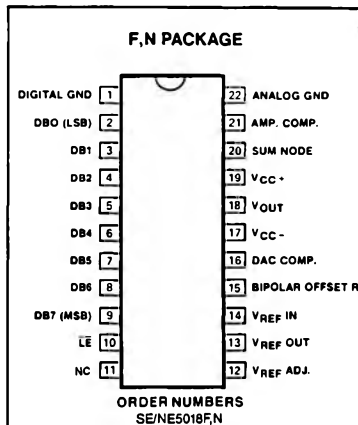
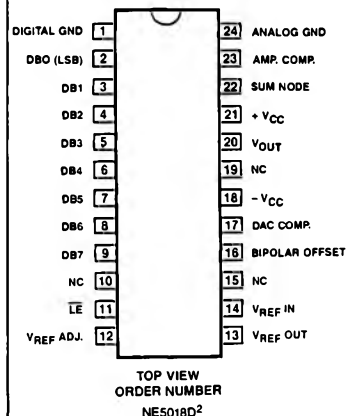


Figure 1

PIN CONFIGURATION



D² PACKAGE



NOTES:

1. SOL-Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC+} Positive supply voltage	18	V
V_{CC-} Negative supply voltage	-18	V
V_{IN} Logic input voltage	0 to 18	V
V_{REFIN} Voltage at V_{REF} input	12	V
V_{REFADJ} Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM} Voltage at sum node	12	V
I_{REFSC} Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC} Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D Power dissipation*		
-N package	800	mW
-F package	1000	mW
T_A Operating temperature range		
SE5018	-55 to +125	°C
NE5018	0 to +70	°C
T_{STG} Storage temperature range	-65 to +150	°C
T_{SOLD} Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5018. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$,
 NE5018. $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified!
 Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5018			NE5018			UNIT
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Relative accuracy				± 0.19			± 0.19	%FS
V_{CC+} Positive supply voltage		11.4	15		11.4	15		V
V_{CC-} Negative supply voltage		-11.4	-15		-11.4	-15		V
$V_{IN(1)}$ Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$ Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$ Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$ Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		-2.0	-10		-2.0	-10	μA
V_{FS} Full scale output voltage	Unipolar operation $V_{REF IN} = 5.000V$, $T_A = 25^{\circ}C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS} Full scale output voltage	Bipolar operation $V_{REF IN} = 5.000V$, $T_A = 25^{\circ}C$	4.5	+4.961	5.5	4.5	+4.961	5.5	V
V_{ZS} Zero scale voltage		-5.04	-5.000	-4.960	-5.04	-5.000	-4.960	V
		-30	5	+30	-30	5	+30	mV
I_{OS} Output short circuit current	$T_A = 25^{\circ}C$ $V_{OUT} = 0V$		15	40		15	40	mA
$PSR^{+}(out)$ Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF IN} = 5.000V$		.001	.01		.001	.01	%FS / %VS
$PSR^{-}(out)$ Output power supply rejection (-)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF IN} = 5.000V$		.001	.01		.001	.01	%FS / %VS
TC_{FS} Full scale temperature coefficient	$V_{REF IN} = 5.000V$		20			20		ppm/°C
TC_{ZS} Zero scale temperature coefficient			5			5		ppm/°C

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DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5018, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$,
NE5018, $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.¹
Typical values are specified at $25^{\circ}C$

PARAMETER	TEST CONDITIONS	SE/5018			NE5018			UNIT
		Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current			3			3	mA
I_{REFSC}	Reference short circuit current		15	30		15	30	mA
$PSR^{+}(REF)$	Reference power supply rejection (+)	Note 8 $T_A = 25^{\circ}C$ $V_{REF OUT} = 0V$						%VR/ %VS
$PSR^{-}(REF)$	Reference power supply rejection (-)							%VR/ %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$						V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$						ppm/ $^{\circ}C$
Z_{IN}	DAC V_{REF} IN input impedance	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$						K Ω
I_{CC+}	Positive supply current	$V_{CC+} = 15V$						mA
I_{CC-}	Negative supply current	$V_{CC-} = -15V$						mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$						mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS² $V_{CC} = \pm 15V$, $T_A = 25^{\circ}C$

PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
				Min	Typ	Max	
T_{SLH}	Settling time	$\pm \frac{1}{2}$ LSB	Input		1.8		μs
T_{SHL}	Settling time	$\pm \frac{1}{2}$ LSB	Input		2.3		μs
t_{plh}	Propagation delay	Output	Input		300		ns
t_{phl}	Propagation delay	Output	Input		150		ns
t_{plsb}	Propagation delay	Output	Input		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100		ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50		ns
t_{pw}	Latch enable pulse width			2, 7	150		ns

NOTES

2. Refer to Figure 3.

3. See Figure 6.

4. See Figure 7.

5. See Figure 8.

6. See Figure 9.

7. See Figure 10.

8. For reference currents $> 3mA$, use of an external buffer is required.

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DC PARAMETRIC TEST CONFIGURATION

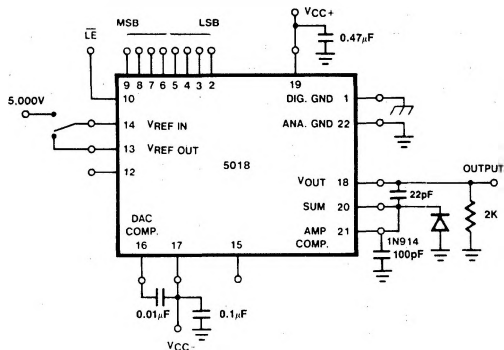


Figure 2

AC PARAMETRIC TEST CONFIGURATION

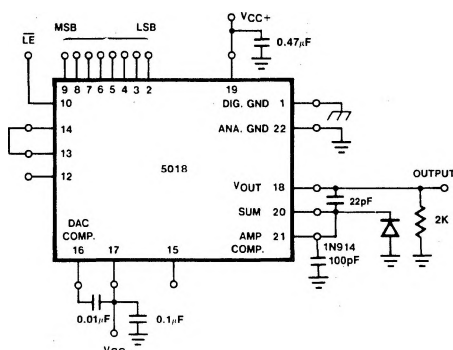


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

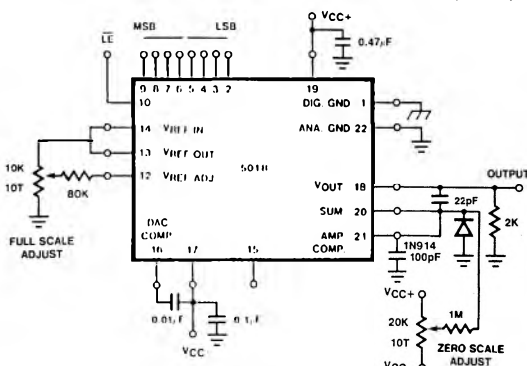


Figure 4

BIPOLAR OUTPUT OPERATION (-5 to +5V)

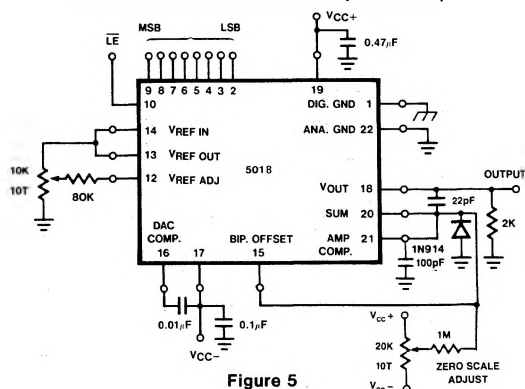


Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

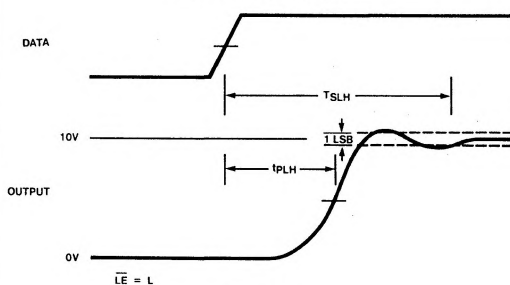


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

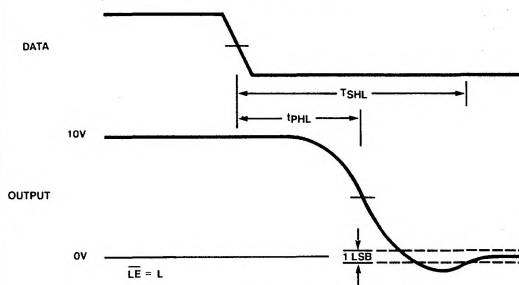


Figure 7

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