Signetics

NE5036
6-Bit A/D Converter (Serial Output)

Product Specification

Linear Products

DESCRIPTION

The NE5036 is an easy-to-use, low cost, successive-approximation Analog-to-Digital converter, fabricated in Bipolar/I^2L technology, and packaged in a convenient 8-pin miniDIP package.

With an external reference voltage, the NE5036 will accept input voltages between 0V and V_{REF}. Holding the $\overline{START}$ pin low for at least 8 clock pulses in duration will provide the 6-bit result of the conversion in a serial format.

FEATURES

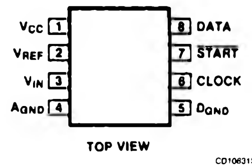
- **Three-state output buffer for easy microprocessor interfacing**
- **Fast successive-approximation converter, 23μs**
- **TTL compatible inputs and outputs**
- **Easy interface to CMOS microprocessors**
- **Guaranteed no missing codes over full operating range**
- **Single supply operation, +5V**
- **High impedance analog inputs**
- **Positive true binary serial output**

APPLICATIONS

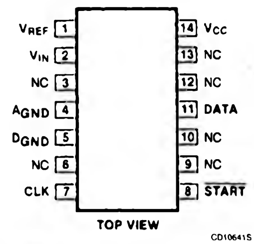
- **Temperature control**
- **μP-based appliances**
- **Light level monitor**
- **Electronic toys**
- **Joystick interface**
- **μP/transducer interface**

PIN CONFIGURATIONS

FE, N Packages



D[1] Package

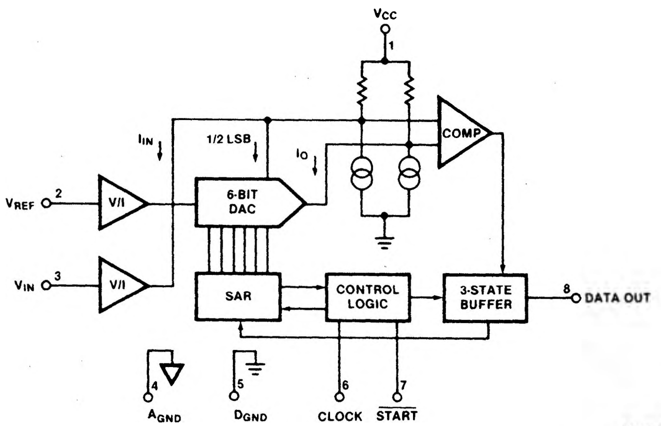


NOTE:
1. SO and non-standard pinouts.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	0 to +70°C	NE5036FE
8-Pin Plastic DIP	0 to +70°C	NE5036N
14-Pin SO Package	0 to +70°C	NE5036D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\ (Analog)}$	Analog input voltage	7	V
$V_{IN\ (Digital)}$	Digital input voltage ($\overline{START}$ & CLOCK)	7	V
D_{OUT}	Data output pin 3-State mode Enabled mode	 7 20	 V mA
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] FE package N package D package	 780 1160 1090	 mW mW mW

NOTE:
1. Derate above 25°C at the following rates:
   FE package at 6.0mW/°C.
   N package at 9.3mW/°C.
   D package at 8.3mW/°C.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 350kHz; 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution Relative accuracy[1, 2]		6	6 ¼	6 ½	Bits LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS} ϵ_{ZS}	Full-scale gain error[2, 3, 4] Zero-scale offset error[2]	V_{REF} = 2.0V, T_A = 25°C V_{REF} = 2.0V, T_A = 25°C		±1 ±½	±2 -½, +2	LSB LSB
PSR	Power supply rejection Max change in full-scale[2]	V_{REF} = 2.0V 4.75V ≤ V_{CC} ≤ 5.5V		±½	±1	LSB
I_{IN} I_{REF} R_{IN}	Analog input bias current Reference bias current Analog input resistance	0 ≤ V_{IN} ≤ 2.5V 0 ≤ V_{REF} ≤ 2.5V	 3	1 1 30	10 10	µA µA MΩ
V_{IH} V_{IL} I_{IH} I_{IL} I_{OH} I_{OL} I_{OZ} I_{CC}	Logic '1' input voltage Logic '0' input voltage Logic '1' input current Logic '0' input current Logic '1' output current Logic '0' output current Three-state leakage current Positive supply current	 2.4V ≤ V_{OH} V_{OL} ≤ 0.4V	2.0 300 1.6	 1 ±0.1 14	 0.8 10 10 ±40 24	V V µA µA µA mA µA mA
P_D	Power dissipation				132	mW

NOTES:
1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on the straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the bit level which is 1.56% of the full-scale voltage.
3. Full-scale gain error is the deviation of the code transition point (111110 to 111111) from its ideal value (accounting for offset error at 000000).
4. The analog input voltage (V_{IN}) range is from 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance V_{REF} can be any value from 1.5V to 2.5V.)

6-Bit A/D Converter

NE5036

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 350kHz; 0°C $\leqslant T_A \leqslant$ 70°C unless otherwise specified. Typical values are specified at 25°C. (Refer to test figures.)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Max clock frequency			50% duty cycle	350			kHz
t_{CONV}	Conversion time						8	Clock cycles
t_W	Clock pulse width[3]				1.3			μs
t_S	Setup time, $\overline{\text{START}}$ to clock[2]	Clock	$\overline{\text{START}}$		500			ns
$t_{P\ (OUT)}$	Propagation delay[1]	Data out	Clock	T_A = 25°C, $t_R = t_F$ < 20ns			600	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay[1]	Data (3-State)	$\overline{\text{START}}$	T_A = 25°C, $t_R = t_F$ < 20ns			600	ns

NOTES:
1. The time between the specified reference points on the clock and the output waveforms with the output changing (Low-to-High or High-to-Low).
2. The High-to-Low transition of the $\overline{\text{START}}$ pulse should occur at least 500ns prior to the negative edge of the clock pulse to insure its recognition. The $\overline{\text{START}}$ pulse should stay high for at least 500ns between conversions to guarantee proper recognition.
3. Negative or positive.

CIRCUIT DESCRIPTION

NE5036 is a complete 6-bit, serial output, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and the output buffer. An externally-generated clock source (maximum frequency = 350kHz) must be provided to Pin 6. An external reference voltage supplied to Pin 2 sets the full-scale range of the A/D converter as shown in the Block Diagram.

Upon the $\overline{START}$ pin going low, successive approximation conversion commences after the first low-going edge of the clock pulse. Successive bits, beginning with the MSB (D5), are applied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to 0 and simultaneously the output buffer goes to 0. If it is less, that bit stays at 1 and the output buffer goes to 1. After the second High-to-Low transition of the clock pulse, the MSB (D5) data is valid. On successive clock pulses, successive bits are tried and the output buffer represents that bit. $\overline{START}$ has to stay low for at least 8 clock pulses for the conversion to be completed and to access the 6-bit result of the conversion. A conversion in process can be interrupted by issuing another $\overline{START}$ pulse.

When $\overline{START}$ is in a high state, the output buffer is in a high impedance state.

The timing diagram for the device is shown in Figure 1.

TRANSFER CHARACTERISTICS

The NE5036 is designed to have a nominal ½ LSB offset, so that the code transition points are located ½ LSB on either side of the exact analog input for a given code. Thus, the first transition (000000 to 000001) will occur at an input of ½ LSB (15.63mV with a V_{REF} of 2.0V), plus any offset. Subsequent transition (to full-scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

The ideal transfer characteristic of NE5036 is shown in Figure 2.

LAYOUT PRECAUTIONS

Analog ground (Pin 4) and Digital ground (Pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The leads to the analog inputs should be kept as short as possible to minimize input noise pick-up. Input bypass capacitors from the analog inputs to ground will eliminate noise pick-up. Power supplies should be decoupled with at least 1µF and should be located close to the device to minimize the effects of noise spikes on V_{CC}.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance at these inputs at or below 2kΩ.

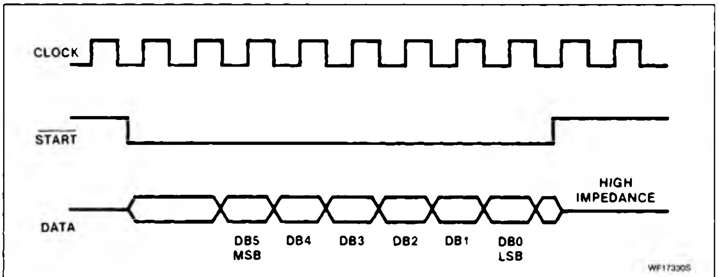


Figure 1. Timing Diagram

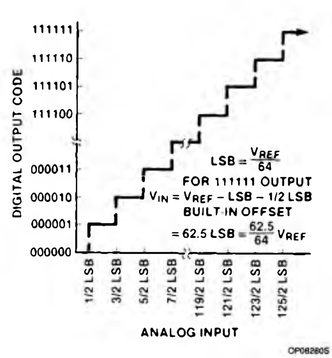
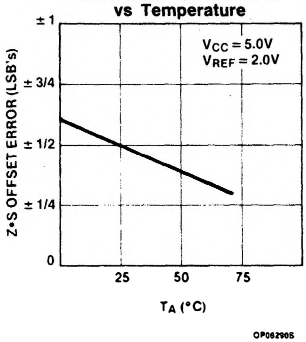


Figure 2. Ideal Transfer Characteristics

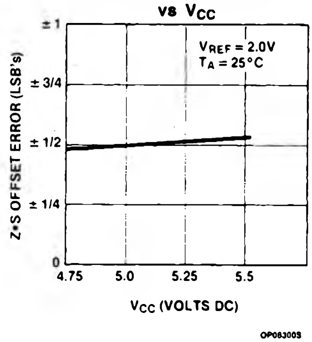
6-Bit A/D Converter NE5036

TYPICAL PERFORMANCE CHARACTERISTICS

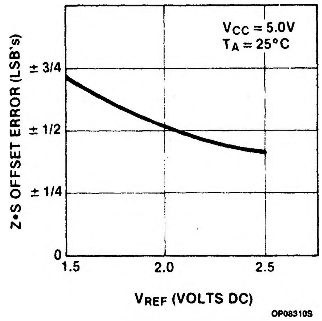
Zero-Scale Offset Error vs Temperature



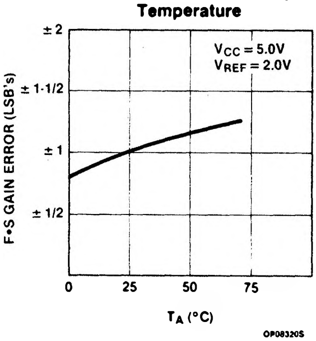
Zero-Scale Offset Error vs V_{CC}



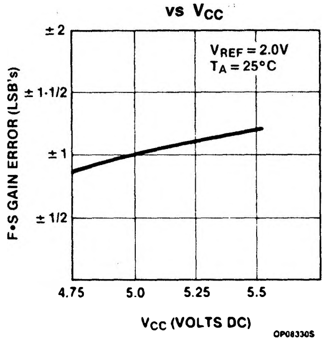
Zero-Scale Offset Error vs V_{REF}



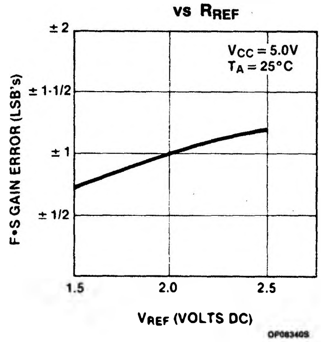
Full-Scale Gain Error vs Temperature



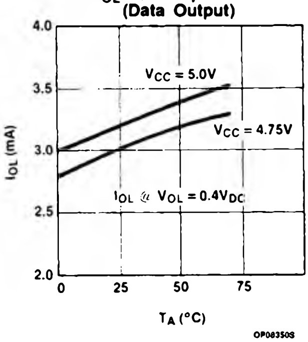
Full-Scale Gain Error vs V_{CC}



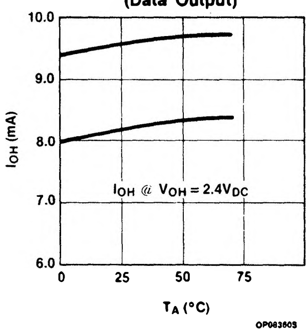
Full-Scale Gain Error vs R_{REF}



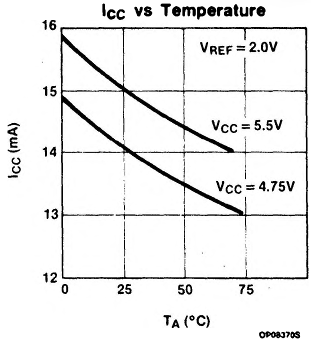
I_{OL} vs Temperature (Data Output)



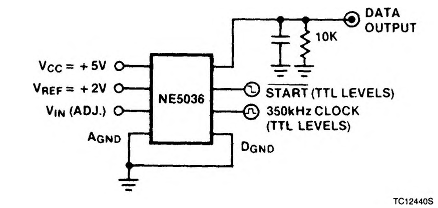
I_{OH} vs Temperature (Data Output)



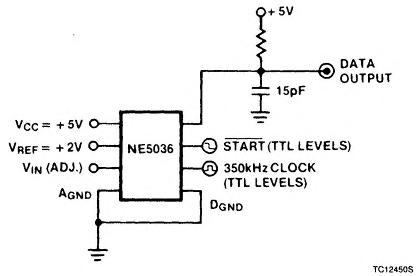
I_{CC} vs Temperature



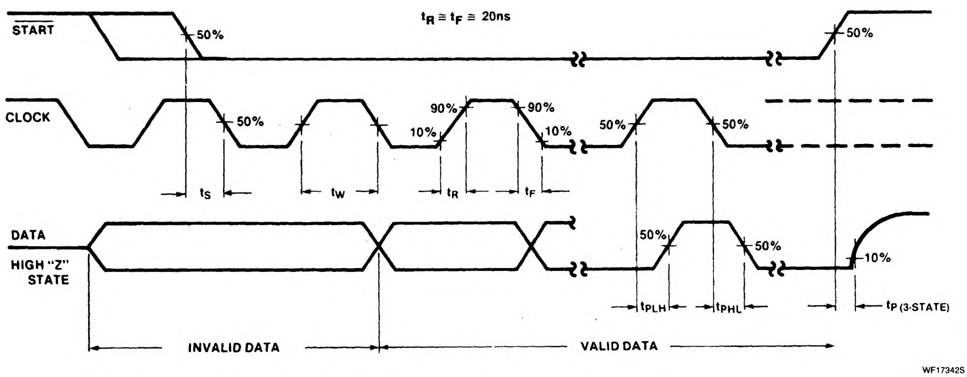
AC TEST CIRCUITS AND WAVEFORMS



Data Output (Low-to-High)



Data Output (High-to-Low)



Propagation Delay Time t_P (Data)

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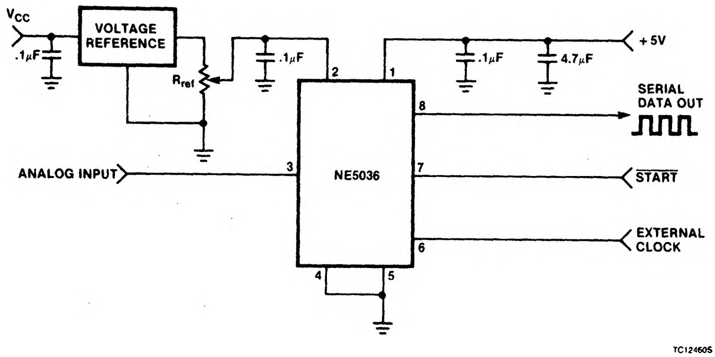
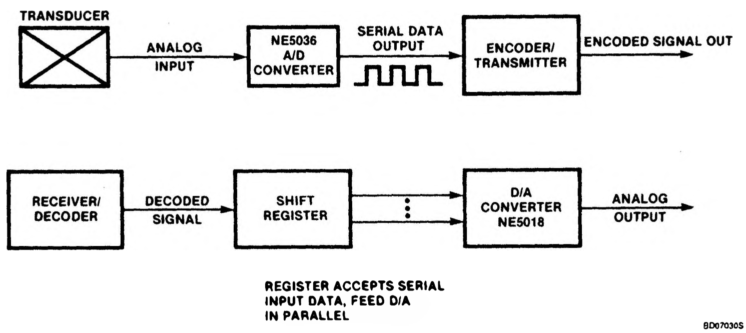
TYPICAL APPLICATIONS



1. Basic NE5036 Configuration



2. Digital Communications Using NE5036