6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

DESCRIPTION

The NE5037 is a low cost, complete successive approximation analog to digital (A/D) converter, fabricated in Bipolar/I^2L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9μs.

FEATURES

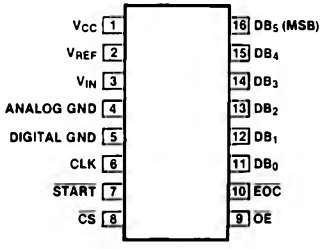
- **T^2L compatible inputs and outputs**
- **Three state output buffer**
- **Easy interface to CMOS μProcessors**
- **Fast conversion—9μs**
- **Guaranteed no missing codes over full temp range**
- **Single supply operation, +5V**
- **Positive true binary outputs**
- **High impedance analog inputs**

APPLICATIONS

- **Temperature control**
- **μP-based appliances**
- **Light level monitors**
- **Head position sensing**
- **Electronic toys**
- **Joystick interface**

PIN CONFIGURATION

D, F, N PACKAGE



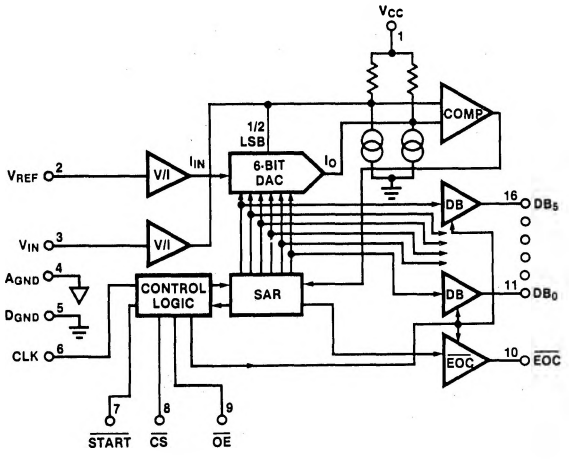
TOP VIEW

ORDER NUMBERS
NE5037F, NE5037N
NE5037D

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\ (Analog)}$	Analog input voltage	7	V
$V_{IN\ (Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5)		
	Three-state mode	7	V
	Enabled mode (each output)	5	mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	−65 to 150	°C
t_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Power dissipation		
	F package	220	mW
	N package	220	mW

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C.

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full scale gain error[2,3,4]	V_{REF} = 2.0V, T_A = 25°C		±1	±2	LSB
ϵ_{ZS}	Zero scale offset error[2]	V_{REF} = 2.0V, T_A = 25°C		±1/2	−1/2, +2	LSB
P_{SR}	Power supply rejection	V_{REF} = 2.0V		±1/2	±1	LSB
	Max change in full scale[2]	4.75V ≤ V_{CC} ≤ 5.5V				
I_{IN}	Analog input bias current	0 ≤ V_{IN} ≤ 2.5V		1	10	μA
I_{REF}	Reference bias current	0 ≤ V_{REF} ≤ 2.5V		1	10	μA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	μA
I_{IL}	Logic '0' input current			1	10	μA
I_{OH}	Logic '1' output current[5]	2.4V ≤ V_{OH}	300			μA
I_{OL}	Logic '0' output current[5]	V_{OL} ≤ 0.4V	1.6			mA
I_{OZ}	Three-state leakage current			±0.1	±40	μA
I_{CC}	Positive supply current			18	24	mA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C. (Refer to AC test figures.)

SYMBOL AND PARAMETER		TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum clock frequency				1			MHz
t_W	Start pulse width				300			ns
	Minimum positive/negative clock pulse width				300			ns
T_{CONV}	Conversion time						9	Clock cycles
$t_{P\ (OUT\ DATA)}$	Propagation delay[6]	Data out	$\overline{OE}$	T_A = 25°C, t_r = t_f ≤ 20ns			500	ns
$t_{P\ (OUT\ EOC)}$	Propagation delay[7]	$\overline{EOC}$	Clock	T_A = 25°C, t_r = t_f ≤ 20ns			800	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay, 3-state	3-State Data	$\overline{OE}$	T_A = 25°C, t_r = t_f ≤ 20ns			500	ns

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSB's refer to the weight of the least significant bit at the 6 bit level which is 1.56% of the full scale voltage.
3. Full scale gain error is the deviation of the full scale code transition point (111110 to 111111) from its ideal value.
4. The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
5. The data outputs have active pull-ups. The $\overline{EOC}$ line is open collector with a nominal 5kΩ internal pull-up resistor
6. Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of $\overline{OE}$.
7. Propagation delay of $\overline{EOC}$ is defined as the delay in $\overline{EOC}$ going low, following the low going edge of the 9th clock pulse after the start pulse.

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally generated clock source (max frequency = 1MHz) must be provided to pin 6. An external reference voltage supplied to pin 2 sets the full scale range of the A/D converter.

The $\overline{CS}$ pin must be at a low level prior to the start of the conversion process. Upon receipt of a $\overline{START}$ pulse the internal control logic resets the SAR. On the first low going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB (D5) are supplied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to '0' and simultaneously the corresponding

output buffer goes to '0'. If it is less, that bit stays at '1' and the output buffer also stays at '1'. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low going edge of the clock pulse (after the receipt of the start pulse). The $\overline{EOC}$ pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the $\overline{OE}$ pin must be set to a low level. $\overline{EOC}$ is reset to a high state when $\overline{OE}$ is low. When $\overline{OE}$ is in a '1' state, the output buffers are in a high impedance state.

Refer to Figure 1 for the timing diagram.

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in Figure 2.

The NE5037 is designed to have a nominal ½ LSB offset so that the code transition points are located ½ LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of ½ LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full scale—111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (pin 4) and Digital ground (pin 5) are not connected internally and should be connected together as close to the device as possible, for optimum performance. The circuit will operate with as much as ±200mV between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pickup. Input bypass capacitors from the analog inputs to ground will eliminate noise pickup. Power supplies should be decoupled with at least 1μF located close to the device to minimize the effects of noise spikes.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance of these inputs at or below 2K-ohms.

TIMING DIAGRAM

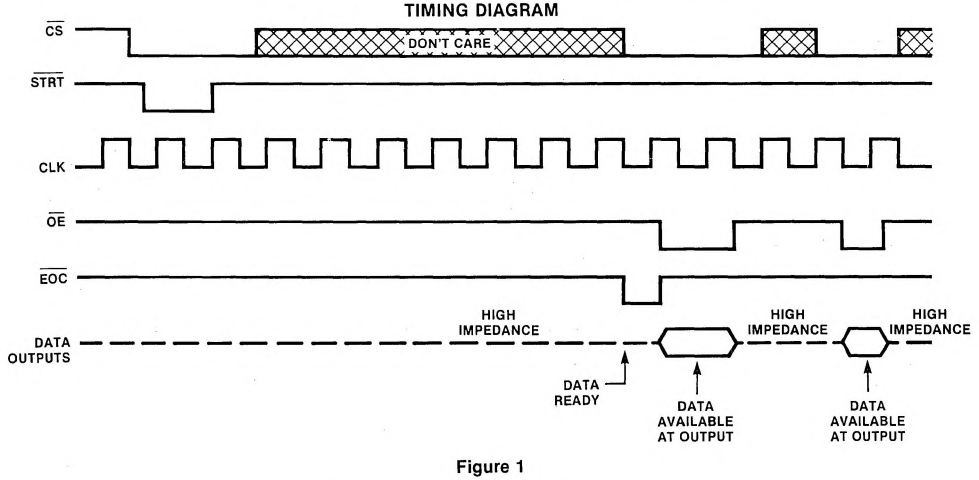


Figure 1

IDEAL TRANSFER CHARACTERISTICS

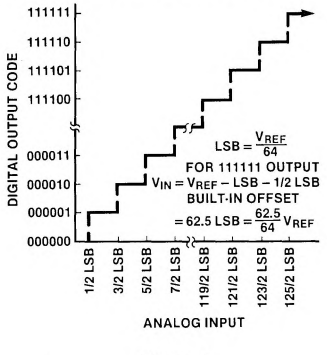
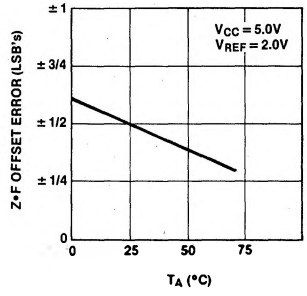


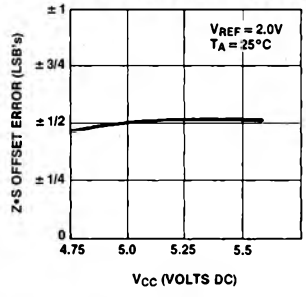
Figure 2

TYPICAL PERFORMANCE CHARACTERISTICS

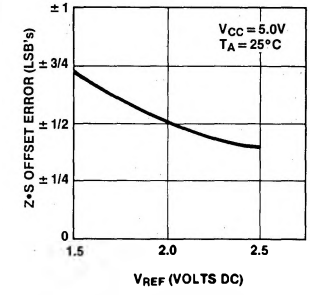
ZERO SCALE OFFSET ERROR vs TEMP



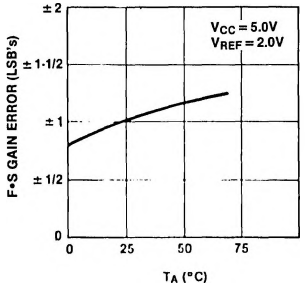
ZERO SCALE OFFSET ERROR vs V_{CC}



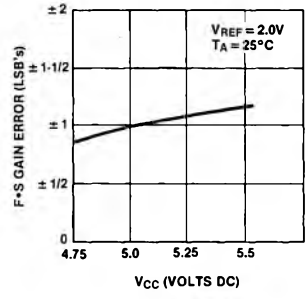
ZERO SCALE OFFSET ERROR vs V_{REF}



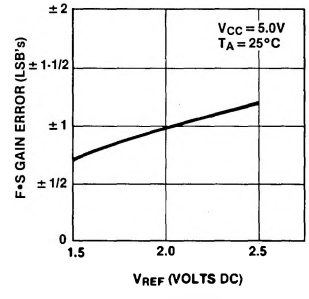
FULL SCALE GAIN ERROR vs TEMP



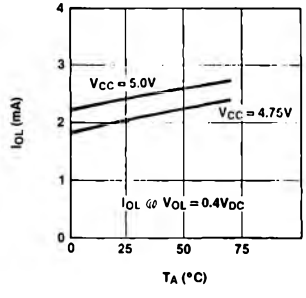
FULL SCALE GAIN ERROR vs V_{CC}



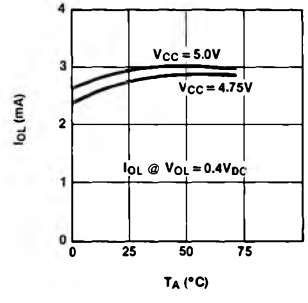
FULL SCALE GAIN ERROR vs V_{REF}



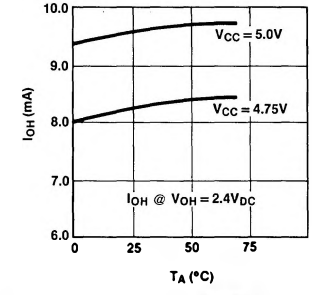
I_{OL} vs TEMP (DATA OUTPUTS)



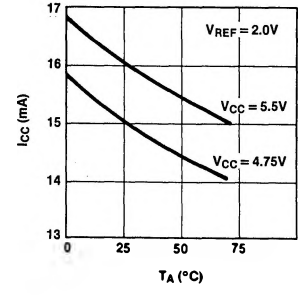
I_{OL} vs TEMP ($\overline{EOC}$)



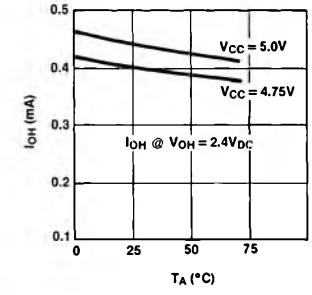
I_{OH} vs TEMP (DATA OUTPUTS)



I_{CC} vs TEMP



I_{OH} vs TEMP ($\overline{EOC}$)



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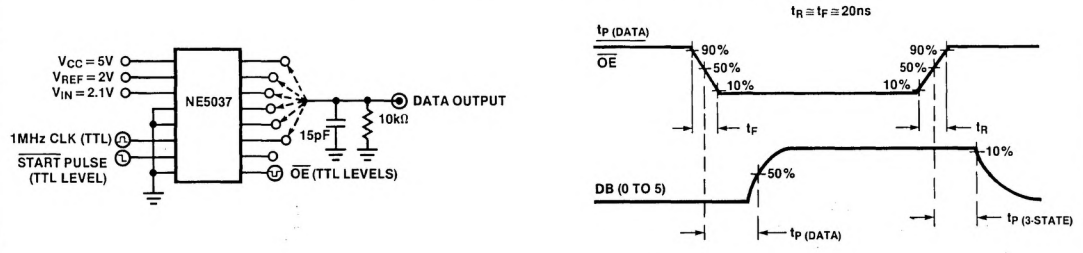
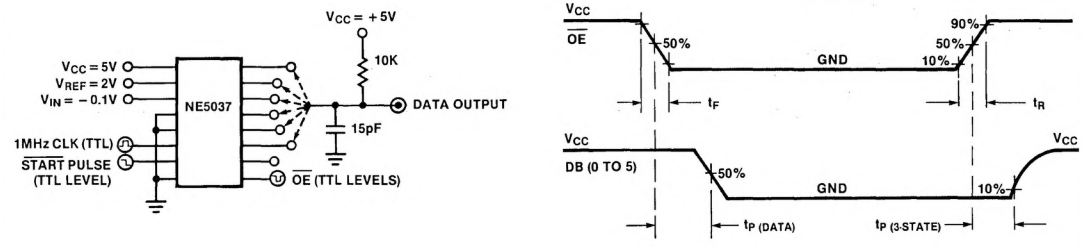
AC TEST CIRCUITS AND WAVEFORMS

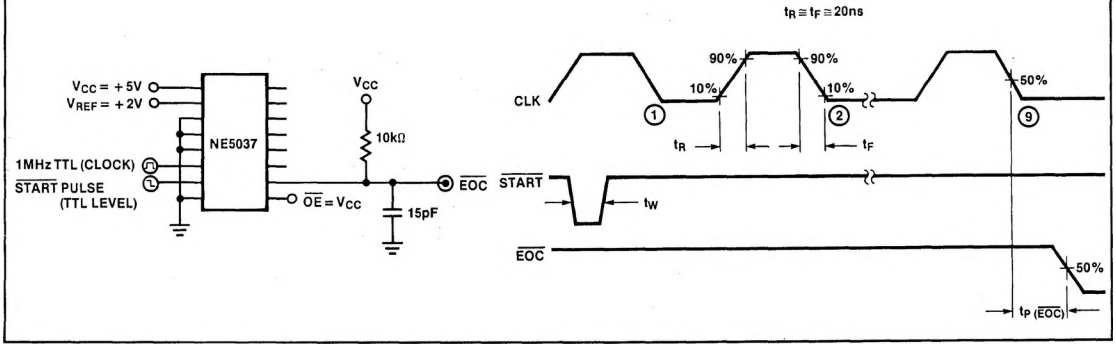
PROPAGATION DELAY TIME $t_{P\,(DATA)}$ AND $t_{P\,(3\text{-STATE})}$



DATA OUTPUT HIGH



PROPAGATION DELAY TIME EOC $t_{P\,(EOC)}$



6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

APPLICATION

- **0 to 63°C Temperature Sensor**

CIRCUIT DESCRIPTION

The temperature sensor of Figure 3A provides an input to Pin 3 of the NE5037 of 32 millivolts per degree Celsius. This 32mV is the value of one LSB for the NE5037. The LM334 is a three-terminal temperature sensor and provides a current of 1 microamp for each degree Kelvin. The 32K-ohm resistor provides the 32 millivolts for each microamp through it, while the transistor bleeds off 273 microamps of the temperature sensor (LM334) current, lowering the reading by 273 degrees Kelvin, thus converting from Kelvin to Celsius.

To read temperature, conversion is started by sending a momentary low signal to Pin 7 of the NE5037. When Pin 10 of the NE5037 goes low, conversion is complete and a low is applied to Pin 9 of the NE5037 to read data on Pins 11 through 16. Note that this temperature data is in straight binary format.

The controller can be a microprocessor in a temperature control application, or discrete circuitry in a simple temperature reporting application. A temperature reporting (digital thermometer) circuit is shown in Figure 3B. The ROMs or PROMs

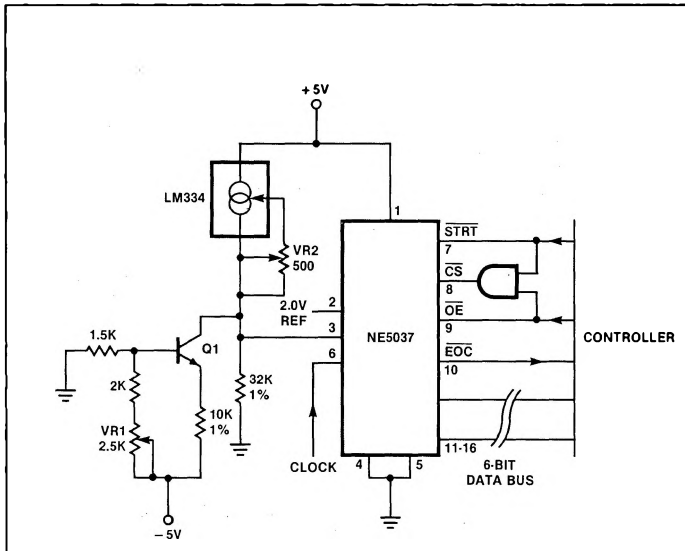


Figure 3A. Temperature Sensor

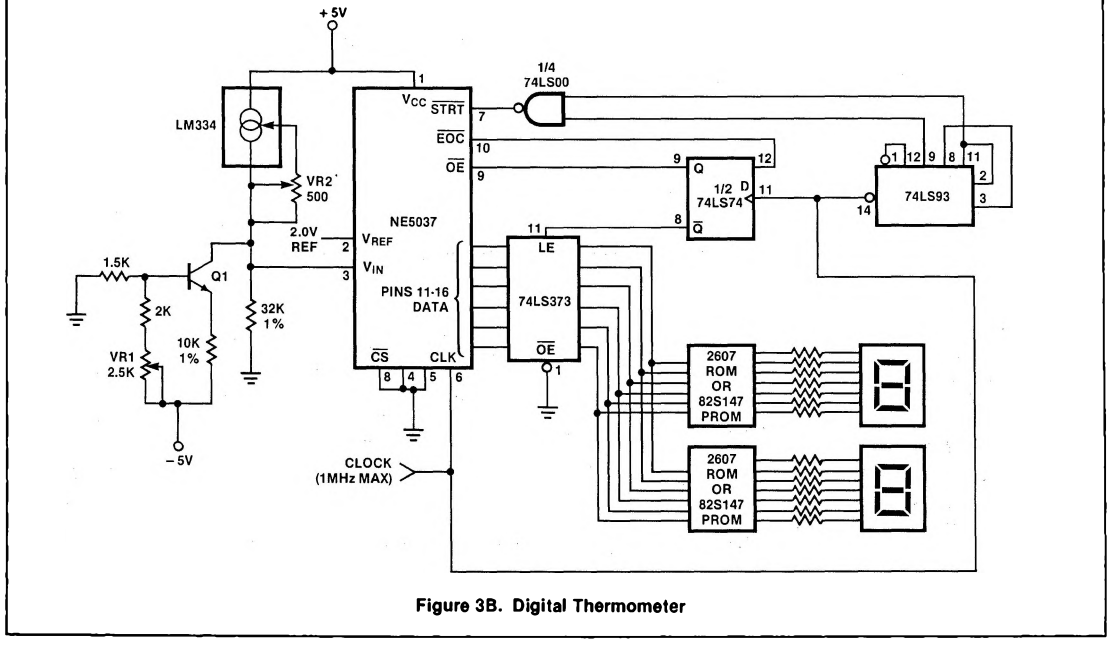


Figure 3B. Digital Thermometer

must have the correct code for converting the data from the NE5037 (used as address for the ROMs or PROMs) to the appropriate segment driver codes.

The displayed output could easily be converted to degrees Fahrenheit by the controller of Figure 3A or through the (P)ROMs of Figure 3B. When doing this, a third (hundreds) digit (P)ROM and display will, of course, be needed for displaying temperatures above 99°F.

An inexpensive clock can be made from NAND gates or inverters, as shown in Figure 3C.

CIRCUIT ADJUSTMENT

Adjust VR2 for about 1/4 of maximum resistance. With the sensor (LM334) stable at a known temperature near the lower end of the expected range of temperature readings, adjust VR1 for a drop of 2.73 volts across the (10K) emitter resistor of Q1. Set reference voltage at Pin 2 of the NE5037 for 2 volts and adjust VR2 for a digital reading corresponding to the known temperature.

Because high accuracy is not necessary in many applications, this is often all the adjustment necessary and yields an indicated temperature that is within 3 degrees Celsius of actual temperature. Should higher accuracy be required, adjustment of the NE5037 reference voltage at Pin 2 is needed. After performing the above adjustments, bring the sensor temperature to a value near the maximum expected reading (but not above 63 degrees Celsius) and adjust the reference voltage at Pin 2 of the NE5037 for a digital output indication of the known temperature. Then stabilize the sensor again at a temperature near the low end of the expected range of readings and adjust VR1 for a digital indication of that known temperature. This procedure will provide an accuracy of ±1 degree Celsius.

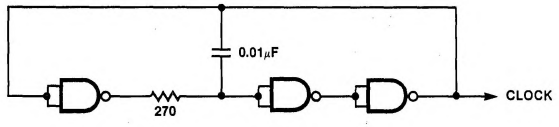


Figure 3C. Simple Clock Circuit