National Semiconductor

NM93C46A
1024-Bit Serial EEPROM
64 x 16-Bit or 128 x 8-Bit Configurable

General Description

The NM93C46A is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or 128 8-bit registers. The organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C46A is available in an SO package for space considerations.

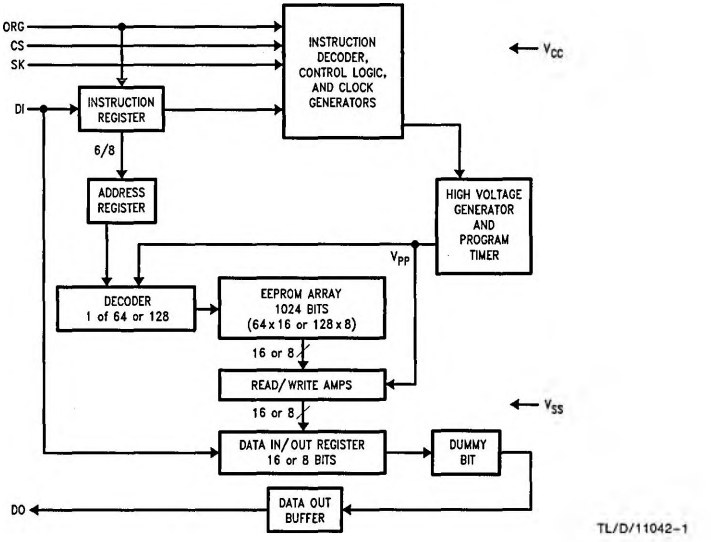
The interface that controls the EEPROM is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C46A is compatible with National Semiconductor's NM93C46 if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC} to default to the 64 x 16 configuration.

Features

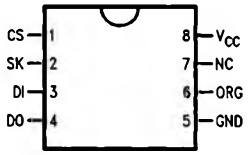
- Device status during programming mode
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



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Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46AN
NM93C46AM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C46AEN
NM93C46AEM8

Military Temp. Range (−55°C to +125°C)

Order Number
NM93C46AMN
NM93C46AMM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
EDS Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46A	0°C to +70°C
NM93C46AE	−40°C to +85°C
NM93C46AM	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% Unless Otherwise Specified

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C46A NM93C46AE NM93C46AM	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C46A NM93C46AE NM93C46AM	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM93C46A NM93C46AE NM93C46AM	CS = 0V		50 100 100	μA
I_{IL}	Input Leakage	NM93C46A NM93C46AE NM93C46AM	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NM93C46A NM93C46AE NM93C46AM	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC}+1	V
V_{OL1}	Output Low Voltage	NM93C46A NM93C46AE NM93C46AM	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NM93C46A NM93C46AE NM93C46AM		0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93C46A NM93C46AE NM93C46AM	(Note 2) (Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM93C46A NM93C46AE NM93C46AM	(Note 2) (Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup Time	NM93C46A NM93C46AE NM93C46AM	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93C46A NM93C46AE NM93C46AM	(Note 4) (Note 4) (Note 5)	250 250 500		ns

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% Unless Otherwised Specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46A NM93C46AE NM93C46AM	Relative to SK	50 50 100		ns
t_{DIS}	DI Setup Time	NM93C46A NM93C46AE NM93C46AM	Relative to SK	100 100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C46A NM93C46AE NM93C46AM	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C46A NM93C46AE NM93C46AM	AC Test		500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C46A NM93C46AE NM93C46AM	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C46A NM93C46AE NM93C46AM	AC Test CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms
t_{DH}	DO Hold Time		Relative to SK	20		ns

Capacitance (Note 6)

T_A = +25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C46A has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8/9 bits carry the op code and the 6/7-bit address for register selection.

Read (READ)

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into an 8- or 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 8- or 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN)

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE)

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE)

The Write (WRITE) instruction is followed by 8 or 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). The ERASE ALL instruction is not required, see note below.

Write All (WRAL)

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Erase/Write Disable (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Note: The NM93C46A device does not require an 'ERASE' or 'ERASE ALL' prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with the NMOS NMC9346.

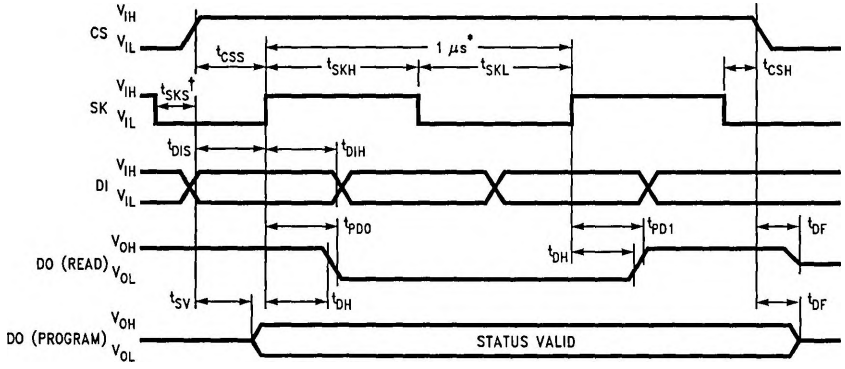
Instruction Set

Instruction	Start Bit	Opcode		Address*		Data		Comments
				128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1	0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1	1	A6–A0	A5–A0			Erase Address AN–A0
WRITE	1	0	1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0	0	11XXXXX	11XXXX			Program Enable
EWDS	1	0	0	00XXXXX	00XXXX			Program Disable
ERAL	1	0	0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0	0	01XXXXX	01XXXX	D7–D0	D15–D0	Program All Addresses

*It is necessary to clock in the "Don't Care" Address Bits.

Timing Diagrams

Synchronous Data Timing



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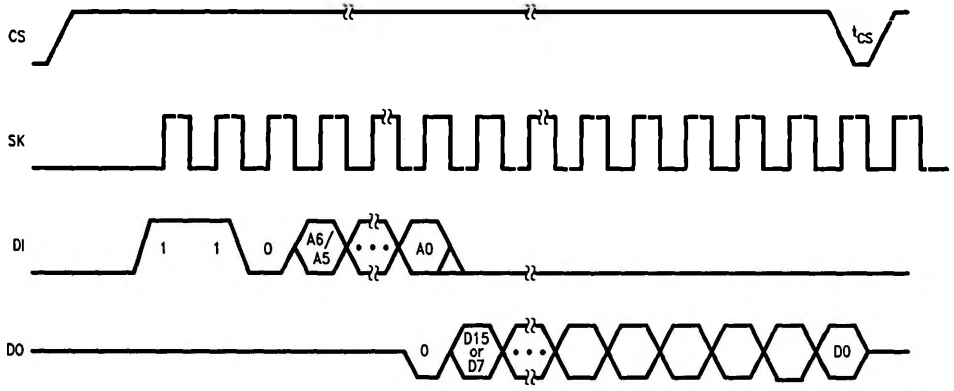
*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ



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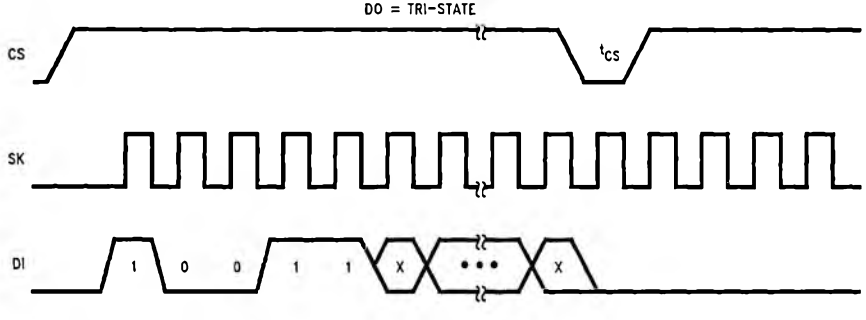
EWEN†



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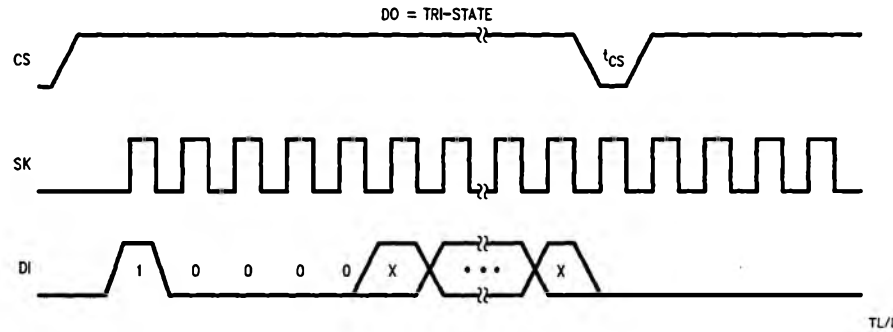
†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

Timing Diagrams (Continued)

EWDS†



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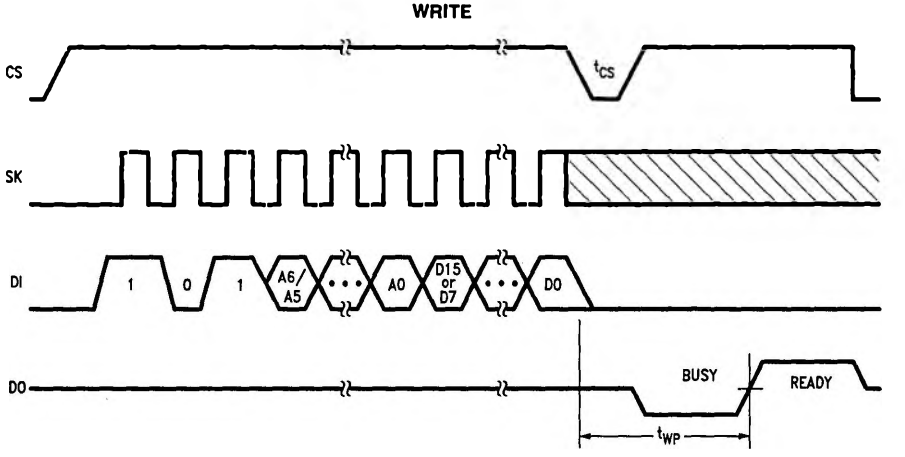
WRITE



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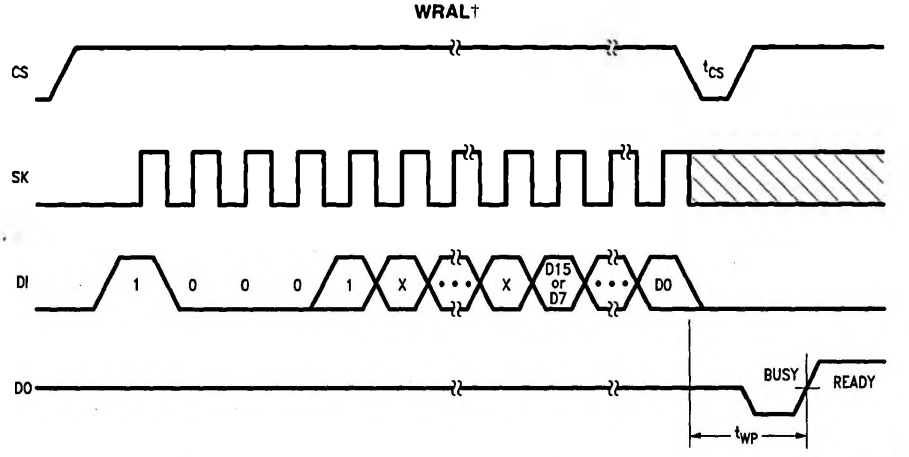
WRAL†



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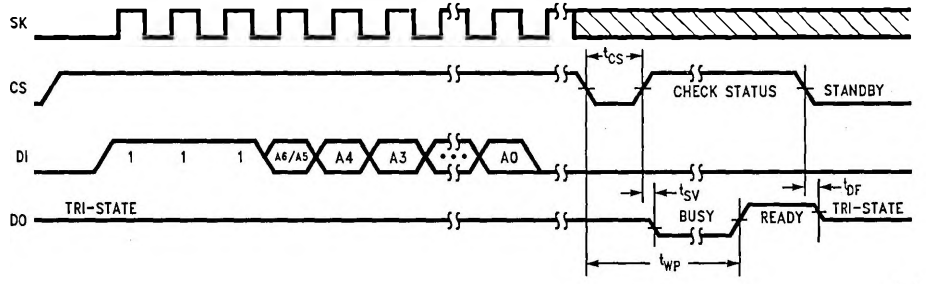
†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

Timing Diagrams (Continued)

ERASE



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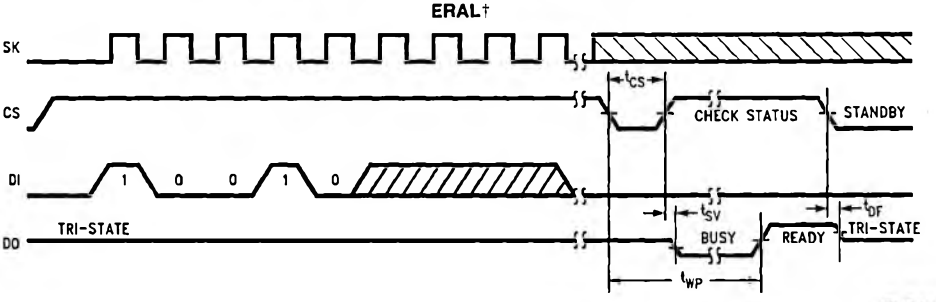
ERAL†



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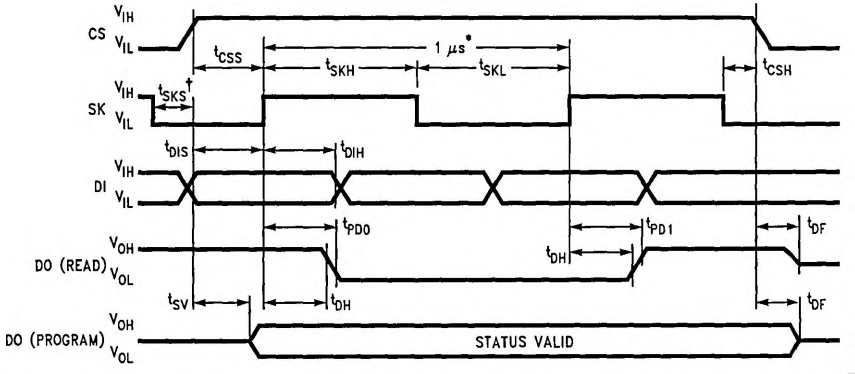
†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

Synchronous Data Timing



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*This is the minimum SK period (Note 2).

††t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).