DATA SHEET

OM5234/OM5284
CMOS single-chip 8-bit microcontrollers

Preliminary specification

1996 Nov 01

Philips
Semiconductors

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CMOS single-chip 8-bit microcontrollers OM5234/OM5284

DESCRIPTION

The OM5234 and OM5284 single-chip 8-bit microcontrollers are manufactured in an advanced CMOS process and are derivatives of the 80C51 microcontroller family. The OM5234 and OM5284 are pre-programmed devices for specific applications. Unless specifically stated otherwise, all references to OM5234 apply equally to OM5284.

The OM5234 contains a non-volatile 16k × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, UART and on-chip oscillator and timing circuits.

FEATURES

- 80C51 central processing unit
- 6k × 8 ROM
- 256 × 8 RAM
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- ROM code protection

ORDERING INFORMATION

OM5234 / F T P / YYY

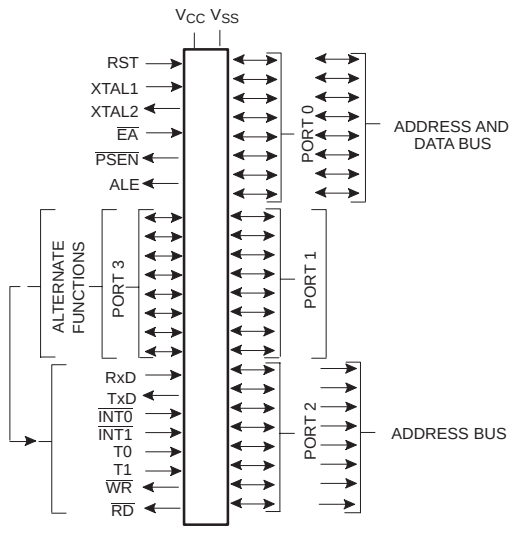
- Device: OM5234
- Frequency Range: F = 3.5 to 16MHz; I = 3.5 to 24MHz
- Temperature Range: B = 0 to 70°C
- Package designator: A = Plastic Leaded Chip Carrier; B = Plastic Quad Flat Package; P = Plastic Dual In-Line Package
- ROM code for application: 5XX, etc.

OM5284 X Y ZZ

- Device: OM5284
- Frequency Range: E = 3.5 to 16MHz; I = 3.5 to 24MHz
- Package designator: A = Plastic Leaded Chip Carier; B = Plastic Quad Flat Package; P = Plastic Dual In-Line Package
- ROM code for application: 01, 02, 03

PART NUMBER	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY (MHz)	DRAWING NUMBER
OM5234/FBB/YYY	0 to 70°C, Plastic Quad Flat Package	16	SOT307-2
OM5234/FBP/YYY	0 to 70°C, Plastic Dual In-Line Package	16	SOT129-1
OM5234/FBA/YYY	0 to 70°C, Plastic Leaded Chip Carrier	16	SOT187-2
OM5284EBYY	0 to 70°C, Plastic Quad Flat Package	16	SOT307-2
OM5284EAYY	0 to 70°C, Plastic Leaded Chip Carrier	16	SOT187-2
OM5284EPYY	0 to 70°C, Plastic Dual In-Line Package	16	SOT129-1

LOGIC SYMBOL



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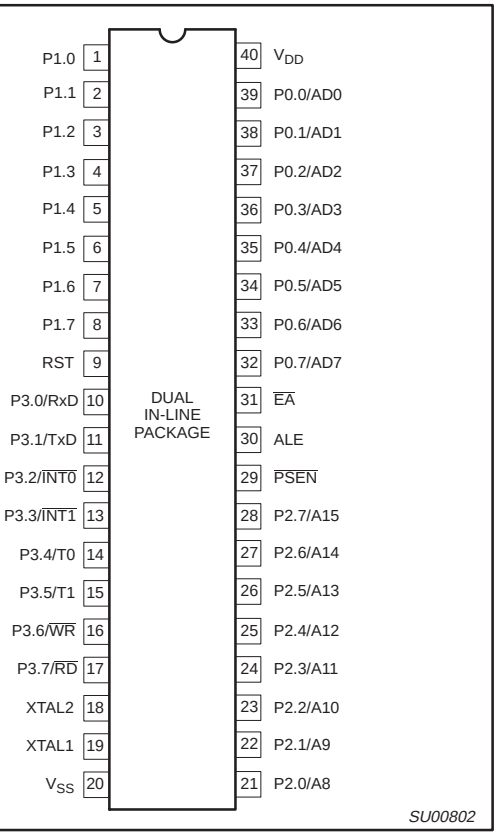
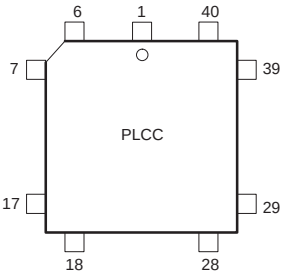
PIN CONFIGURATIONS

DUAL IN-LINE PACKAGE PIN FUNCTIONS



PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	NC*	16	P3.4/T0	31	P2.7/A15
2	P1.0	17	P3.5/T1	32	$\overline{PSEN}$
3	P1.1	18	P3.6/$\overline{WR}$	33	ALE
4	P1.2	19	P3.7/$\overline{RD}$	34	NC*
5	P1.3	20	XTAL2	35	$\overline{EA}$
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	V_{SS}	37	P0.6/AD6
8	P1.6	23	NC*	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/$\overline{INT0}$	29	P2.5/A13	44	V_{DD}
15	P3.3/$\overline{INT1}$	30	P2.6/A14		

* DO NOT CONNECT

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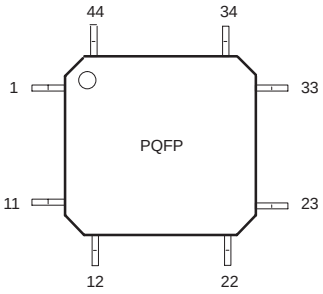
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	P1.5	16	V_{SS1}	31	P0.6/AD6
2	P1.6	17	NC*	32	P0.5/AD5
3	P1.7	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	V_{SS4}	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/$\overline{INT0}$	23	P2.5/A13	38	V_{DD}
9	P3.3/$\overline{INT1}$	24	P2.6/A14	39	V_{SS3}
10	P3.4/T0	25	P2.7/A15	40	P1.0
11	P3.5/T1	26	$\overline{PSEN}$	41	P1.1
12	P3.6/$\overline{WR}$	27	ALE	42	P1.2
13	P3.7/$\overline{RD}$	28	V_{SS2}	43	P.13
14	XTAL2	29	$\overline{EA}/V_{PP}$	44	P1.4
15	XTAL1	30	P0.7/AD7		

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PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER PLCC	QFP	DIP	TYPE	NAME AND FUNCTION
V_{SS}	22	6, 16, 28, 39	20	I	**Ground:** 0V reference. With the QFP package, all V_{SS} pins (V_{SS1} to V_{SS4}) must be connected.
V_{DD}	44	38	40	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	43–36	37–30	39–32	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	2–9	40–44, 1–3	1–8	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7, which are open drain for OM5234 (only). Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Alternate functions include:
P1.6	8	2	7	I/O	Bidirectional I/O with internal pull-ups (OM5284), and open drain for (OM5234).
P1.7	9	3	8	I/O	Bidirectional I/O with internal pull-ups (OM5284), and open drain for (OM5234).
P2.0–P2.7	24–31	18–25	21–28	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	11, 13–19	5, 7–13	10–17	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	11	5	10	I	**RxD (P3.0):** Serial input port
	13	7	11	O	**TxD (P3.1):** Serial output port
	14	8	12	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt
	15	9	13	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt
	16	10	14	I	**T0 (P3.4):** Timer 0 external input
	17	11	15	I	**T1 (P3.5):** Timer 1 external input
	18	12	16	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	19	13	17	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
RST	10	4	9	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE	33	27	30	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{\text{PSEN}}$	32	26	29	O	**Program Store Enable:** Read strobe to external program memory via Port 0 and Port 2. It is activated twice each machine cycle during fetches from the external program memory. When executing out of external program memory, two activations of $\overline{\text{PSEN}}$ are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated (remains HIGH) during fetches from external program memory. $\overline{\text{PSEN}}$ can sink/source 8 LSTTL inputs and can drive CMOS inputs without external pull-ups.
$\overline{\text{EA}}$	35	29	31	I	**External Access:** If during a RESET, $\overline{\text{EA}}$ is held at TTL, level HIGH, the CPU executes out of the internal program memory ROM provided the Program Counter is less than 16384. If during a RESET, $\overline{\text{EA}}$ is held at TTL LOW level, the CPU executes out of external program memory. $\overline{\text{EA}}$ is not allowed to float.
XTAL1	21	15	19	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	20	14	18	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid “latch-up” effect at power-on, the voltage on any pin at any time must not be higher than V_{DD} + 0.5V or V_{SS} – 0.5V, respectively.

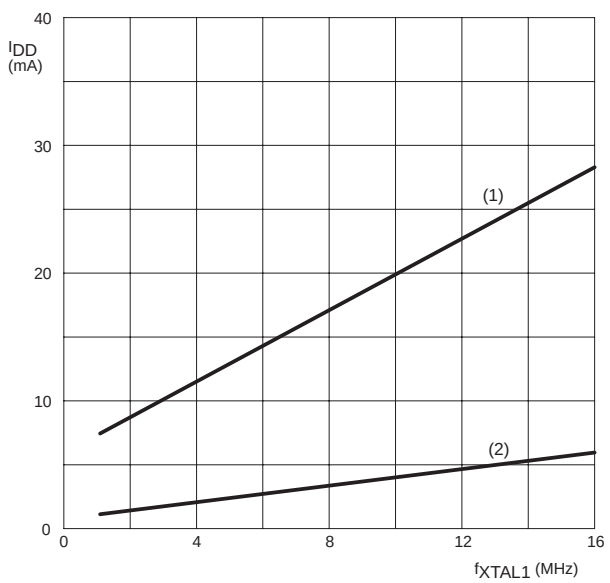
DC ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, V_{DD} = 5V ± 10%, T_{amb} = 0°C to +70°C

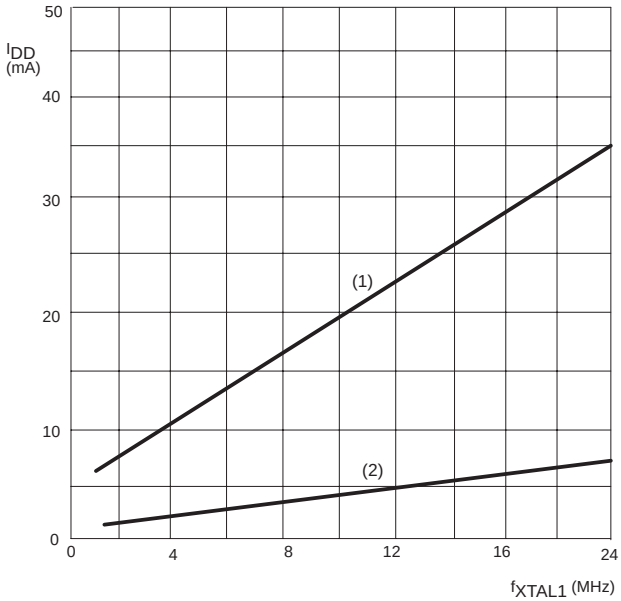
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{IL}	Input low voltage, except $\overline{EA}$, P1.6, P1.7		–0.5	$0.2V_{DD}$–0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$		–0.5	$0.2V_{DD}$–0.3	V
V_{IL2}	Input low voltage to P1.6, P1.7		–0.5	$0.3V_{DD}$	V
V_{IH}	Input high voltage, except XTAL1, RST, P1.6, P1.7		$0.2V_{DD}$+0.9	V_{DD}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{DD}$	V_{DD}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3, except P1.6, P1.7	I_{OL} = 1.6mA[6, 7]		0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$	I_{OL} = 3.2mA[6, 7]		0.45	V
V_{OL2}	Output low voltage, P1.6, P1.7	I_{OL} = 3.0mA		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3, ALE, $\overline{PSEN}$[8]	I_{OH} = –25µA	$0.75V_{DD}$		V
I_{IL}	Logical 0 input current, ports 1, 2, 3, except P1.6, P1.7	V_{IN} = 0.45V		–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6, P1.7	See note 5		–650	µA
I_{L1}	Input leakage current, port 0, $\overline{EA}$, P1.6, P1.7	0.45V < V_I < 4.7V		±10	µA
I_{DD}	Power supply current: Active mode @ 16MHz[1, 9] Idle mode @ 16MHz[2, 9] Power down mode[3, 4]	V_{DD}=5.5V		 32.0 6 50	 mA mA µA
R_{RST}	Internal reset pull-down resistor		40	225	kΩ
C_{IO}	Pin capacitance			15	pF

NOTES:

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 5ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{DD}$ –0.5V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = V_{DD}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 5ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{DD}$ –0.5V; XTAL2 not connected; Port 0 = P1.6 = P1.7 = V_{DD}; $\overline{EA}$ = RST = V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = P1.6 = P1.7 = V_{DD}; $\overline{EA}$ = RST = V_{SS}.
4. 2V $\leq V_{PD} \leq V_{DD}$max.
5. Pins of ports 1 , 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
7. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows: Maximum I_{OL} = 10mA per port pin; Maximum I_{OL} = 26mA total for Port 0; Maximum I_{OL} = 15mA total for Ports 1, 2, and 3; Maximum I_{OL} = 71mA total for all output pins. If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
8. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{DD}$ specification when the address bits are stabilizing.
9. I_{DDMAX} for other frequencies can be derived from Figure 1, where FREQ is the external oscillator frequency in MHz. I_{DDMAX} is given in mA.



(1) MAXIMUM OPERATING MODE: V_{DD} = V_{DDmax}
(2) MAXIMUM IDLE MODE: V_{DD} = V_{DDmax}
These values are valid within the specified frequency range.



(1) MAXIMUM OPERATING MODE: V_{DD} = V_{DDmax}
(2) MAXIMUM IDLE MODE: V_{DD} = V_{DDmax}
These values are valid within the specified frequency range.

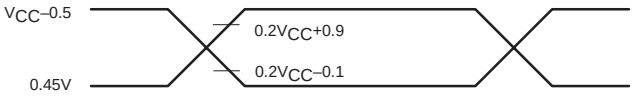
SU00801

Figure 1. I_{DD} vs. Frequency

AC ELECTRICAL CHARACTERISTICS[1, 2]

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
External Clock							
t_{CHCX}	2	High time[3]	20		20	$t_{CLCL} - t_{LOW}$	ns
t_{CLCX}	2	Low time[3]	20		20	$t_{CLCL} - t_{HIGH}$	ns
t_{CLCH}	2	Rise time[3]		20		20	ns
t_{CHCL}	2	Fall time[3]		20		20	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. These values are characterized but not 100% production tested.

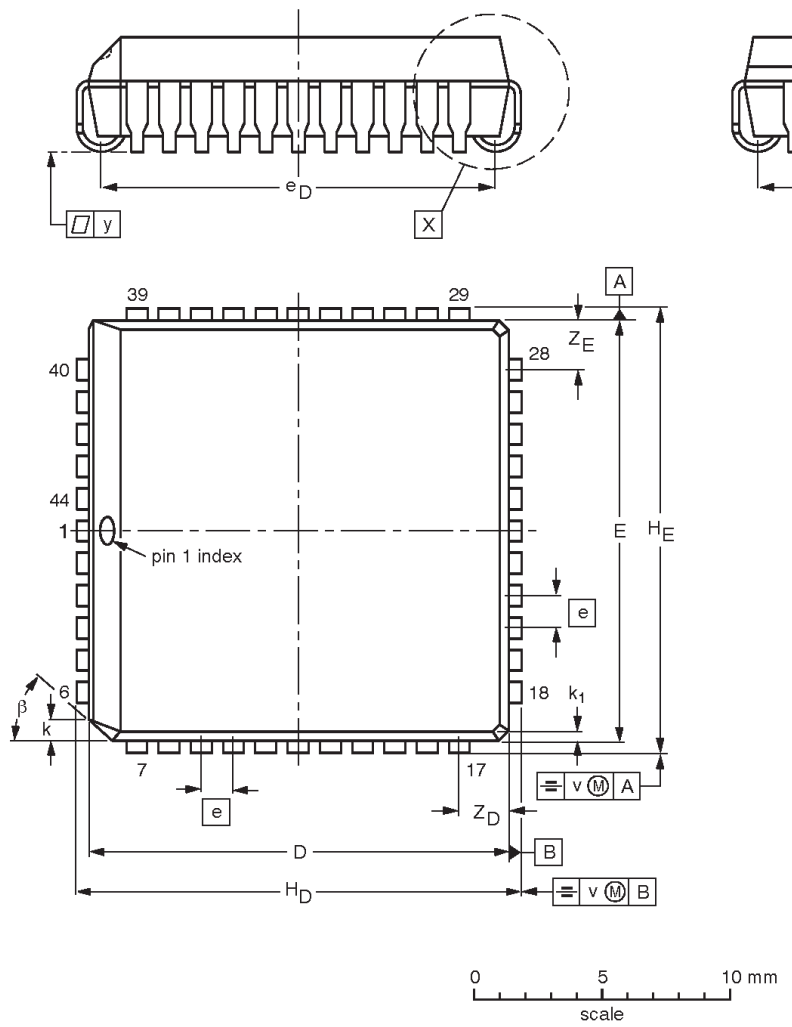


NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic '1' and 0.45V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

SU00010

Figure 2. AC Testing Input/Output

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

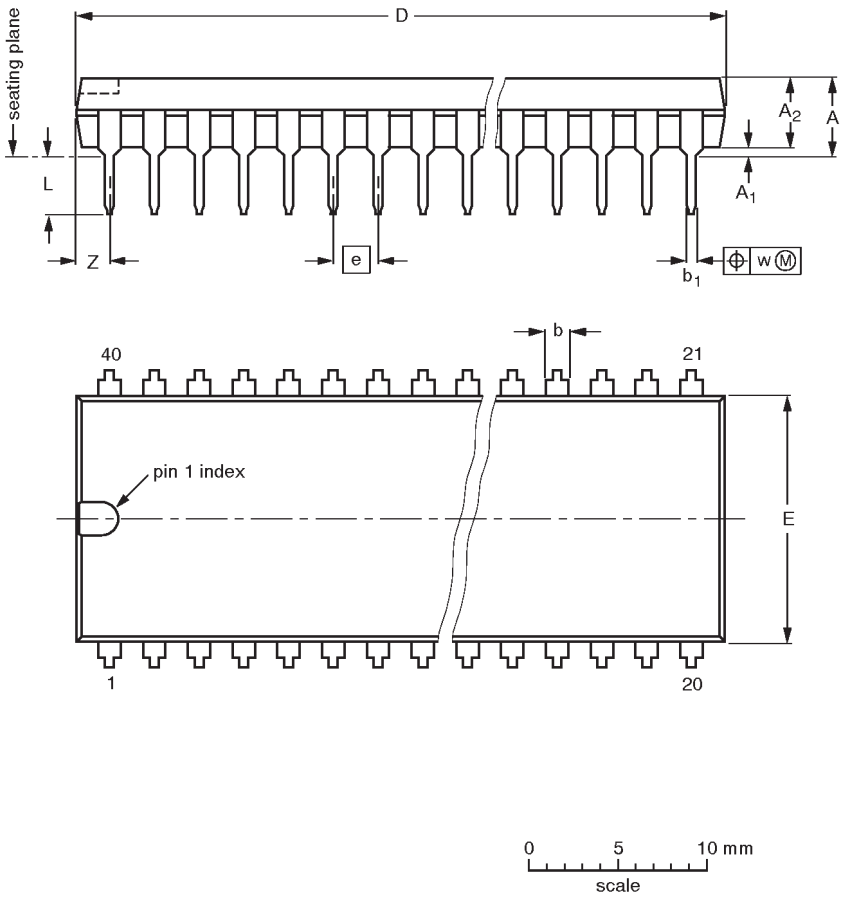
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

DIP40: plastic dual in-line package; 40 leads (600 mil) SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

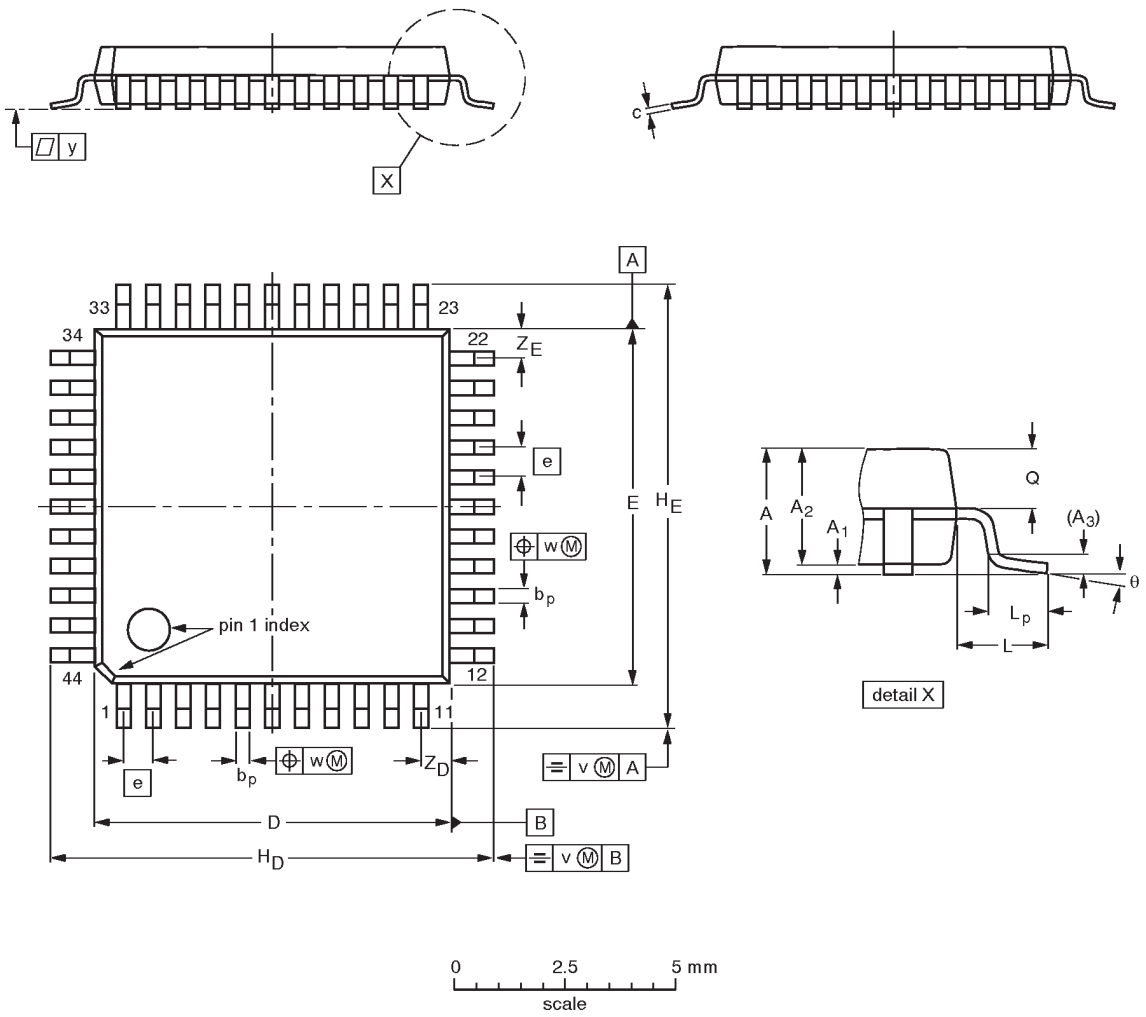
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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