



SBOS161A - JANUARY 1989 - REVISED JULY 2003

Precision Dual *Difet* ® Operational Amplifier

FEATURES

● Very Low Noise: 8nV/√Hz at 10kHz

Low V_{os}: 1mV max
 Low Drift: 10µV/°C max
 Low I_n: 10pA max

● Fast Settling Time: 2µs to 0.01%

Unity-Gain Stable

APPLICATIONS

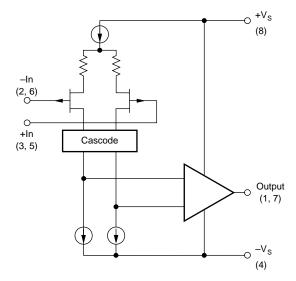
- Data Acquisition
- DAC Output Amplifiers
- Optoelectronics
- High-Impedance Sensor Amps
- High-Performance Audio Circuitry
- Medical Equipment, CT Scanners

DESCRIPTION

The OPA2107 dual operational amplifier provides precision **Difet** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (*Difet*) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent dc performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in DIP-8 and SO-8 packages.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±18V
Input Voltage Range±	V _S ±2V
Differential Input Voltage Total	V _S ±4V
Operating Temperature	-
P and U Packages25°C to	+ 85°C
Storage Temperature	
P and U Packages40°C to +	+125°C
Output Short Circuit to Ground (T _A = +25°C) Cont	tinuous
Junction Temperature 4	+175°C
Lead Temperature	
P Package (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C

NOTE: Stresses above these ratings may cause permanent damage.

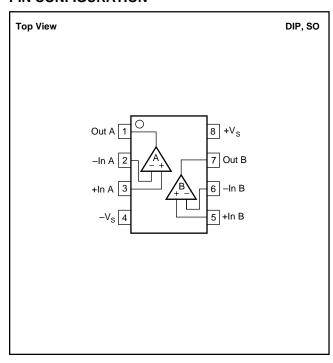


ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2107	DIP-8	Р	−25°C to +85°C	OPA2107AP	OPA2107AP	Tube, 50
OPA2107	SO-8 "	D "	−25°C to +85°C	OPA2107AU "	OPA2107AU OPA2107AU/2K5	Tube, 100 Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.



ELECTRICAL CHARACTERISTICS

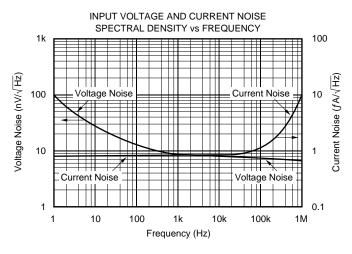
At T_A = +25°C, V_S = ±15V, unless otherwise noted.

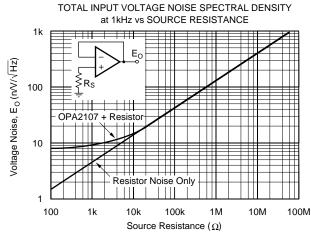
			OPA2107AP, AU				
PARAMETER	CONDITION	MIN	TYP	TYP MAX			
OFFSET VOLTAGE ⁽¹⁾ Input Offset Voltage Over Specified Temperature	V _{CM} = 0V		0.1 0.5	1 2	mV mV		
Average Drift Over Specified Temperature Power Supply Rejection	$V_{S} = \pm 10 \text{ to } \pm 18V$	80	3 96	10	μV/°C dB		
INPUT BIAS CURRENT ⁽¹⁾ Input Bias Current Over Specified Temperature	V _{CM} = 0V		4 0.25	10 1.5	pA nA		
Input Offset Current Over Specified Temperature	$V_{CM} = 0V$		1	8	pA nA		
INPUT NOISE Voltage: f = 10Hz f = 100Hz f = 1kHz f = 10kHz BW = 0.1 to 10Hz BW = 10 to 10kHz Current: f = 0.1Hz thru 20kHz BW = 0.1Hz to 10Hz	R _S = 0		30 12 9 8 1.2 0.85 1.2 23		nV/√Hz nV/√Hz nV/√Hz nV/√Hz μVp-p μVrms fA/√Hz fAp-p		
INPUT IMPEDANCE Differential Common-Mode			10 ¹³ 2 10 ¹⁴ 4		Ω pF Ω pF		
INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature Common-Mode Rejection	V _{CM} = ±10V	±10.5 ±10.2 80	±11 ±10.5 94		V V dB		
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature	$V_O = \pm 10V, R_L = 2k\Omega$	82 80	96 94		dB dB		
DYNAMIC RESPONSE Slew Rate Settling Time: 0.1%	$G = +1$ $G = -1, 10V Step$ $G = 100$ $G = +1, f = 1kHz$ $f = 100Hz, R_L = 2k\Omega$	13	18 1.5 2 4.5 0.001 120		V/μs μs μs MHz % dB		
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		±4.5	±15 ±4.5		V V mA		
OUTPUT Voltage Output Over Specified Temperature Short Circuit Current Output Resistance, Open-Loop Capacitive Load Stability	R _L = 2kΩ 1MHz G = +1	±11 ±10.5 ±10	±12 ±11.5 ±40 70 1000		V V mA Ω pF		
TEMPERATURE RANGE Specification Operating Storage Thermal Resistance $(\theta_{1:\Delta})$		-25 -25 -40		+85 +85 +125	°C °C °C		
DIP-8 SO-8			90 175		°C/W		

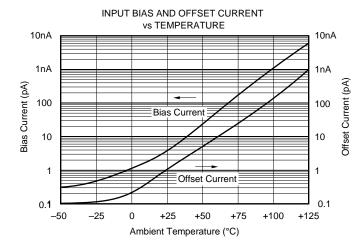
NOTE: (1) Specified with devices fully warmed up.

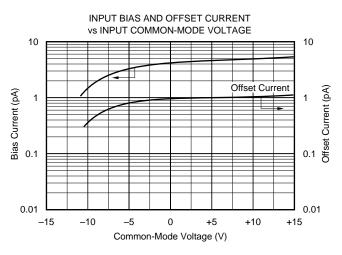
TYPICAL CHARACTERISTICS

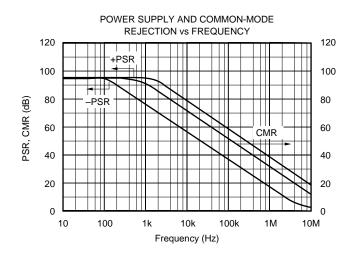
 T_A = +25°C, V_S = ±15V unless otherwise noted.

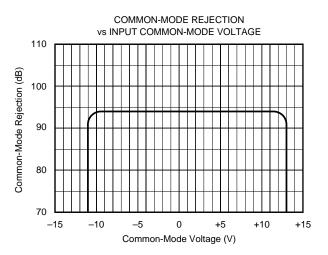






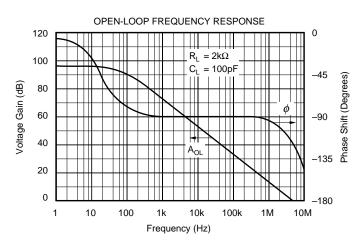


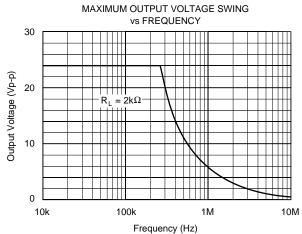


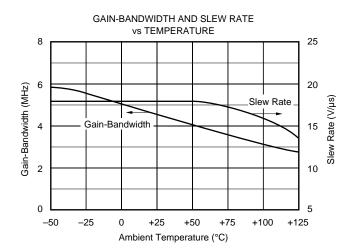


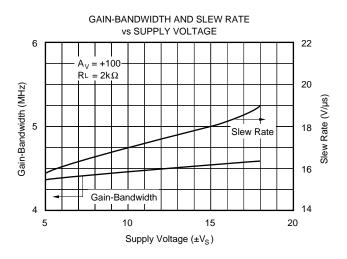
TYPICAL CHARACTERISTICS (Cont.)

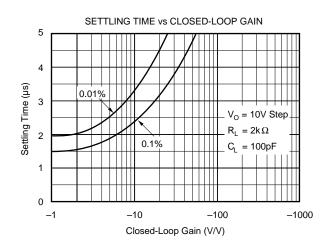
 $T_A = +25$ °C, $V_S = \pm 15$ V unless otherwise noted.

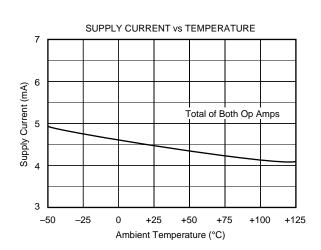






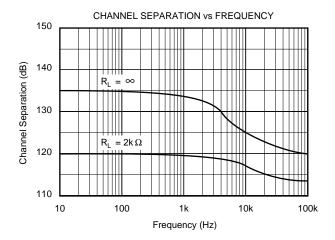


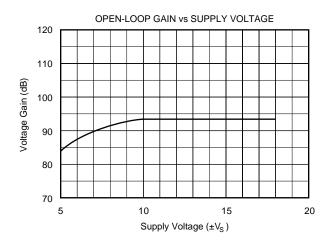


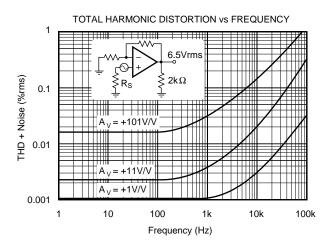


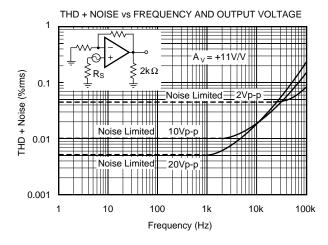
TYPICAL CHARACTERISTICS (Cont.)

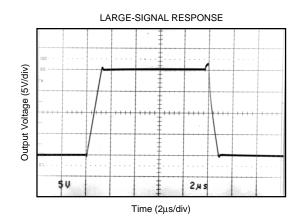
 $T_A = +25$ °C, $V_S = \pm 15$ V unless otherwise noted.

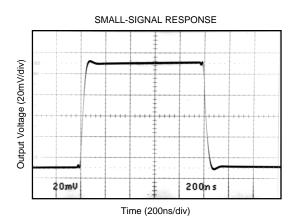












APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has an excellent phase margin. This makes it easy to use in a wide variety of applications.

Power-supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, $0.1\mu F$ ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to $1\mu F$ tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107 **Difet** input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit-board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances, a two-step cleaning process is adequate using a clean organic solvent rinse followed by deionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit-board guard pattern effectively reduces errors due to circuit-board leakage (Figure 1). By encircling critical high-impedance nodes with a low-impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low-impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

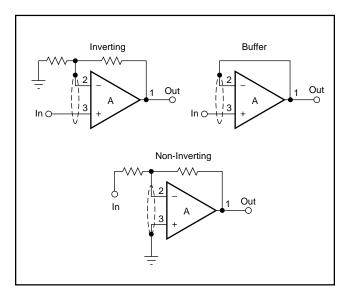


FIGURE 1. Connection of Input Guard.

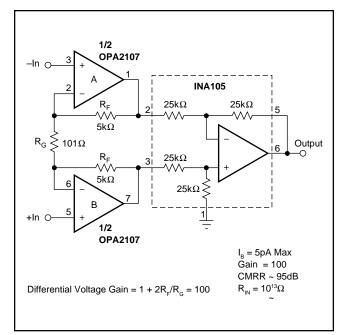


FIGURE 2. FET Input Instrumentation Amplifier.

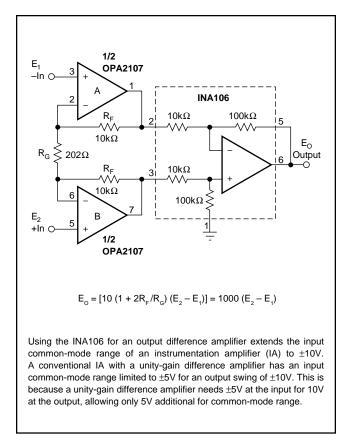


FIGURE 3. Precision Instrumentation Amplifier.





i.com 16-Feb-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
OPA2107AP	ACTIVE	PDIP	Р	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2107APG4	ACTIVE	PDIP	Р	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2107AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2107AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2107AU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2107AUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

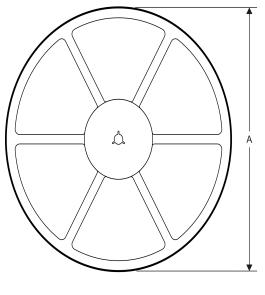
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

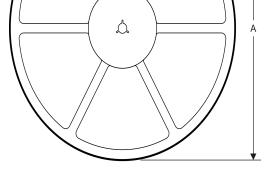
PACKAGE MATERIALS INFORMATION

14-Jul-2012 www.ti.com

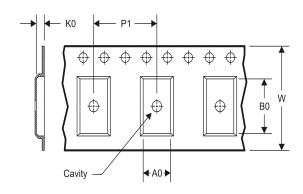
TAPE AND REEL INFORMATION

REEL DIMENSIONS





TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2107AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

www.ti.com 14-Jul-2012

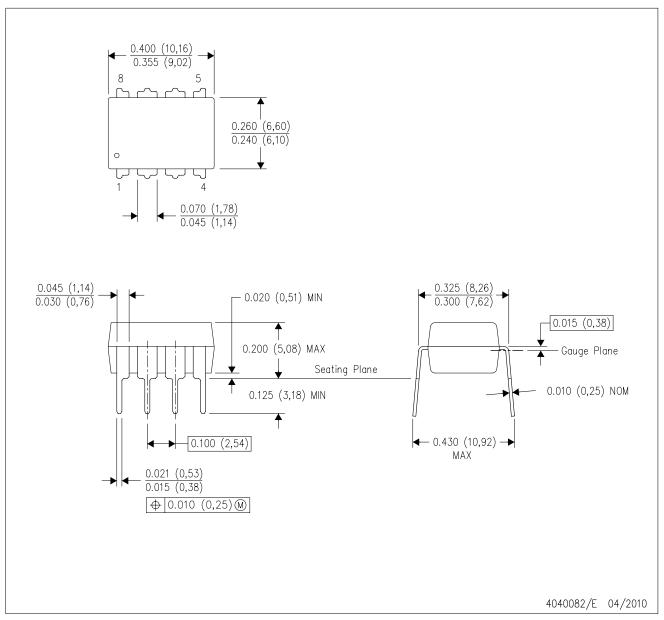


*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	OPA2107AU/2K5	SOIC	D	8	2500	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

roducts		Applications
	ti aaaa/adia	A

Pr

Audio Automotive and Transportation www.ti.com/automotive www.ti.com/audio www.ti.com/communications **Amplifiers** amplifier.ti.com Communications and Telecom **Data Converters** dataconverter.ti.com Computers and Peripherals www.ti.com/computers **DLP® Products** Consumer Electronics www.ti.com/consumer-apps www.dlp.com DSP dsp.ti.com **Energy and Lighting** www.ti.com/energy Clocks and Timers www.ti.com/clocks Industrial www.ti.com/industrial Interface interface.ti.com Medical www.ti.com/medical Logic logic.ti.com Security www.ti.com/security

Power Mgmt power.ti.com Space, Avionics and Defense www.ti.com/space-avionics-defense

Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

OMAP Mobile Processors www.ti.com/omap TI E2E Community e2e.ti.com

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>

www.ti-rfid.com