National Semiconductor

PAL10/10016RM4A
ECL Registered Programmable Array Logic

General Description

The PAL10/10016RM4A is a member of the National Semiconductor ECL PAL® family. The ECL PAL Series-A is characterized by 4 ns maximum propagation delays (combinatorial input-to-output). The pinout, JEDEC fuse-map format and programming algorithm of these devices are compatible with those of all prior ECL PAL products from National. Series-A ECL PAL devices are manufactured using National Semiconductor's advanced oxide-isolated process with proven titanium-tungsten fuse technology to provide high-speed user-programmable replacements for conventional ECL SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016RM logic array has a total of 16 complementary input pairs, 32 product terms and four output functions; each output function is the OR-sum of 8 product terms. The 16RM4A provides an edge-triggered D-type register on each of its four outputs. Registers allow the PAL device to implement sequential logic circuits. Polarity fuses allow each output to be active-high or active-low.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by several conventional TTL PLD programming units. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

Features

- High speed:
  - t_{SU} = 3 ns min
  - t_{CLK} = 2 ns max
  - f_{MAX} = 200 MHz max (registered)
  - t_{PD} = 4 ns max (combinatorial)
- Programmable replacement for ECL SSI/MSI logic
- Both 10 KH and 100K I/O compatible versions
- Four registered output functions with I/O pin feedback; twelve dedicated inputs
- Individually programmable polarity on all logic outputs
- Reliable Titanium Tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLAN™ Software
- Packaging:
  - 24-pin thin DIP (0.300")
  - 24-pin Quad Cerpak

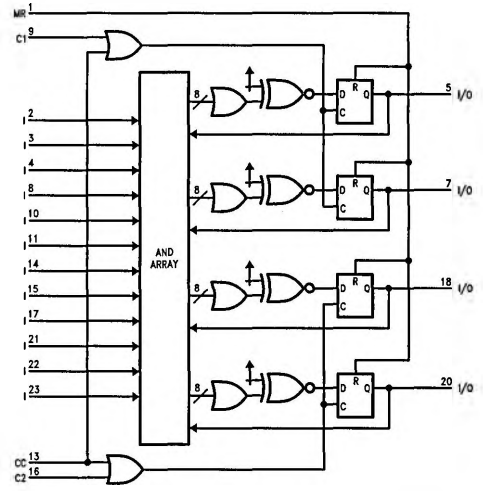
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

- Programmable Array Logic Family
- ECL I/O Compatibility:
  - 10 = 10 kH
  - 100 = 100K
- Number of Arrays
- Output Type:
  - RM = Registered with Multiple Clocks
- Number of Registered Outputs
- Speed/Power Version:
  - No Symbol = 6 ns t_{PD}
  - A = 4 ns t_{PD}
- Package:
  - J = 24-Pin Ceramic DIP
  - W = 24-Pin Quad Cerpak
- Temperature Range:
  - C = Commercial:
    - 0°C to +75°C for 10 kH,
    - 0°C to +85°C for 100k

PAL 10 16 RM 4 A J C

Block Diagram



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V_{EE} = 12, V_{CC} = 24, V_{CCO} (5,7) = 6, V_{CCO} (18,20) = 19
Pinout applies to 24-pin DIP.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7V to +0.5V
Input Voltage	V_{EE} to +0.5V
Output Current	−50 mA
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Tolerance	1000V
C_{ZAP} = 100 pF R_{ZAP} = 1500Ω Test Method: Human Body Model Test Specification: NSC SOP-5-028	

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{EE}	Supply Voltage	10 KH	−5.46	−5.2	−4.94	V
		100K	−4.73	−4.5	−4.27	
T	Operating Temperature (Note)	10 KH	0		+75	°C
		100K	0		+85	
R_L	Standard 10 KH/100K Load			50		Ω
C_L	Standard 10 KH/100K Load			5		pF
t_{SU}	Setup Time of Input or Feedback		3.0			ns
t_H	Input Hold Time		0			ns
t_W	Clock or Enable Pulse Width		2.0			ns
t_{WMR}	Master Reset Pulse Width		2.0			ns

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions		T_A	Min	Max	Units
V_{IH}	High Level Input Voltage	Guaranteed Input Voltage High For All Inputs	10 KH	0°C +25°C +75°C	−1170 −1130 −1070	−840 −810 −735	mV
			100K	0°C to +85°C	−1165	−880	
V_{IL}	Low Level Input Voltage	Guaranteed Input Voltage Low For All Inputs	10 KH	0°C +25°C +75°C	−1950 −1950 −1950	−1480 −1480 −1450	mV
			100K	0°C to +85°C	−1810	−1475	
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} Max. or V_{IL} Min.	10 KH	0°C +25°C +75°C	−1020 −980 −920	−840 −810 −735	mV
			100K	0°C to +85°C	−1025	−880	
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} Max. or V_{IL} Min.	10 KH	0°C +25°C +75°C	−1950 −1950 −1950	−1630 −1630 −1600	mV
			100K	0°C to +85°C	−1810	−1620	
I_{IH}	High Level Input Current	V_{IN} = V_{IH} Max.	Inputs, I/Os and MR			220	μA
			Clocks			350	
I_{IL}	Low Level Input Current	V_{IN} = V_{IL} Min. Except I/O Pins			0.5		μA
I_{EE}	Supply Current	V_{EE} = Min., All Inputs and Outputs Open			−240		mA

Note: Operating temperatures for circuits in Dual-In-Line packages are specified as ambient temperatures (T_A) with circuits mounted in socket or printed circuit board and transverse airflow exceeding 500 linear feet per minute. Operating temperatures for circuits packaged in Quad Cerpak are specified as case temperatures (T_C). All specifications apply after thermal equilibrium has been established.

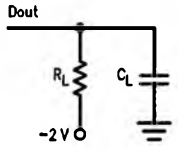
Switching Characteristics Over Recommended Operating Conditions

Output Load: $R_L = 50\Omega$ to $-2.0V$, $C_L = 5$ pF to GND

Symbol	Parameter	Measured		Min	Max	Units
		From	To			
t_{CLK}	Clock to Output or Feedback	$C_n \uparrow$	I/O		2.0	ns
t_{PD}	Input or Feedback to Output	I	I/O		4.0	ns
t_{MR}	Master Reset to Output	MR $\uparrow$	I/O $\downarrow$		3.5	ns
f_{MAX} (Note 1)	Maximum Frequency				200	MHz
t_r	Output Rise Time	Measured Between 20% and 80% points		0.5	2.0	ns
t_f	Output Fall Time			0.5	2.0	ns

Note 1: $f_{MAX} = (t_{SU} + t_{CLK})^{-1}$

Test Load



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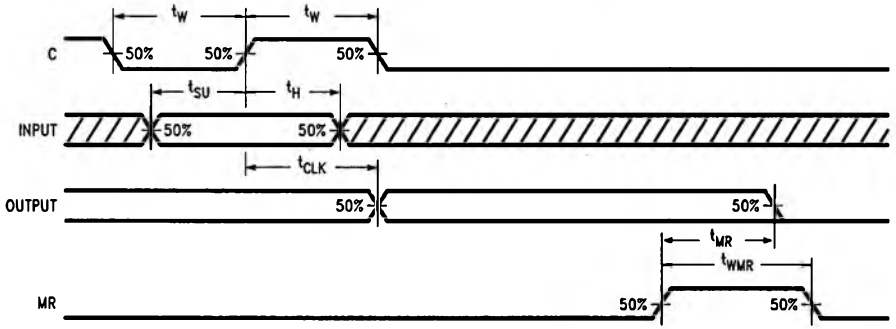
Timing Waveform PAL10/10016RM4A



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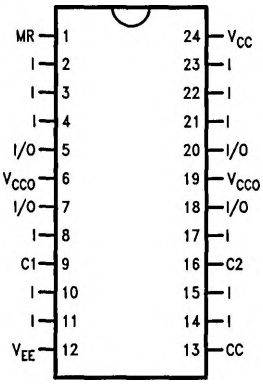
Connection Diagrams

24-Pin Dual-In-Line Package
PAL10/10016RM4A



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Pin Descriptions

Pin	Description
I	Twelve dedicated inputs to logic array.
I/O	Four outputs from registered provides feedback and may be used for additional inputs to logic array.
C1	Clock input ORed with CC to control registers on output pins* 5 and 7. Data is written into registers on rising edge of clock.
C2	Clock input ORed with CC to control registers on output pins* 18 and 20. Data is written into registers on rising edge of clock.
CC	Common Clock input (see C1, C2).
MR	Master Reset input. Asynchronously resets all registers to the low state while MR is high (overrides clock input).
V_{EE}	Supply voltage.
V_{CC}	Ground for internal circuitry.
V_{CCO}	Ground for output drivers (2 outputs per V_{CCO}).

*Corresponds to DIP pinout

Functional Description

The PAL10/10016RM consists of a single programmable AND-gate array with fixed OR-gate connections. The AND array consists of 16 complementary pairs of input lines crossing 32 product-term lines with a programmable fuse at each intersection (1024 fuses). The product terms are organized into four groups of eight each. The eight product terms in each group are connected into an OR-gate to produce the sum-of-products logic function.

An unprogrammed fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term. Programming the fuse removes the connection. A product term is satisfied (logically true) while all the input lines connected to it (via intact fuses) are in the proper logic state. Therefore, if both the true and complement of at least one array input are left connected to a product line, that product term would always be held in the low logic state (which is the state of all product terms in an unprogrammed device).

The four outputs of the PAL10/10016RM4A pass through D-type registers triggered on the high-going edge of the appropriate clock input. The four registers are separated into two pairs. A separate clock input is provided for each pair. An additional common clock input is ORed with each (see logic diagrams which follow).

The AND-OR logic functions can be optionally inverted before the registers. Polarity inversion is controlled by an individual "polarity fuse" associated with each output function (the original unprogrammed state produces active-high logic functions). Device output pins always indicate active-high register outputs.

The I/O pins used for outputting the registered logic functions also feed back into the logic array as additional inputs. This is useful, for example, to implement sequential circuits with registered parts. Any of these I/O pins may, instead, be used as an additional dedicated input pin. By leaving the associated logic function unprogrammed, the output driver would remain in the low logic state allowing an externally-applied signal to control the array input.

Logic functions requiring more than eight product terms can be implemented conveniently by OR-tying two (or more) device outputs. Partial sums are formed on each of the OR-tied output functions. Each function, however, must be programmed for active-high output polarity, and the associated registers should be controlled by the same clock signal. Each of the array inputs fed back from the OR-tied I/O pins would indicate the correct final logic function.

All input and I/O pins have on-chip 50 kΩ pull-down resistors.

Functional Testing

As with all field-programmable devices, the user of ECL PAL devices provides the final manufacturing step. While National's PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user's pattern.

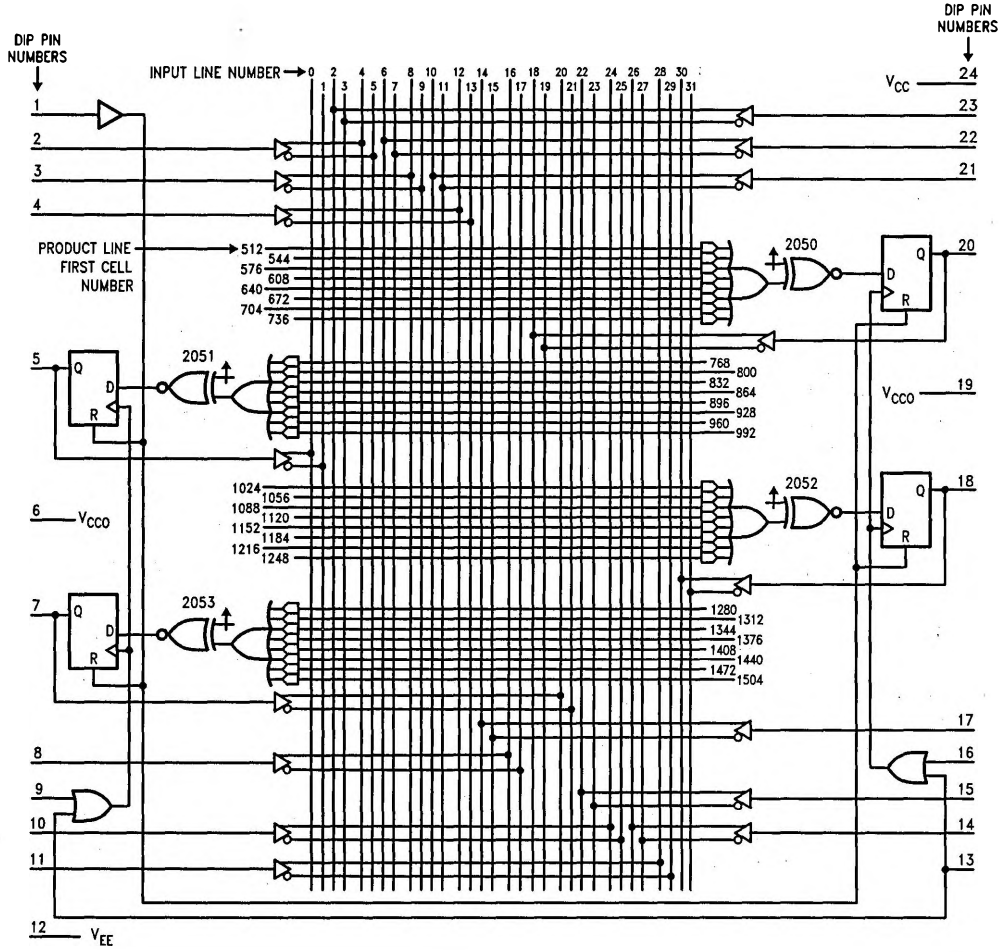
To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that PAL devices be functionally tested before they are installed in your system. Even though the number of post-programming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. For more information about the functional testing of PAL devices, please refer to National Semiconductor's Application Note #351 and the *Programmable Logic Design Guide.*

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the PAL10/10016RM are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the ECL PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Logic Diagram—PAL1016RM4A/PAL10016RM4A



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JEDEC logic array cell number = product line first cell number + input line number.