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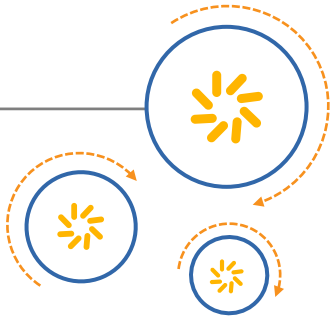

Qualcomm® Snapdragon™ 600E Processor APQ8064E

Device Specification

July 2017

Qualcomm Technologies, Inc.
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U.S.A.

LM80-P0598-1 Rev. D

Revision history

Revision	Date	Description
A	June 1, 2015	Initial Release
B	February 10, 2016	Removed Figure 3.1 and Section 3.1.1
C	September 2016	■ Updated part number to “E” ■ Chapter 1: modified bullet item to: Longevity beyond lifecycle of mobile chipsets through 2025 ■ Section 1.4: Referenced documents: added section ■ Chapter 2, 3, and 22: Changed WGR7640 to RGR7640 ■ Section 3.1.1: Architecture and baseband processing features: Changed processor speed to 1.5 GHz ■ Section 3.1.7: Features of internal functions: removed QFPROM section ■ Section 3.1.9, Table 3-2: Key APQ 8064E features: Changed processor speed to 1.5 GHz ■ Section 3.2: Krait microprocessor subsystem: Changed to: Quad Krait mP CPUs, each with up to 1.5 GHz ■ Section 12.2.1 EEPROM: removed since it references an obsolete document ■ Section 28.2.3: Changed Qualcomm Atheros reference to Qualcomm Technologies, Inc.
D	July 18, 2017	■ Changed document type to Device Specification ■ Modified contents to use source document 80-NM754-1_G APQ8064AU Automotive Device Specification

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1 Introduction

This document describes features and functionality of Qualcomm® Snapdragon™ 600E processor (model APQ8064E) for embedded computing. This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE Enabling some features may require additional licensing fees

Qualcomm processors for embedded computing are dedicated to support embedded device OEMs in several ways:

- Longevity beyond lifecycle of mobile chipset, support through to 2025
- Detailed documentation for developers
- Availability of development kits/community board for early access
- Multiple OS support including mainline Linux support
- Availability of several computing module partners for customization for your individual projects/products

Snapdragon 600 processors deliver high-performance computing, low-power consumption, and a rich multimedia experience for embedded devices.

It is an ideal solution for any application that requires compute horsepower and integrated Wi-Fi/Bluetooth connectivity, such as Smart Home, Industrial Appliances, Digital Media and TV dongles, Smart Surveillance, and Robotics.

Snapdragon supports a clear deployment path for embedded device OEMs and developers – starting with single-board computers and development kits, and scaling up to customer solutions, integration services, and production-ready, customizable computing modules.

For further information, visit https://www.qualcomm.com/products/snapdragon/embedded-computing.

1.1 Documentation overview

This document is the device specification for the APQ8064E. Complementary ICs within the APQ8064E chipset include:

- Integrated GPS: RGR7640 IC
- Power management: PMM8920 IC
- WLAN and FM radio: QCA6234 IC
- Audio codec: WCD9311 IC

Table 1-1 Primary APQ8064E documentation

Title/description	Document #
GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH+Xtal Mini-Specification Provides a description of chipset capabilities.	LM80-P0598-8
PMM8920 Power Management Module Device Specification Introduces the PMM8920 device that integrates two power management (PM) die (PM8921 and PM8821 die) into a single module, and then defines: its pin assignments; composite (PM8921 + PM8821 IC) electrical specifications; mechanical packaging; shipping, storage, and handling instructions; printed circuit board (PCB) mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.	LM80-P0598-4
QCA6234 Integrated Dual-Band 2 x 2 802.11n + Bluetooth 4.0 Data Sheet	LM80-P0598-12
Qualcomm Snapdragon 600E (APQ8064E) Clock Plan	LM80-P0598-15
Qualcomm Snapdragon 600E Processor APQ8064E Design Guidelines Provides detailed descriptions of all APQ806E device functions and interfaces, including its various operating modes, and is largely applicable to the APQ8064E device. Example applications are presented, then specific design topics are addressed, such as layout guidelines, power-distribution recommendations, external-component recommendations, and troubleshooting techniques.	LM80-P0598-14
Qualcomm Snapdragon 600E Processor APQ8064E Device Specification Provides all device electrical and mechanical specifications including feature descriptions, pin assignment definitions, shipping, storing, and handling instructions, printed circuit board (PCB) mounting specifications, and part reliability	LM80-P0598-1 (this document)
Qualcomm Snapdragon 600E Processor APQ8064E Hardware Register Description Provides detailed information about the APQ8064E software interface and its clocks, security, user interface, and registers.	LM80-P0598-5
Qualcomm Snapdragon 600E Processor APQ8064E Multimedia Card/Secure Digital Card Application Note	LM80-P0598-7
Qualcomm Snapdragon 600E Processor APQ8064E Recommended Memory Controller And Device Settings Application Note	LM80-P0598-6

This APQ8064E device specification is organized as follows:

Chapter 1 Provides an overview of the APQ8064E device documentation, a high-level functional description of the device, the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical performance specifications, including absolute maximum and recommended operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 6 Discusses shipping, storage, and handling of the APQ8064E device.

Chapter 5 Presents procedures and specifications for mounting the APQ8064E device onto PCBs.

Chapter 7 Presents APQ8064E device reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 APQ8064E introduction

The APQ8064E solution's high-level integration significantly reduces the bill-of-material (BOM). The 28 nm CMOS fabrication technology improves power efficiency for longer wireless connectivity, while enhancing the user's multimedia experience. These factors reduce product complexity, cost, time-to-market, and adds features and functions.

1.2.1 APQ8064E example products

Connectivity and embedded-computing products based upon the APQ8064E chipset include:

1. Robots
2. Drones
3. Digital signage systems
4. Medical devices
5. Smart home hubs
6. Video conferencing system
7. Security and surveillance system
8. Gaming machines and kiosks
9. Point of Sale devices
10. Specialized cameras

1.2.2 APQ8064E benefits

The APQ8064E device benefits include:

- Higher integration to reduce PCB surface area, power consumption, time-to-market, and BOM costs, while adding capabilities and processing power
- Integrated quad-core applications processor, integrated GPU, and hardware cores that eliminate the need for external multimedia coprocessor or external GPU
  - Higher computational power for high-end features
  - DC power savings enable longer run-times and lower temperature operation for any use case
- Position-location and navigation systems supported through the RGR7640 global navigation satellite system (GNSS) receiver
  - The APQ8064E device supports GPS and GLONASS operations
- The APQ8064E device is fabricated using the advanced 28 nm CMOS process. The device is available in the following package:
  - 23 × 23 × 2.57 mm package – 784-pin flip-chip ball grid array + heat spreader package (784 FCBGA+HS) footprint.

- The device includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. See Chapter 2 for pin assignment details and Chapter 4 for mechanical information.

1.2.3 APQ8064E major function blocks

The APQ8064E device includes many diverse functions, its operation is more easily understood by considering major functional blocks individually. This APQ8064E device specification document is organized according to the following block partitioning:

- Architecture and baseband processors features
- Memory support features
- Air interfaces features
- Multimedia features
- Connectivity features
- Configurable GPIO features
- Internal function features
- Chipset interfaces features
- Package features

Most of the information contained in this device specification are organized accordingly, including the circuit groupings within the functional block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3). Refer to the *Qualcomm Snapdragon 600E Processor APQ8064E Design Guidelines* (LM80-P0598-14) for a detailed description of each APQ8064E device function and interface, plus guidelines for implementing your design.

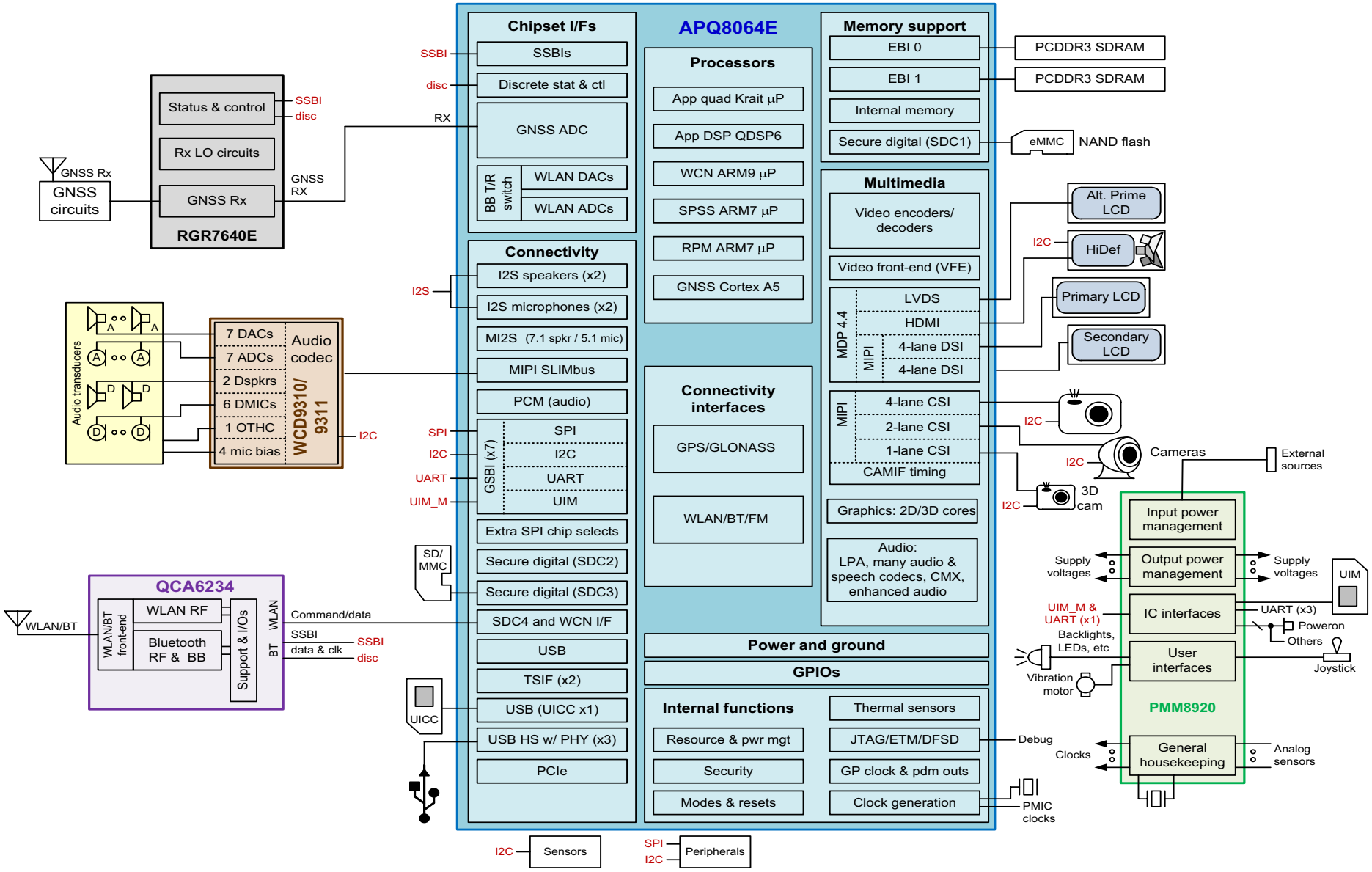


Figure 1-1 APQ8064E device functional block diagram and example application

1.3 APQ8064E device features

NOTE Some of the hardware features integrated within the APQ8064E device must be enabled by software. See the latest version of the applicable software release notes to identify the enabled APQ8064E device features. Enabling some features will require additional licensing fees.

The following features are integrated into the APQ8064E device:

- Advanced fabrication technology
- Processing power
- Smart peripheral subsystem (SPSS) for improved secure digital (SD) and USB transfer rates while offloading the application processors
- Global navigation satellite system (GNSS) engine
- High camera resolution
- Graphics support
- Mobile Industry Processor Interface (MIPI) support for cameras and displays
- High-definition encode/decode and integrated high-definition multimedia interface (HDMI)
- Three-display support
- Support for both SD and multimedia card (MMC)
- Wireless connectivity support depending on external devices

1.3.1 Air interface features

The APQ8064E has several wireless interfaces for transmission and reception of information. These interfaces are GPS, Wi-Fi, and Bluetooth. The following sections describe the key features of each air interface.

1.3.1.1 Position-location and navigation systems

Table 1-2 Position-location and navigation summary

Standard	Feature descriptions
Qualcomm ® location ***with GNSS support***	
GPS	■ Global positioning system (GPS) □ Qualcomm location with GPS engine and low-power tracking □ Qualcomm location for standalone GPS performance □ Navigation 3.0, dynamic power optimization, on-demand positioning, and SBAS (such as WAAS, EGNOS, MSAS) □ Support for Wi-Fi positioning □ Control plane: IS-801, IS-881, and UMTS CP assisted-GPS protocols □ User plane: v1/v2 trusted mode and OMA SUPL 1.0 assisted-GPS protocols □ Wideband processing of GPS signals helps resolve multipath interference, promoting improved measurement accuracy
GLONASS	■ Support for GLONASS standalone mode □ GLONASS capability increases the number of satellites available to the positioning engine

1.3.1.2 Wireless connectivity

WLAN and Bluetooth functionality is controlled by the QCA6234 device.

The QCA6234 is a complete, small form factor 2x2 802.11 a/b/g/n WLAN plus BT4.0 combo solution optimized for low-power, mobile consumer electronic devices. The device integrates all WLAN and BT functionality in a single package to support a low cost, layout-friendly implementation while allowing flexibility for platform specific customization.

For more information on wireless connectivity, see *QCA6234 Integrated Dual-Band 2 x 2 802.11n + Bluetooth 4.0 Data Sheet*, LM80-P0598-12.

Table 1-3 Wireless connectivity summary (organized by standard)

Standard	Feature descriptions
WLAN	
802.11 a/b/g/n/ac	■ 40 MHz channels at 5 GHz ■ Half guard interval for high throughput ■ Frame aggregation for high throughput ■ Space time block coding (STBC) Rx for improved downlink robustness over range ■ Low density parity check (LDPC) encoding for improved uplink and downlink robustness over range ■ Maximum ratio combining (MRC) ■ Transmit beamforming (TxBF) ■ Maximum likelihood (ML) decoder ■ Supports popular interfaces used in embedded designs: □ SDIO 2.0 (50 MHz, 4-bit and 1-bit) for WLAN □ High-speed UART (up to 4 Mbps) ■ All WLAN RF transmitters are pre-calibrated

Table 1-3 Wireless connectivity summary (organized by standard) (cont.)

Standard	Feature descriptions
BT	
BT 4.0 LE	■ Bluetooth low energy (BT4.0) ready □ Class 1.5 Bluetooth with integrated Tx/Rx switch ■ All WLAN RF transmitters are pre-calibrated ■ Near-zero power consumption in idle and stand-by ■ Advanced BT

1.3.2 Summary of key APQ8064E features

Table 1-4 lists all the key features of APQ8064E.

Table 1-4 Key APQ8064E features

Feature	APQ8064E capability
Processors	
Processors Applications subsystem RPM system Smart peripheral subsystem BT/FM GPS subsystem Cache Coprocessor	 Four Krait mP cores (to 1.5 GHz) plus one QDSP6 core (to 500 MHz) ARM7 ARM7 ARM9 Cortex A5 2 MB L2 cache (combined) VeNum 128-bit SIMD multimedia (Single Instruction Multiple Data)
Memory support	
External memory Via EBI Via SDC interface Via SPI	Up to 4 chip selects (2 on EBI0 and 2 on EBI1) 533 MHz; 32-bit; up to 4 GB density DDR3/3L SDRAM eMMC NAND flash / SD devices NOR memory devices (requires user-modified software)
Other internal memory	256 kB of LMEM 192 kB of MIMEM
RF support	
GNSS – supported features	gpsOne; standalone, MS-A, MS-B, and GLONASS
Multimedia	
Camera interfaces Primary Secondary Tertiary In-line JPEG	Camera; 20 MP 4-lane MIPI_CSI – 20 MP; 60 fps WXGA viewfinder frame rate, VFE raw dump of CSI data at line rate (4 Gbps) to LPDDR2 or PCDDR3), SMIA++ support, I^2C or SPI control 2-lane MIPI_CSI – 8 MP; web cam support 1-lane MIPI_CSI - 8 MP; 3D support Reduced shot-to-shot latency for multi-shot photos

Table 1-4 Key APQ8064E features (cont.)

Feature	APQ8064E capability
Video applications performance	
Camcorder	30 fps at 1080p (H.264/MPEG4); 30 fps at D1 (H.263)
TV	
Playback	30 fps 1080p (H.264/MPEG2/4/DivX/VC-1); 30 fps D1 (H.263)
Streaming	30 fps 1080p (H.264/MPEG2/4/DivX/VC-1); 30 fps at D1 (H.263)
Videophone	15 fps at QCIF (MPEG4/H.263)
Audio	
Codec	Integrated within the WCD9311, I2S busses or SLIMbus Up to 6 digital microphones, 2 speakers, 7 ADCs, and 7 DACs
Low-power audio	Low-power, low-complexity; versatile post-processing; 7.1 surround
Synthesizer	CMX: 128-voices, 512 kB polyphony wavetable
Enhanced	MP3, AAC, aacPlus, eAAC, AMR-NB, AMR-WB, G.711, WMA 9/10 Pro Dolby 5.1 and 7.1 Surround (AC-3) Qualcomm(R) Fluence™ noise cancellation technology AudioFX/Concert/Ensemble
A/V outputs	
HDMI Rev 1.4a (or MHL)	Integrated HDMI Tx core and HDMI PHY 1080 p at 60 Hz refresh; 24-bit RGB colorpack Up to 8-channel audio for 7.1 surround sound Dolby Digital Plus, Dolby True-HD, and DTS-HD Master
2D/3D graphics acceleration	Qualcomm® Adreno™ GPU 320 graphics core: 200 M peak triangles/sec; 6.4 B vector shader instructions/sec; 3.2 BP/sec; 3.2 B texel/sec APIs include OpenGL ES 1.x, 2.0, and 3.0; Direct3D Dx9.x; C2D for 2D composition; OpenCL for Adreno 320
Display support	Up to three concurrent displays, dual display up to 60 Hz refresh, Color depth: 24-bit pp, types: TFT, LTPS< CSTN, and OLED
Primary	Dual-link MIPI DSI, 1 Gbps per lane, up to QXGA (2560 x 1600)
Alternate primary	LVDS – up to QXGA (2048 x 1536); dual channel
Secondary	4-lane MIPI DSI, 1 Gbps per lane, up to QHD (960 × 540)
Simultaneous display	Primary via 4-lane MIPI DSI or LVDS, up to QXGA (2048 x 1536); secondary via 3-lane MIPI DSI, up to QHD (960 × 540); plus external display
Tertiary	HDMI/MHL
Mobile display processor (MDP)	MDP 4.4
Connectivity	
GSBI ports	Seven, each up to 4 bits wide; multiplexed serial interface functions; configuration options: UART, UIM, I2C, SPI, GPIO bits
USB interfaces	3 USB 2.0 HS ports with built-in PHY (480 Mbps) as a peripheral or embedded host 1 USB 2.0 full-speed for UICC only: SIM, USIM, and CSIM apps; multi-mode support for SIM+USIM+CSIM, & UMTS support for SIM+USIM
High-speed inter-chip (HSIC)	Interface between the APQ8064E device and an external connectivity module; easy integration, low power, and low processor loading

Table 1-4 Key APQ8064E features (cont.)

Feature	APQ8064E capability
PCIe interface	PCIe 2.0 port, 1-lane
UART interfaces	Via GSBI; high-speed (UART_DM ports, up to 4 Mbps) and standard UART ports
User Identify Module (UIM) support	Via GSBI; SIM+USIM+CSIM and SIM+USIM, data rates up to 4 MHz, 1.8 V support; 3.0 V support with PMIC-level translators
Secure digital (SD) controller interfaces	Up to four ports; supports both 4-bit and 8-bit interfaces; MMC and SD cards; eMMC NAND flash; SD/eMMC boot, Different operating voltages available, depends on the controller WLAN support SDC3 support dual-voltage (1.8 V and 2.9 V) SD card interface Supports both SD version 3.0 and MMC version 4.4.1/4.5
I^2C interfaces	Via GSBI; 1.8 V interfaces, controls for some chipset ICs; camera sensor/ module controls; NFC; etc.
I^2S interfaces	Supports external audio devices
SLIMbus	Audio interfaces with the WCD9311
Serial peripheral interface (SPI) (master only)	Via GSBI; up to 52 MHz output clock; sensor/module controls; external bridge components, other applications; NOR memory support (with user-modified software)
Pulse-coded modulation (PCM)	Available
Transport stream interface (TSIF)	Up to two ports
Touch screen support Capacitive panels	Supports an external touch screen controller IC, via I^2C, SPI, and interrupts
NFC	With external NFC device via I^2C
Configurable GPIO	90 GPIO pins (GPIO_0 to GPIO_89) Input configurations: pullup, pulldown, keeper, or no-pull Output configurations: programmable drive current top-level mode multiplexer (TLMM) to program groups of GPIOs
Internal functions	
Security	Secure boot, secure file systems (SFS), OMA DRM 1.0/2.1, ARM TrustZone, SecureAPQ v3, Microsoft Windows Mobile DRM10 and HDCP for HDMI Crypto engine V4 with algorithms that accelerate file system encryption (AES-XTS) and IPSec and SSL (HMAC-SHA, CCM, and CBCMAC) New security controller (with enhanced Qfuse) provides secure HDCP key provisioning and secure debug facility
Resource and power manager (RPM)	Improved efficiency through clock control, split-rail power collapse and voltage scaling, supports several low-power sleep modes Enables new boot sequences compared to previous APQs

Table 1-4 Key APQ8064E features (cont.)

Feature	APQ8064E capability
Boot sequence	New boot sequence: 1) RPM system 2) Applications system 3) Other processor subsystem Supports emergency boot over HS-USB Fast boot time
Phase-locked loop (PLLs) and clock generation / distribution	19.2 MHz CXO, 27 MHz PXO, 48 MHz WCN_XO & 32.768 kHz sleep clock inputs Includes multiple internal clock regimes Contains general-purpose clock, M/N counter, and PDM outputs Contains internal watchdog and sleep timers
Chipset interface functions	
Wireless GPS receiver (RGR)	Rx analog baseband from RGR to APQ ADC Clock from PMM8920E Single-wire serial bus interface (SSBI) Dedicated status and control lines as needed
Audio codec to / from the WCD	SLIMbus for highly multiplexed, high-speed audio data I^2C for primary status and control Plus dedicated status and control lines as needed
Wireless connectivity network interfaces	SDIO interface to QCA6234 module for Wi-Fi and BT wireless interfaces
PMIC status and control (PMM8920E)	SSBI Interrupt ports and other dedicated clock and control signals
Housekeeping ADC and analog multiplexer	Integrated into the PMM8920E
Package features	
Ball grid array Outline Ground pins	784-pin flip-chip ball grid array (BGA) package (784 FCBGA+ Heat Spreader), 0.8 mm pitch 23 mm × 23 mm × 2.57 mm outline Purposely-placed ground pins for improved electrical grounding, mechanical strength, and thermal continuity

1.4 Chip subsystems

Table 1-5 lists all the subsystems of APQ8064E.

Table 1-5 APQ8064E chip subsystems

Feature	APQ8064E capability
Krait microprocessor subsystem	
Fast and power-efficient Krait cores	
ARM7 architecture extensions	Virtualization & 36-bit physical addressing
	QGIC2 interrupt controller includes virtualization extension ARM generic timer (QTIMER) 2nd-generation SAW (SAW2) Dynamic power management using SAW2 New address map to support security requirements
Quad Krait mP CPUs, each with:	Operating frequency up to 1.5 GHz 2 MB L2 cache 32 kB L1 instruction and data caches ARM v7 compliant TrustZone support VeNum 128-bit SIMD MM coprocessor
Shared L2 cache	2 MB, 8-way set associative with ECC Hardware-enforced coherency, including slave port Dual-interleaved AXI master ports increase memory BW L2 lines individually lockable to create virtual TCM
KMSS AHB	32-bit at 66 MHz Local connection from CPUs to memory High-BW multimedia traffic mostly localized to separate multimedia FABRIC Tiered arbitration to enable efficient bus/memory sharing with priority for CPUs
SDRAM memory	See Section 1.5 Memory Map
Multiple power and clock domains	Independent domains for µP1, µP2, µP3, µP4, and memories L2 data retention enables CPU power-collapse Independently-scalable clocks for each core and L2
Multimedia subsystem	
Major blocks:	Display support (red) Image processing (green) Graphics (orange) Audio
Graphics-acceleration hardware	Adreno 320 3D graphics engine for user interface, browsing, and gaming performance API support, including Open VG, Open GL ES 2.0, etc. Tiled 3D GPU architecture with 512 kB memory reduces DDR bandwidth requirements

Table 1-5 APQ8064E chip subsystems

Feature	APQ8064E capability
Other multimedia acceleration hardware	JPEG encode & JPEG decode Video preprocessing (VPE) Display preprocessing Display engine with in-line processing for HDMI support
Advanced bus fabric	128-bit wide FABRIC at 166 MHz for high-BW access to local multimedia memories Tiered arbitration enables efficient sharing of bus and memories
Encoder/decoder acceleration hardware	Multi-format decoder and encoder support up to 1080p at 30 fps Encode/decode function fully offloaded from applications CPUs Video performance for apps: broadcast TV, movie playback, web browsing, and camcorder
Multimedia DDR memory	See Section 1.5 Memory Map
Low-power audio subsystem (LPASS)	
Power efficient audio processing	New QDSP6v4 core New SLIMbus interfaces ■ Approximately 24 Mbps of uncompressed audio data bandwidth ■ SLIMbus includes customized slew-rate limited IOs Support for up to 6 digital microphones
Low-power features	Power gating within LPASS core QDSP6 supports L2 cache data retention during power collapse Supported modes: ACTIVE / IDLE / DORMANT / OFF
Clock control	Local clock control with dedicated PLL
Low-power memory	Dedicated SRAM Bitstream buffer, PCM buffers, DSP OS
Musical Instrument Digital Interface (MIDI)	Acceleration HW 128-poly MIDI processing
Audio DSP	Near-zero cache miss-rates during steady-state low-power audio playback Separate voltage domain is scaled with performance requirements
Audio interfaces	PCM, DMIC, MI^{2}S/I^{2}S legacy low-power audio interfaces
Smart Peripheral Subsystem (SPSS)	
SPSS improves peripheral operations that require significant main CPU and system DRAM involvement (high loading) - power optimized architecture for higher throughput at lower power dissipation	Decentralized, very scalable architecture High-throughput peripheral devices are concentrated in a semi-autonomous subsystem
General SPSS features	Hardware clock-gating Dedicated buses with performance monitoring Security features based on virtual master ID implementation Dynamic bus scaling (HS-USB requires 60 MHz+)
DMA accelerator interface	

Table 1-5 APQ8064E chip subsystems

Feature	APQ8064E capability
Pipe memory	Producers and consumers communicate through unidirectional pipes Memory and configuration parameters
Sensor processor	ARM7 up to 64 MHz with 176 kB TCM
Bus access manager (BAM)	Manages data transfers between the peripheral and the pipe memory
Crypto4	Used to encrypt/decrypt content to/from SD and USB devices
Sensor-specific features	Centralized hub with dedicated memory Interfaces for several sensors, different types BOM reduction, low-cost sensors Low-latency response Reduced software complexity 24 x 7 applications, such as pedometer
Chip peripheral subsystem	
USB features: 3 controller types	The primary controller has three HS-USB ports with an integrated physical layer (PHY). These ports can support USB operations at low-speed and full-speed. The second controller type is HSIC. The third controller type is FS-USB (full-speed, or 12 Mbps), used only for the UICC, Additional USB information is available at www.usb.org/developers/.
TSIF features	
Transport stream interfaces	APQ8064E has two transport stream interfaces for communication with broadcast ICs Each TSIF bus consists of CLK, data, En and sync lines
Format	Specified by IEC 13818-1 and is the MPEG 2 TS format
Frequency	27 MHz

1.5 The memory map

The system memory map is shown in Figure 1-2.

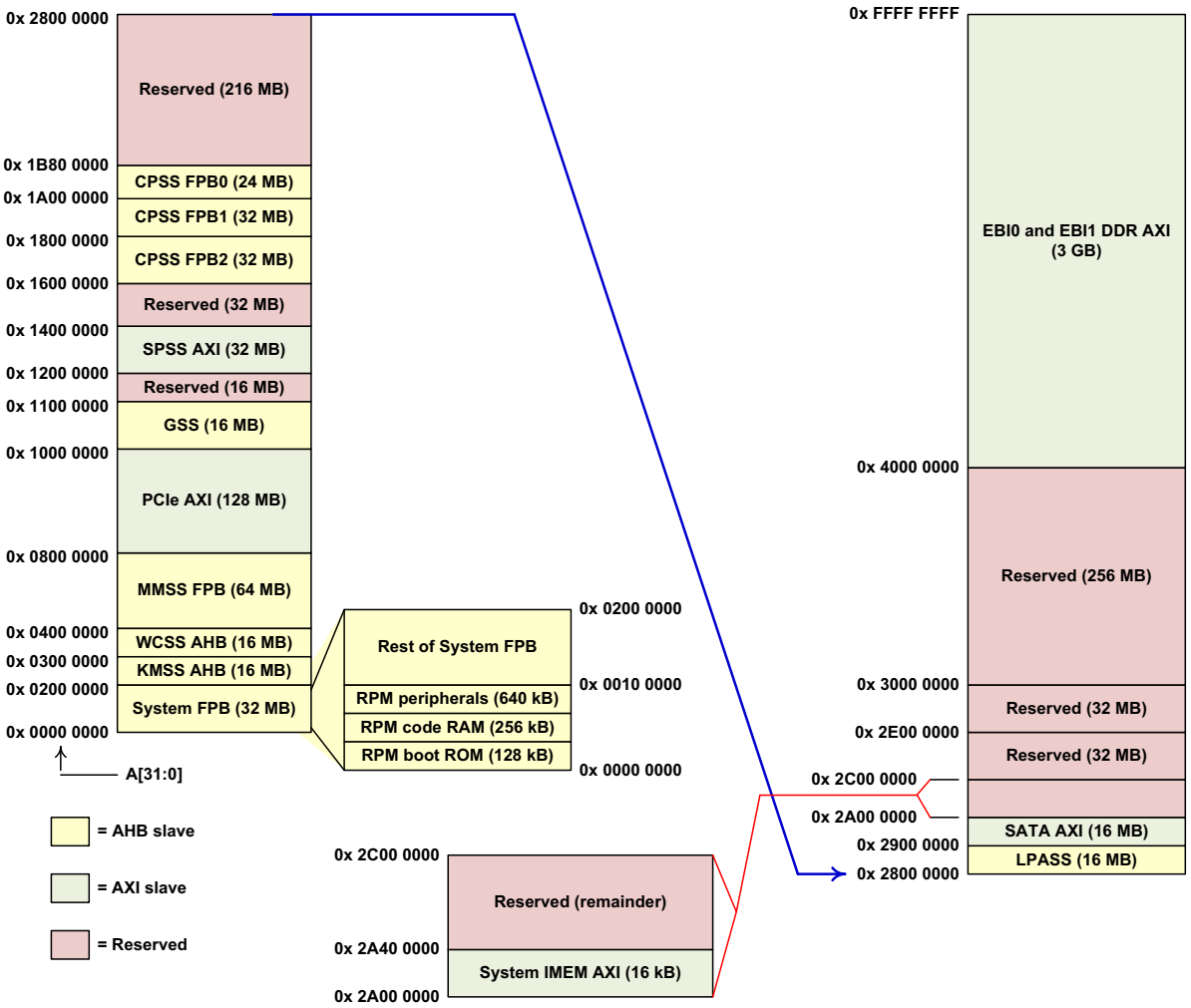


Figure 1-2 Memory map

1.5.1 Memory controller

See Section Section 3.9 Memory support.

1.5.2 eMMC NAND flash on SDC

The eMMC is the primary boot device (see Boot modes in Section 1.6.1) and is connected to Secure Digital Card Controller 3 (SDC3) through an 8-bit SDIO bus. See Section 3.9.4 eMMC NAND flash on SDIO.

1.6 Device configurations

1.6.1 Boot modes

Table 1-6 lists the various boot_config options.

Table 1-6 BOOT_CONFIG pin options 1 through 5

Option	FAST_ BOOT_ SELECT fuse	OEM_ SECURE_ BOOTn fuse	BOOT_ CONFIG [6] GPIO status	BOOT_CONFIG[5:0] GPIO status	Secure boot enabled	Advantages and use-case
1	Blown	Blown	Don't care	1. BOOT_CONFIG[5:0] pin state is ignored. 2. BOOT_CONFIG pins can be re-purposed as GPIOs. 3. Fast boot device is selected by the FAST_BOOT_SELECT fuse blown values set by software. 4. SECURE_BOOT configuration is controlled by the OEM_SECURE_ BOOTn (n = 1...28) fuse settings. 5. AUTH_EN, TABLE_SEL, and KEY_SEL bits of the enabled configuration are selected by blowing these bits of the selected OEM_SECURE_BOOTn fuse settings. 6. OEM_SECURE_BOOT1 is supported.	Yes **Recom-mended solution for production environment**	Fixed, most secure and recommended solution for production environment. Less components are required (removal of pull-ups on BOOT_CONFIG pins), reduces BOM cost and PCB area.
2	Not blown	Not blown	1	1. Fast boot device is selected by BOOT_ CONFIG[4:0] combinations as shown in Table 1-7. 2. BOOT_CONFIG[5] is not used.	No	Allows boot device flexibility (for example, USB vs. eMMC) and is intended for use in R&D stage. Device boots up in non-secure mode.
3	Not blown	Blown	1	1. Fast boot device is selected by BOOT_ CONFIG[4:0] combinations as shown in the Table 1-7. 2. BOOT_CONFIG[5] is not used. 3. Secure Boot Authentication is controlled by OEM_SECURE_BOOTn fuses.	Yes	Allows boot device flexibility (for example, USB vs. eMMC) and is intended for use in R&D stage. Device boots up in secure mode.

Table 1-6 BOOT_CONFIG pin options 1 through 5

Option	FAST_ BOOT_ SELECT fuse	OEM_ SECURE_ BOOTn fuse	BOOT_ CONFIG [6] GPIO status	BOOT_CONFIG[5:0] GPIO status	Secure boot enabled	Advantages and use-case
4	Blown	Not blown	0	1. Status of BOOT_CONFIG[4:0] pins as shown in the Table 1-8 determines which OEM_SECURE_BOOTn region is turned on by selecting the specific AUTH_EN bit of that region. **Note:** In option 1 – AUTH_EN bit is blown in the fuse settings. 2. OEM_SECURE_BOOT1 is supported. 3. TABLE_SEL and KEY_SEL bits of the enabled configuration are selected by blowing these bits in the OEM_ SECURE_BOOTn fuse settings. 4. Fast boot device is selected by the FAST_BOOT_SELECT fuse blown values set by software.	Yes	Recommended to be used for a fixed boot device (example – eMMC only) and for authentication testing in R&D stage. Device boots up in secure mode if the OEM_SECURE_BOOT1 region is turned on.
5	Not blown	Blown	0	1. Status of BOOT_CONFIG[4:0] pins as shown on the Table 1-7 determines which OEM_ SECURE_BOOTn region is turned on by selecting the specific AUTH_EN bit of that region. **Note:** In option 1 – AUTH_EN bit is blown in the fuse settings. 2. OEM_SECURE_BOOT1 is supported. Refer to Note 1 on the Table 1-7. 3. TABLE_SEL and KEY_SEL bits of the enabled configuration are selected by blowing these bits in the OEM_ SECURE_BOOTn fuse settings. 4. Fast boot device is the default boot device (SDC3).	Yes	Device boots up with the default boot device (SDC3). Boot device cannot be changed. Device boots up in secure mode if the OEM_SECURE_BOOT1 region is turned on.

Table 1-7 Fast boot device selection by BOOT_CONFIG GPIOs

BOOT_CONFIG[5:0]	BOOT_CONFIG[6] = 1 = fast boot
0b000000	SDC3 followed by HS-USB
0b000001	SDC3 followed by SDC1
0b000010	SDC3 followed by SDC2
0b000011	SDC1(eMMC)
0b000100	SDC2

Table 1-8 Secure boot device selection by BOOT_CONFIG GPI

BOOT_CONFIG[5:0]	BOOT_CONFIG[6] = 0 = secure boot
0b000000	No secure boot, as BOOT_CONFIG[4:0] = 0
0b000001	Secure boot1 from OEM_SECURE_BOOT1 configuration
0b000010	Secure boot2 from OEM_SECURE_BOOT2 configuration
0b000011	Secure boot3 from OEM_SECURE_BOOT3 configuration
0b000100	Secure boot4 from OEM_SECURE_BOOT4 configuration

1.6.2 Device clocking

1.6.2.1 Clock architecture

Figure 1-3 illustrates the APQ8064E clock architecture. For details, see the *Qualcomm Snapdragon 600E (APQ8064E) Clock Plan*, LM80-P0598-15.

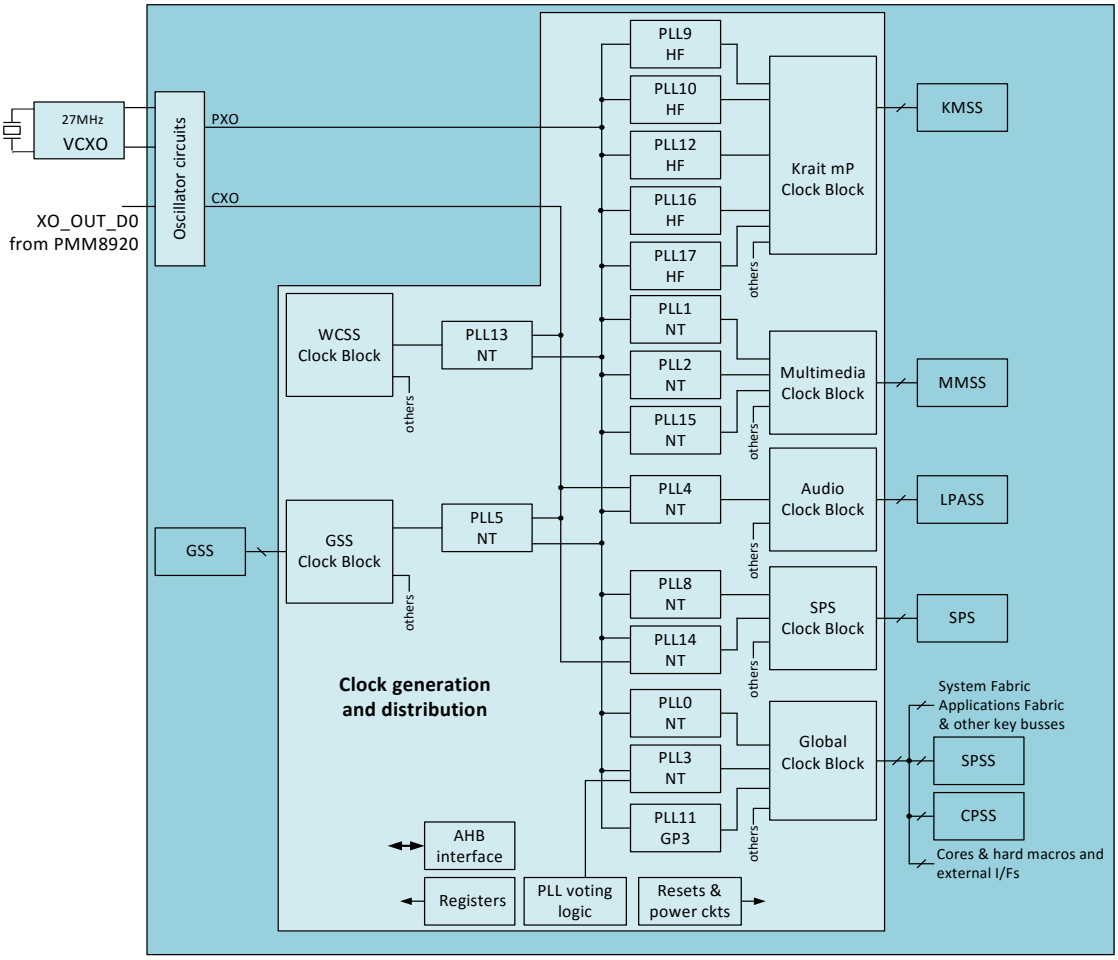


Figure 1-3 Clock architecture

NOTE PLL13 is only used if the WCN3660 XO is not used.

1.6.2.2 Phased-locked loops

- Types
  - General purpose (GP3)
  - Low power (NT)
  - High frequency (HF)

- Four PLLs have an option to use CXO, all others use PXO
- 16 PLLs total

1.6.2.3 Clock blocks

- Inputs include the oscillator signals, PLL signals, and test sources.
- Various clock-circuit types generate all clocks needed by the system.
- Clock outputs are organized into clock regimes.
- Three clock blocks are dedicated to specific systems or subsystems.
- One clock block serves multiple systems and subsystems, in addition to buses, hardware cores, hard macros, and external interfaces.

1.6.2.4 Clock regimes

Clock regimes are defined as collections of clock signals that drive sets of circuit cores or blocks having similar clock requirements.

Table 1-9 Clock regimes

Clock regime	Highest frequency	Frequency range
Apps fabric	533 MHz turbo mode 400 MHz normal	27 to 533 MHz; other selections available within this range
System fabric	160 MHz normal mode	Integer divide of different PLLs
SPSS fabric	64 MHz	64 MHz and integer divide of PLL8
RPM system FPB	64 MHz	64 MHz and integer divide of PLL8
CPSS FPBs	64 MHz	64 MHz and integer divide of PLL8
Multimedia fabric	220 MHz	200 MHz and integer divide of PLL8
MMSS FPB	83 MHz	83 MHz and integer divide of PLL8
EBI	533 MHz	27 to 533 MHz; other selections available in this range

1.6.2.5 Supported by digital control functions

- AHB interface, registers, reset circuits, and power control circuits: enables subsystem configuration, control, and status
- PLL voting logic:
  - Processors cast votes to enable their PLLs
  - Vote-to-enable scheme prevents one processor from denying another processor’s PLL
  - State machine implements control without software intervention

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

1.6.4 Device reset

Four types of reset; available resets depend on the boot mode (Boot Overview):

- Cold boot
  - Poweron reset via PMIC (IC-level Interfaces)
- Warm boot
  - Watchdog-expired reset
  - Software system reset through register write

1.7 System interconnect (FABRIC)

The APQ8064E device uses a tiered interconnect:

- Provides a low latency path from the Krait processor subsystem (KPSS) to the external EBI1 memory
- System FABRIC is the main system bus with all the masters and slaves connected to it directly or through other interconnects
  - The system FABRIC can be run at a maximum clock frequency of 133 MHz at 0.945 V and 177 MHz at 1.055 V
  - 15 x 15 system FABRIC: Bus ID = 1; 133 MHz Operation; 64-bit internal bus

Table 1-10 lists the subtending FABRIC configurations that system FABRIC interconnects.

Table 1-10 FABRIC configurations

	Bus ID	Operation	Internal bus
3 x 4 FABRIC	0	64 MHz	32-bit
13 x 3 Multimedia subsystem	3	166 MHz	128-bit
6 x 5 Apps FABRIC	2	400 MHz	64-bit

1.8 Terms and acronyms

Table 1-11 defines terms and acronyms commonly used throughout this document.

Table 1-11 Terms and acronyms

Term	Definition
ADC	Analog-to-digital converter
AES	Advanced encryption standard
AHB	AMBA high-speed bus
AHPB	Advanced high performance bus
AMR	Absolute maximum rating
API	Application programming interface
APQ	Application processor Qualcomm
AR	Area ratio
ARM	Advanced RISC machines
AVS	Adaptive voltage scaling
AXI	Advanced extensible interface
BAM	Bus access manager
bps	bits per second
BT	Bluetooth
BW	Bandwidth

Table 1-11 Terms and acronyms (cont.)

Term	Definition
CCD	Charged coupled device
CMOS	Complementary metal oxide semiconductor (a type of temporary memory)
CMX	Compact multimedia extension
CPSS	Chip peripheral subsystem
CRC	Cyclic redundancy code
CRCI	Channel rate control interface
CSIM	CDMA subscriber identify module
CSI	Camera serial interface
CSTN	Color super twisted nematic
CXO	Clock crystal oscillator
DAC	Digital-to-analog converter
DDR	Double data rate
DFSD	Design for software debug
DMA	Direct memory access
DMIC	Digital Microphone
DRAM	Dynamic random access memory
DRM	Digital rights management
DSI	Display serial interface
DSP	Digital signal processor
DTS	Digital test sequence or source
EB	External bus
EBI	External bus interface
ECC	Error-correcting code
EDR	Enhanced data rate
eMMC	Embedded multimedia card
ETM	Embedded trace macrocell
FABRIC	Flexible advanced bus and reusable interconnect cores.
FCBGA+HS	Flip-chip ball grid array + heat spreader
FPB	Fast peripheral bus
GLONASS	Global orbiting navigation satellite system
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPS	Global positioning system
GPU	Graphics processing unit
GSBI	General serial bus interface
HDCP	High-bandwidth digital content protection

Table 1-11 Terms and acronyms (cont.)

Term	Definition
HDMI	High-definition multimedia interface
HSIC	High-speed inter-chip
I^2C	Inter-integrated circuit
I^2S	Inter-IC sound
IS-801	3GPP2 C.S022/TIA (IS-801): Position determination service standard for dual mode spread spectrum systems, 2004
IS-881	3GPP2 X.S0002/TIA PN4747 (IS-881): Third generation partnership program; map location services enhancements, 2002
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
kbps	kilobits per second
KMSS	Krait multiprocessor subsystem
LCC	LPASS clock controller
LCD	Liquid crystal display
LDPC	Low density parity check
LMEM	Local memory
LPA	Low-power audio
LPASS	Low-power audio subsystem
LPDDR	Low-power double data rate
LSbit or LSByte	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
LTPS	Low temperature polysilicon LCD
LVDS	Low-voltage differential signaling
MDP	Mobile display processor
MHL	Mobile hi-definition link
MIDI	Musical instrument digital interface
MIMEM	Multimedia internal memory
MIPI	Mobile industry processor interface
ML	Maximum likelihood
MMC	Multimedia card
MPM	Master power management
MRC	Maximum ratio combining
MSbit or MSByte	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
NAND	Memory with logic cells similar to Not AND gates
NFC	Near-field communication
NSP	Nanoscale package

Table 1-11 Terms and acronyms (cont.)

Term	Definition
OLED	Organic light-emitting diode
OMA	Open mobile architecture
OpenGL ES	OpenGL ES (graphics library embedded systems)
Open VG	Open vector graphics
PCIe	Peripheral component interconnect express
PCM	Pulse-coded modulation
PDM	Pulse-density modulation
PHY	Physical layer
PLL	Phase-locked loop
PM	Power management
PMIC	Power management integrated circuit
PXO	Platform crystal oscillator
QDSP6	Qualcomm digital signal processor, 6th-generation
QFPROM	Qualcomm fuse programmable read-only memory
QGIC	Qualcomm generic interrupt controller
QTI	Qualcomm Technologies, Inc.
QXGA	Quad extended graphics array (2048 × 1536)
RGB	Red-green-blue
RGR	RF GPS receiver
RPM	Resource and power manager
SBI	Serial bus interface
SD	Secure digital
SDC	Secure digital card
SDCC	Secure digital card controller
SDIO	Secure digital input output
SRAM	Static random access memory
SDRAM	Synchronous dynamic random access memory
SFS	Secure file system
SIM	Subscriber identity module
SIMD	Single instruction multiple data
SMIA	Standard mobile imaging architecture
SMT	Surface mount technology
SPI	Serial peripheral interface
SPM	Subsystem power manager
SPS	Sensor processor subsystem
sps	Symbols per second (or samples per second)

Table 1-11 Terms and acronyms (cont.)

Term	Definition
SPSS	Smart peripheral subsystem
SROT	Secure root of trust
SSBI	Single-wire serial bus interface
SSL	Secure sockets layer
STBC	Space time block coding
TAP	Test access port
TCM	Tightly coupled memory
TCXO	Temperature-compensated crystal oscillator
TLMM	Top-level mode multiplexer
TSIF	Transport stream interface
TxBF	Transmit beamforming
UART	Universal asynchronous receiver transmitter
UICC	Universal integrated circuit card
UIM	User identity module
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
USB-OTG	Universal serial bus on-the-go
USIM	UMTS subscriber identity module
UICC	Universal integrated circuit card
VPE	Video preprocessing
WCA	Wireless connectivity and analog functions
WCN	Wireless connectivity network
WLAN	Wireless local area network
WMA	Windows media audio (file type)
WXGA	Wide extended graphics array (1280 x 800)
XO	Crystal oscillator

1.9 Special marks

Table 1-12 defines special marks used in this document.

Table 1-12 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, EBI2_AD_[7:4] indicates a range that is 4 bits in length, or DATA[7:0] refers to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10), unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, for example, 0011 (binary).
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin definitions

2.1 APQ8064E pin assignments

2.1.1 APQ8064E pin maps

The APQ8064E device is available in the 784-pin flip-chip BGA package (784 FCBGA+HS) that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

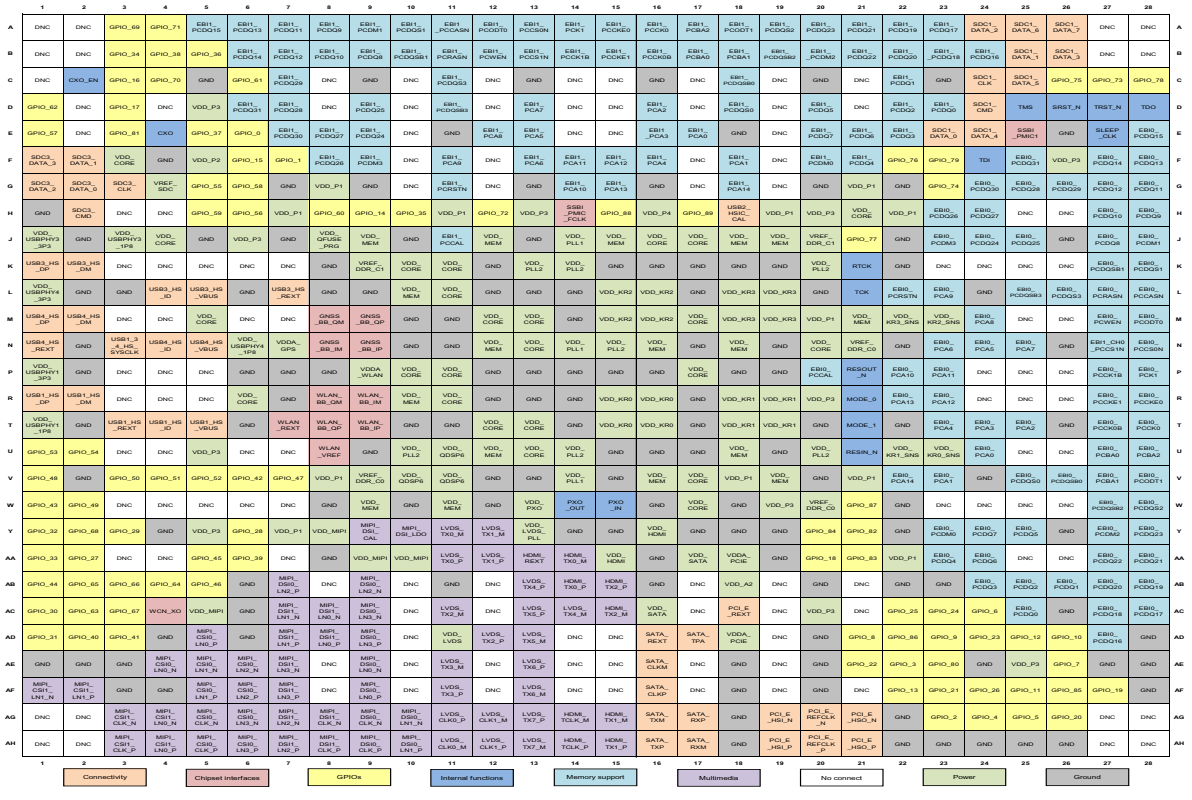
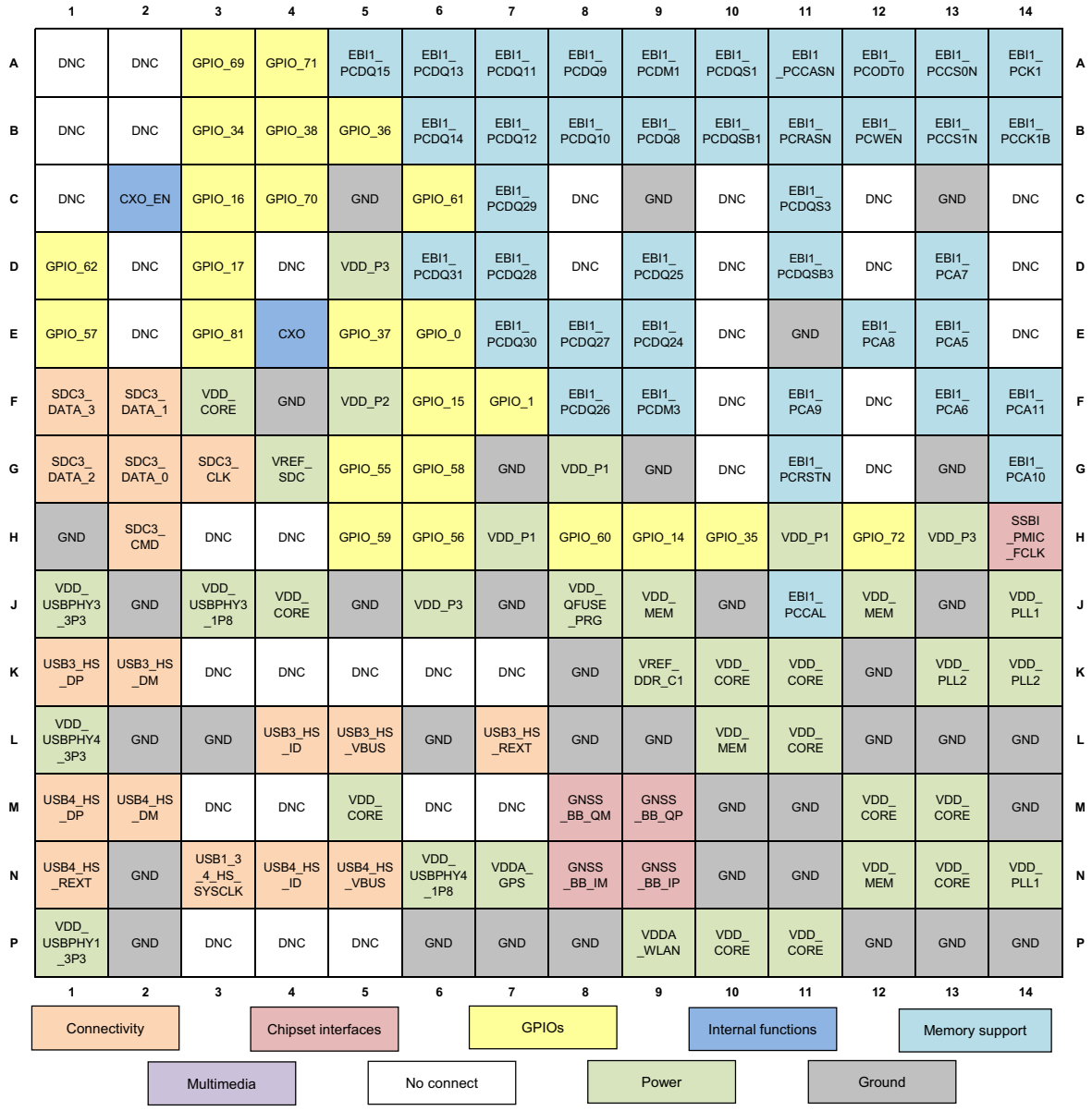


Figure 2-1 APQ8064E pin assignments (top view)

Since the text within Figure 2-1 is very difficult to read, close-up views of each quadrant are shown in Figure 2-2 through Figure 2-5.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DNC	DNC	GPIO_69	GPIO_71	EBI1_ PCDQ15	EBI1_ PCDQ13	EBI1_ PCDQ11	EBI1_ PCDQ9	EBI1_ PCDM1	EBI1_ PCDQS1	EBI1 _PCCASN	EBI1_ PCODT0	EBI1_ PCCS0N	EBI1_ PCK1	A
B	DNC	DNC	GPIO_34	GPIO_38	GPIO_36	EBI1_ PCDQ14	EBI1_ PCDQ12	EBI1_ PCDQ10	EBI1_ PCDQ8	EBI1_ PCDQSB1	EBI1_ PCRASN	EBI1_ PCWEN	EBI1_ PCCS1N	EBI1_ PCCK1B	B
C	DNC	CXO_EN	GPIO_16	GPIO_70	GND	GPIO_61	EBI1_ PCDQ29	DNC	GND	DNC	EBI1_ PCDQS3	DNC	GND	DNC	C
D	GPIO_62	DNC	GPIO_17	DNC	VDD_P3	EBI1_ PCDQ31	EBI1_ PCDQ28	DNC	EBI1_ PCDQ25	DNC	EBI1_ PCDQSB3	DNC	EBI1_ PCA7	DNC	D
E	GPIO_57	DNC	GPIO_81	CXO	GPIO_37	GPIO_0	EBI1_ PCDQ30	EBI1_ PCDQ27	EBI1_ PCDQ24	DNC	GND	EBI1_ PCA8	EBI1_ PCA5	DNC	E
F	SDC3_ DATA_3	SDC3_ DATA_1	VDD_ CORE	GND	VDD_P2	GPIO_15	GPIO_1	EBI1_ PCDQ26	EBI1_ PCDM3	DNC	EBI1_ PCA9	DNC	EBI1_ PCA6	EBI1_ PCA11	F
G	SDC3_ DATA_2	SDC3_ DATA_0	SDC3_ CLK	VREF_ SDC	GPIO_55	GPIO_58	GND	VDD_P1	GND	DNC	EBI1_ PCRSTN	DNC	GND	EBI1_ PCA10	G
H	GND	SDC3_ CMD	DNC	DNC	GPIO_59	GPIO_56	VDD_P1	GPIO_60	GPIO_14	GPIO_35	VDD_P1	GPIO_72	VDD_P3	SSBI _PMIC _FCLK	H
J	VDD_ USBPHY3 _3P3	GND	VDD_ USBPHY3 _1P8	VDD_ CORE	GND	VDD_P3	GND	VDD_ QFUSE _PRG	VDD_ MEM	GND	EBI1_ PCCAL	VDD_ MEM	GND	VDD_ PLL1	J
K	USB3_HS _DP	USB3_HS _DM	DNC	DNC	DNC	DNC	DNC	GND	VREF_ DDR_C1	VDD_ CORE	VDD_ CORE	GND	VDD_ PLL2	VDD_ PLL2	K
L	VDD_ USBPHY4 _3P3	GND	GND	USB3_HS _ID	USB3_HS _VBUS	GND	USB3_HS _REXT	GND	GND	VDD_ MEM	VDD_ CORE	GND	GND	GND	L
M	USB4_HS _DP	USB4_HS _DM	DNC	DNC	VDD_ CORE	DNC	DNC	GNSS _BB_QM	GNSS _BB_QP	GND	GND	VDD_ CORE	VDD_ CORE	GND	M
N	USB4_HS _REXT	GND	USB1_3 _4_HS_ SYSCLK	USB4_HS _ID	USB4_HS _VBUS	VDD_ USBPHY4 _1P8	VDDA_ GPS	GNSS _BB_IM	GNSS _BB_IP	GND	GND	VDD_ MEM	VDD_ CORE	VDD_ PLL1	N
P	VDD_ USBPHY1 _3P3	GND	DNC	DNC	DNC	GND	GND	GND	VDDA _WLAN	VDD_ CORE	VDD_ CORE	GND	GND	GND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 2-2 APQ8064E assignments – upper left quadrant

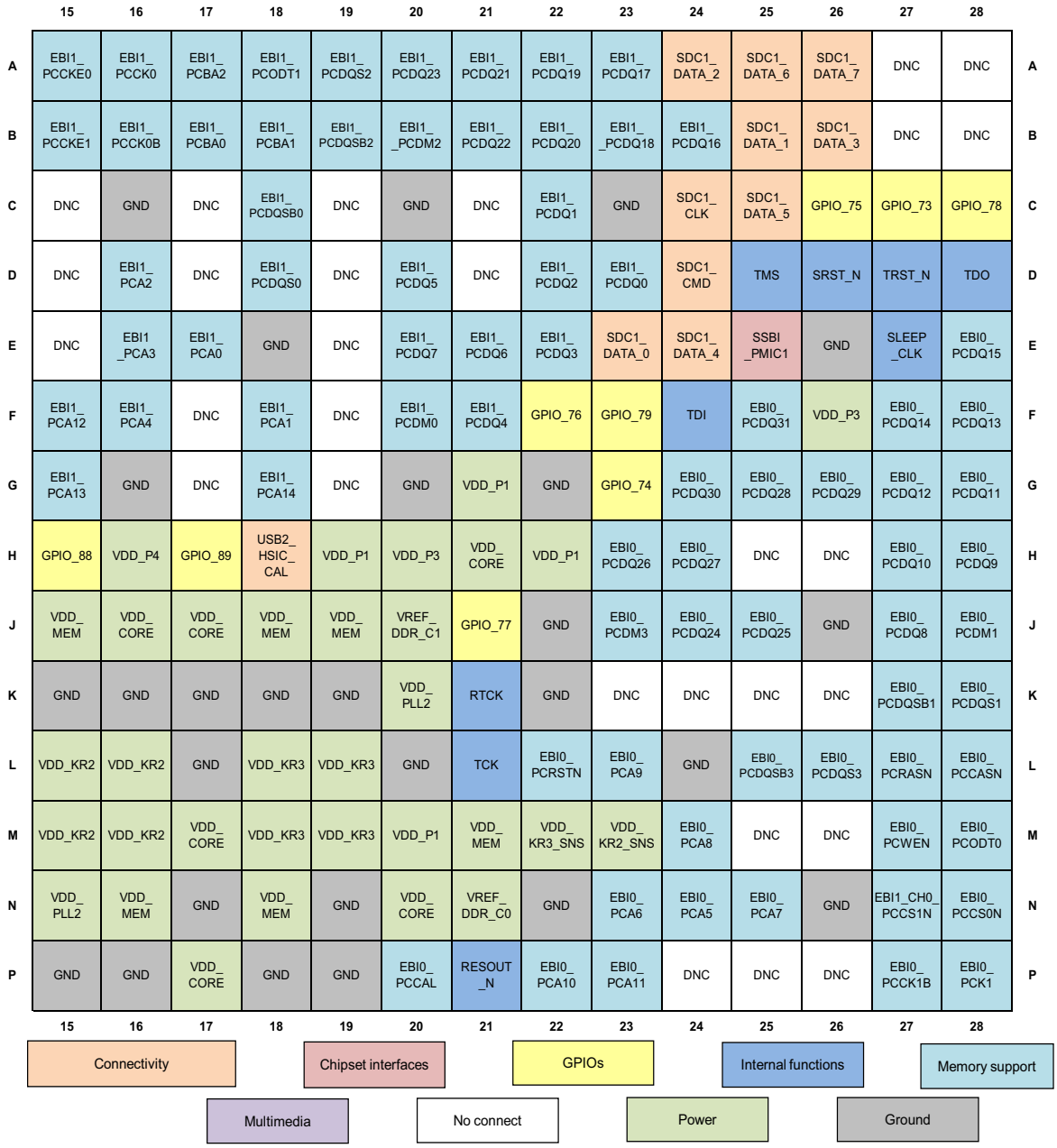


Figure 2-3 APQ8064E pin assignments – upper right quadrant

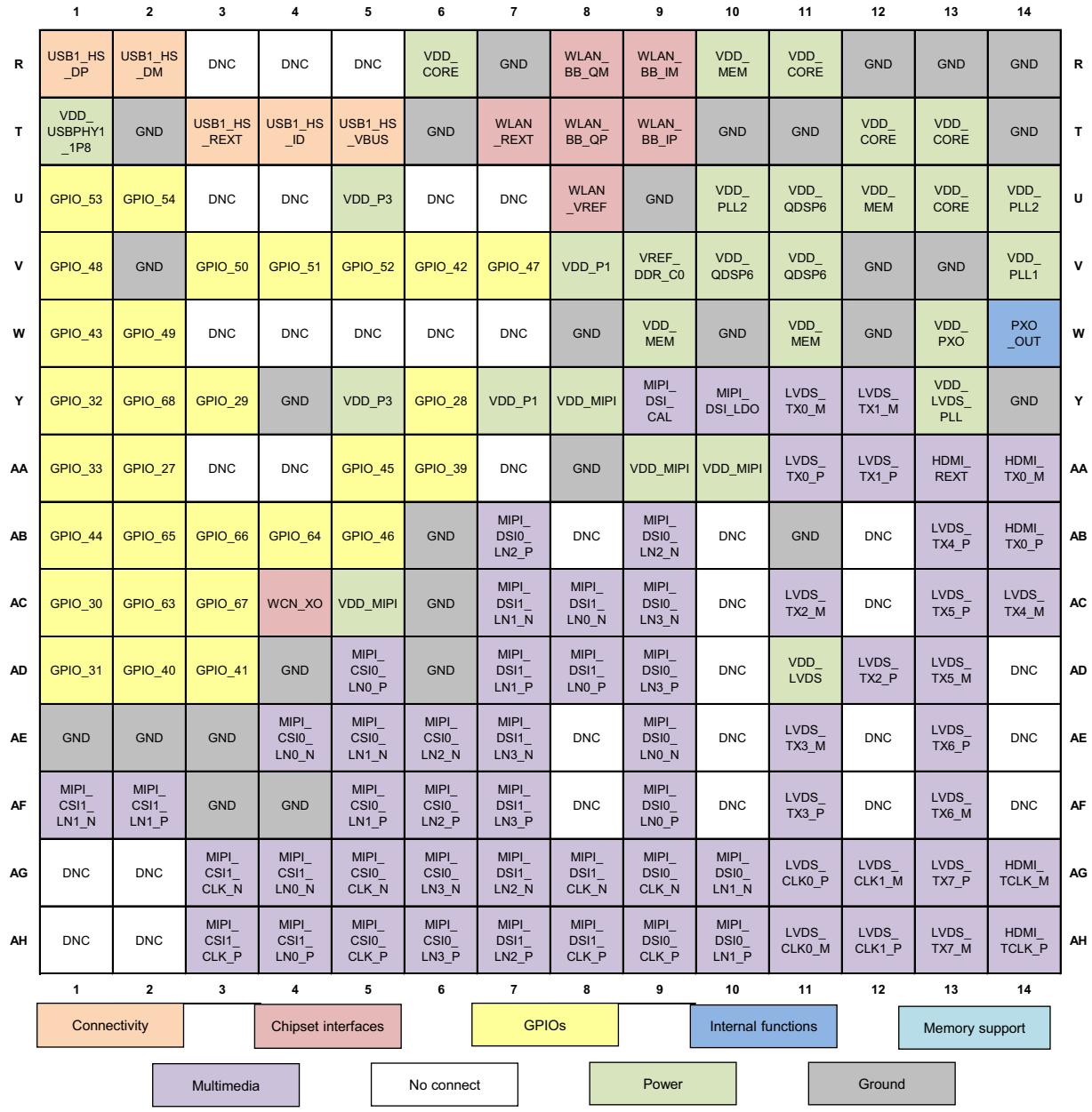


Figure 2-4 APQ8064E assignments – lower left quadrant

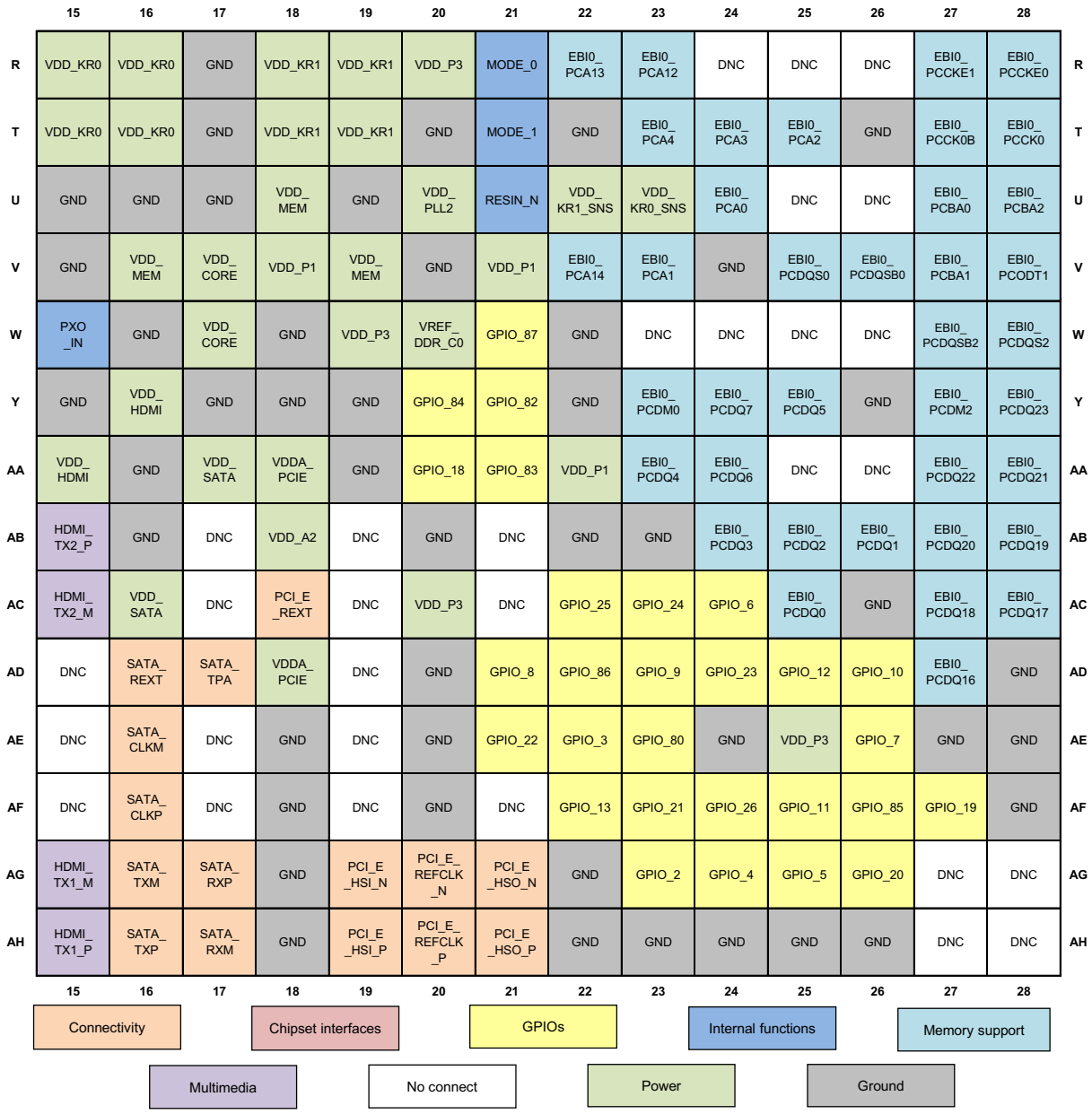


Figure 2-5 APQ8064E pin assignments – lower right quadrant

2.2 I/O parameter definitions

Use the descriptions listed in Table 2-1 to understand the pin types column displayed in the following tables.

Table 2-1 I/O description (pin type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
W	Wakeup interrupt during deep-sleep mode
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad-pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pulldown with programmable options following the colon (:) PU: nppdkp = default pullup with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pullup device
PD	Contains an internal pulldown device
Pad voltage groupings for baseband circuits	
P1	Pad group 1 (EBI0 and EBI1); tied to VDD_P1 pins (1.35–1.5 V only)
P2	Pad group 2 (SDC3); tied to VDD_P2 pins (1.8 V or 2.85 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P4	Pad group 4 (HSIC); tied to VDD_P4 pins (1.8 V only)
Output current drive strength	
EBI0 and EBI1 pads	Pads for EBI0 and EBI1 are tailored for 1.35–1.5 V interfaces and are source terminated. At the pads, after the source termination, the drive strength at I_{OL}, I_{OH} is equivalent to a range of 0.8 to 2.5 mA in nonlinear steps when the JEDEC standard range (90%/10%) is followed.
3.0 V (H) pads	Programmable drive strength, 2 to 8 mA in 2 mA steps
Others [1]	Programmable drive strength, 2 to 16 mA in 2 mA steps

1. Digital pads other than EBI0 and EBI1 pads.

2.2.1 Pin descriptions

Descriptions of the pins are presented in the following tables, organized by functional group:

Table 2-2: Memory support functions

Table 2-3: Multimedia functions

Table 2-4: Connectivity functions

Table 2-5: Internal functions

Table 2-6: APQ8064E wakeup pins

Table 2-7: Chipset interface functions

Table 2-8: General-purpose input/output ports

Table 2-9: GSBI configurations: seven 4-pin sets of GPIOs are available as general serial bus interface ports that can be configured for UART, UIM, SPI, or I^2C operation

Table 2-10: Channel rate control interface (CRCI) assignments

Table 2-11: No connection, do not connect, and reserved pins

Table 2-12: Power supply pins

Table 2-13: Ground pins

Table 2-2 APQ8064E pin descriptions – memory support functions

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
EBI0 for DDR3 SDRAM block 1, channel 0					
U24	EBI0_PCA0		P1	DO	DDR3 block 1, channel 0 command/address bit 0
V23	EBI0_PCA1		P1	DO	DDR3 block 1, channel 0 command/address bit 1
T25	EBI0_PCA2		P1	DO	DDR3 block 1, channel 0 command/address bit 2
T24	EBI0_PCA3		P1	DO	DDR3 block 1, channel 0 command/address bit 3
T23	EBI0_PCA4		P1	DO	DDR3 block 1, channel 0 command/address bit 4
N24	EBI0_PCA5		P1	DO	DDR3 block 1, channel 0 command/address bit 5
N23	EBI0_PCA6		P1	DO	DDR3 block 1, channel 0 command/address bit 6
N25	EBI0_PCA7		P1	DO	DDR3 block 1, channel 0 command/address bit 7
M24	EBI0_PCA8		P1	DO	DDR3 block 1, channel 0 command/address bit 8
L23	EBI0_PCA9		P1	DO	DDR3 block 1, channel 0 command/address bit 9
P22	EBI0_PCA10		P1	B	DDR3 block 1, channel 0 command/address bit 10
P23	EBI0_PCA11		P1	B	DDR3 block 1, channel 0 command/address bit 11
R23	EBI0_PCA12		P1	B	DDR3 block 1, channel 0 command/address bit 12
R22	EBI0_PCA13		P1	B	DDR3 block 1, channel 0 command/address bit 13
V22	EBI0_PCA14		P1	B	DDR3 block 1, channel 0 command/address bit 14
U27	EBI0_PCBA0		P1	B	DDR3 block 1, channel 0 byte access bit 0
V27	EBI0_PCBA1		P1	B	DDR3 block 1, channel 0 byte access bit 1

Table 2-2 APQ8064E pin descriptions – memory support functions (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
U28	EBI0_PCBA2		P1	B	DDR3 block 1, channel 0 byte access bit 2
P20	EBI0_PCCAL		P1	B	DDR3 block 1, channel 0 I/O calibration pad
L28	EBI0_PCCASN		P1	B	DDR3 block 1, channel 0 CAS
T28	EBI0_PCCK0		P1	B	DDR3 block 1, channel 0 differential clock 0 (+)
T27	EBI0_PCCK0B		P1	B	DDR3 block 1, channel 0 differential clock 0 (-)
P27	EBI0_PCCK1B		P1	B	DDR3 block 1, channel 0 differential clock 1 (-)
R28	EBI0_PCCKE0		P1	B	DDR3 block 1, channel 0 clock enable bit 0
R27	EBI0_PCCKE1		P1	B	DDR3 block 1, channel 0 clock enable bit 1
N28	EBI0_PCCS0N		P1	B	DDR3 block 1, channel 0 chip select bit 0
N27	EBI0_PCCS1N		P1	B	DDR3 block 1, channel 0 chip select bit 1
Y23	EBI0_PCDM0		P1	B	DDR3 block 1, channel 0 data mask bit 0
J28	EBI0_PCDM1		P1	B	DDR3 block 1, channel 0 data mask bit 1
Y27	EBI0_PCDM2		P1	B	DDR3 block 1, channel 0 data mask bit 2
J23	EBI0_PCDM3		P1	B	DDR3 block 1, channel 0 data mask bit 3
AC25	EBI0_PCDQ0		P1	B	DDR3 block 1, channel 0 data bit 0
AB26	EBI0_PCDQ1		P1	B	DDR3 block 1, channel 0 data bit 1
AB25	EBI0_PCDQ2		P1	B	DDR3 block 1, channel 0 data bit 2
AB24	EBI0_PCDQ3		P1	B	DDR3 block 1, channel 0 data bit 3
AA23	EBI0_PCDQ4		P1	B	DDR3 block 1 channel 0 data bit 4
Y25	EBI0_PCDQ5		P1	B	DDR3 block 1 channel 0 data bit 5
AA24	EBI0_PCDQ6		P1	B	DDR3 block 1 channel 0 data bit 6
Y24	EBI0_PCDQ7		P1	B	DDR3 block 1 channel 0 data bit 7
J27	EBI0_PCDQ8		P1	B	DDR3 block 1 channel 0 data bit 8
H28	EBI0_PCDQ9		P1	B	DDR3 block 1 channel 0 data bit 9
H27	EBI0_PCDQ10		P1	B	DDR3 block 1 channel 0 data bit 10
G28	EBI0_PCDQ11		P1	B	DDR3 block 1, channel 0 data bit 11
G27	EBI0_PCDQ12		P1	B	DDR3 block 1, channel 0 data bit 12
F28	EBI0_PCDQ13		P1	B	DDR3 block 1, channel 0 data bit 13
F27	EBI0_PCDQ14		P1	B	DDR3 block 1, channel 0 data bit 14
E28	EBI0_PCDQ15		P1	B	DDR3 block 1, channel 0 data bit 15
AD27	EBI0_PCDQ16		P1	B	DDR3 block 1, channel 0 data bit 16
AC28	EBI0_PCDQ17		P1	B	DDR3 block 1, channel 0 data bit 17
AC27	EBI0_PCDQ18		P1	B	DDR3 block 1, channel 0 data bit 18
AB28	EBI0_PCDQ19		P1	B	DDR3 block 1, channel 0 data bit 19
AB27	EBI0_PCDQ20		P1	B	DDR3 block 1, channel 0 data bit 20
AA28	EBI0_PCDQ21		P1	B	DDR3 block 1, channel 0 data bit 21
AA27	EBI0_PCDQ22		P1	B	DDR3 block 1, channel 0 data bit 22
Y28	EBI0_PCDQ23		P1	B	DDR3 block 1, channel 0 data bit 23
J24	EBI0_PCDQ24		P1	B	DDR3 block 1, channel 0 data bit 24
J25	EBI0_PCDQ25		P1	B	DDR3 block 1, channel 0 data bit 25

Table 2-2 APQ8064E pin descriptions – memory support functions (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
H23	EBI0_PCDQ26		P1	B	DDR3 block 1, channel 0 data bit 26
H24	EBI0_PCDQ27		P1	B	DDR3 block 1, channel 0 data bit 27
G25	EBI0_PCDQ28		P1	B	DDR3 block 1, channel 0 data bit 28
G26	EBI0_PCDQ29		P1	B	DDR3 block 1, channel 0 data bit 29
G24	EBI0_PCDQ30		P1	B	DDR3 block 1, channel 0 data bit 30
F25	EBI0_PCDQ31		P1	B	DDR3 block 1, channel 0 data bit 31
V25	EBI0_PCDQS0		P1	B	DDR3 block 1, channel 0 differential data strobe for byte 0 (+)
V26	EBI0_PCDQSB0		P1	B	DDR3 block 1, channel 0 differential data strobe for byte 0 (-)
K28	EBI0_PCDQS1		P1	B	DDR3 block 1, channel 0 differential data strobe for byte 1 (+)
K27	EBI0_PCDQSB1		P1	B	DDR3 block 1, channel 0 differential data strobe for byte 1 (-)
W28	EBI0_PCDQS2		P1	B	DDR3 block 1, channel 0 differential data strobe for byte 2 (+)
W27	EBI0_PCDQSB2		P1	B	DDR3 block 1, channel 0 differential data strobe for byte 2 (-)
L26	EBI0_PCDQS3		P1	B	DDR3 block 1, channel 0 differential data strobe for byte 3 (+)
L25	EBI0_PCDQSB3		P1	B	DDR3 block 1, channel 0 differential data strobe for byte 3 (-)
P28	EBI0_PCK1		P1	B	DDR3 block 1, channel 0 differential clock (+)
M28	EBI0_PCODT0		P1	B	DDR3 block 1, channel 0 ODT bit 0
V28	EBI0_PCODT1		P1	B	DDR3 block 1, channel 0 ODT bit 1
L27	EBI0_PCRASN		P1	B	DDR3 block 1, channel 0 RAS
L22	EBI0_PCRSTN		P1	B	DDR3 block 1, channel 0 reset
M27	EBI0_PCWEN		P1	B	DDR3 block 1, channel 0 write enable
EBI1 for DDR3 SDRAM block 1, channel 1					
E17	EBI1_PCA0		P1	DO	DDR3 block 1, channel 1 command/address bit 0
F18	EBI1_PCA1		P1	DO	DDR3 block 1, channel 1 command/address bit 1
D16	EBI1_PCA2		P1	DO	DDR3 block 1, channel 1 command/address bit 2
E16	EBI1_PCA3		P1	DO	DDR3 block 1, channel 1 command/address bit 3
F16	EBI1_PCA4		P1	DO	DDR3 block 1, channel 1 command/address bit 4
E13	EBI1_PCA5		P1	DO	DDR3 block 1, channel 1 command/address bit 5
F13	EBI1_PCA6		P1	DO	DDR3 block 1, channel 1 command/address bit 6
D13	EBI1_PCA7		P1	DO	DDR3 block 1, channel 1 command/address bit 7
E12	EBI1_PCA8		P1	DO	DDR3 block 1, channel 1 command/address bit 8
F11	EBI1_PCA9		P1	DO	DDR3 block 1, channel 1 command/address bit 9
G14	EBI1_PCA10		P1	B	DDR3 block 1, channel 1 command/address bit 10
F14	EBI1_PCA11		P1	B	DDR3 block 1, channel 1 command/address bit 11
F15	EBI1_PCA12		P1	B	DDR3 block 1, channel 1 command/address bit 12
G15	EBI1_PCA13		P1	B	DDR3 block 1, channel 1 command/address bit 13
G18	EBI1_PCA14		P1	B	DDR3 block 1, channel 1 command/address bit 14
B17	EBI1_PCBA0		P1	B	DDR3 block 1, channel 1 byte access bit 0
B18	EBI1_PCBA1		P1	B	DDR3 block 1, channel 1 byte access bit 1
A17	EBI1_PCBA2		P1	B	DDR3 block 1, channel 1 byte access bit 2
J11	EBI1_PCCAL		P1	B	DDR3 block 1, channel 1 I/O calibration pad

Table 2-2 APQ8064E pin descriptions – memory support functions (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
A11	EBI1_PCCASN		P1	B	DDR3 block 1, channel 1 CAS
A16	EBI1_PCCK0		P1	B	DDR3 block 1, channel 1 differential clock 0 (+)
B16	EBI1_PCCK0B		P1	B	DDR3 block 1, channel 1 differential clock 0 (-)
B14	EBI1_PCCK1B		P1	B	DDR3 block 1, channel 1 differential clock 1 (-)
A15	EBI1_PCCKE0		P1	B	DDR3 block 1, channel 1 clock enable bit 0
B15	EBI1_PCCKE1		P1	B	DDR3 block 1, channel 1 clock enable bit 1
A13	EBI1_PCCS0N		P1	B	DDR3 block 1, channel 1 chip select bit 0
B13	EBI1_PCCS1N		P1	B	DDR3 block 1, channel 1 chip select bit 1
F20	EBI1_PCDM0		P1	B	DDR3 block 1, channel 1 data mask bit 0
A9	EBI1_PCDM1		P1	B	DDR3 block 1, channel 1 data mask bit 1
B20	EBI1_PCDM2		P1	B	DDR3 block 1, channel 1 data mask bit 2
F9	EBI1_PCDM3		P1	B	DDR3 block 1, channel 1 data mask bit 3
D23	EBI1_PCDQ0		P1	B	DDR3 block 1, channel 1 data bit 0
C22	EBI1_PCDQ1		P1	B	DDR3 block 1, channel 1 data bit 1
D22	EBI1_PCDQ2		P1	B	DDR3 block 1, channel 1 data bit 2
E22	EBI1_PCDQ3		P1	B	DDR3 block 1, channel 1 data bit 3
F21	EBI1_PCDQ4		P1	B	DDR3 block 1, channel 1 data bit 4
D20	EBI1_PCDQ5		P1	B	DDR3 block 1, channel 1 data bit 5
E21	EBI1_PCDQ6		P1	B	DDR3 block 1, channel 1 data bit 6
E20	EBI1_PCDQ7		P1	B	DDR3 block 1, channel 1 data bit 7
B9	EBI1_PCDQ8		P1	B	DDR3 block 1, channel 1 data bit 8
A8	EBI1_PCDQ9		P1	B	DDR3 block 1, channel 1 data bit 9
B8	EBI1_PCDQ10		P1	B	DDR3 block 1, channel 1 data bit 10
A7	EBI1_PCDQ11		P1	B	DDR3 block 1, channel 1 data bit 11
B7	EBI1_PCDQ12		P1	B	DDR3 block 1, channel 1 data bit 12
A6	EBI1_PCDQ13		P1	B	DDR3 block 1, channel 1 data bit 13
B6	EBI1_PCDQ14		P1	B	DDR3 block 1, channel 1 data bit 14
A5	EBI1_PCDQ15		P1	B	DDR3 block 1, channel 1 data bit 15
B24	EBI1_PCDQ16		P1	B	DDR3 block 1, channel 1 data bit 16
A23	EBI1_PCDQ17		P1	B	DDR3 block 1, channel 1 data bit 17
B23	EBI1_PCDQ18		P1	B	DDR3 block 1, channel 1 data bit 18
A22	EBI1_PCDQ19		P1	B	DDR3 block 1, channel 1 data bit 19
B22	EBI1_PCDQ20		P1	B	DDR3 block 1, channel 1 data bit 20
A21	EBI1_PCDQ21		P1	B	DDR3 block 1, channel 1 data bit 21
B21	EBI1_PCDQ22		P1	B	DDR3 block 1, channel 1 data bit 22
A20	EBI1_PCDQ23		P1	B	DDR3 block 1, channel 1 data bit 23
E9	EBI1_PCDQ24		P1	B	DDR3 block 1, channel 1 data bit 24
D9	EBI1_PCDQ25		P1	B	DDR3 block 1, channel 1 data bit 25
F8	EBI1_PCDQ26		P1	B	DDR3 block 1, channel 1 data bit 26
E8	EBI1_PCDQ27		P1	B	DDR3 block 1, channel 1 data bit 27

Table 2-2 APQ8064E pin descriptions – memory support functions (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
D7	EBI1_PCDQ28		P1	B	DDR3 block 1, channel 1 data bit 28
C7	EBI1_PCDQ29		P1	B	DDR3 block 1, channel 1 data bit 29
E7	EBI1_PCDQ30		P1	B	DDR3 block 1, channel 1 data bit 30
D6	EBI1_PCDQ31		P1	B	DDR3 block 1, channel 1 data bit 31
D18	EBI1_PCDQS0		P1	B	DDR3 block 1, channel 1 differential data strobe for byte 0 (+)
C18	EBI1_PCDQSB0		P1	B	DDR3 block 1, channel 1 differential data strobe for byte 0 (-)
A10	EBI1_PCDQS1		P1	B	DDR3 block 1, channel 1 differential data strobe for byte 1 (+)
B10	EBI1_PCDQSB1		P1	B	DDR3 block 1, channel 1 differential data strobe for byte 1 (-)
A19	EBI1_PCDQS2		P1	B	DDR3 block 1, channel 1 differential data strobe for byte 2 (+)
B19	EBI1_PCDQSB2		P1	B	DDR3 block 1, channel 1 differential data strobe for byte 2 (-)
C11	EBI1_PCDQS3		P1	B	DDR3 block 1, channel 1 differential data strobe for byte 3 (+)
D11	EBI1_PCDQSB3		P1	B	DDR3 block 1, channel 1 differential data strobe for byte 3 (-)
A14	EBI1_PCK1		P1	B	DDR3 block 1, channel 1 differential clock (+)
A12	EBI1_PCODT0		P1	B	DDR3 block 1, channel 1 ODT bit 0
A18	EBI1_PCODT1		P1	B	DDR3 block 1, channel 1 ODT bit 1
B11	EBI1_PCRASN		P1	B	DDR3 block 1, channel 1 RAS
G11	EBI1_PCRSTN		P1	B	DDR3 block 1, channel 1 reset
B12	EBI1_PCWEN		P1	B	DDR3 block 1, channel 1 write enable

Table 2-3 APQ8064E pin descriptions – multimedia functions [1]

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
Primary camera serial interface – 4-lane MIPI-CSI (CSI0)					
AH5	MIPI_CSI0_CLK_P		–	AI	MIPI camera serial interface 0 clock – positive
AG5	MIPI_CSI0_CLK_N		–	AI	MIPI camera serial interface 0 clock – negative
AH6	MIPI_CSI0_LN3_P		–	AI, AO	MIPI camera serial interface 0 lane 3 – positive
AG6	MIPI_CSI0_LN3_N		–	AI, AO	MIPI camera serial interface 0 lane 3 – negative
AF6	MIPI_CSI0_LN2_P		–	AI, AO	MIPI camera serial interface 0 lane 2 – positive
AE6	MIPI_CSI0_LN2_N		–	AI, AO	MIPI camera serial interface 0 lane 2 – negative
AF5	MIPI_CSI0_LN1_P		–	AI, AO	MIPI camera serial interface 0 lane 1 – positive
AE5	MIPI_CSI0_LN1_N		–	AI, AO	MIPI camera serial interface 0 lane 1 – negative
AD5	MIPI_CSI0_LN0_P		–	AI, AO	MIPI camera serial interface 0 lane 0 – positive
AE4	MIPI_CSI0_LN0_N		–	AI, AO	MIPI camera serial interface 0 lane 0 – negative
Secondary camera serial interface – 2-lane MIPI-CSI (CSI1)					
AH3	MIPI_CSI1_CLK_P		–	AI	MIPI camera serial interface 1 clock – positive
AG3	MIPI_CSI1_CLK_N		–	AI	MIPI camera serial interface 1 clock – negative
AF2	MIPI_CSI1_LN1_P		–	AI, AO	MIPI camera serial interface 1 lane 1 – positive
AF1	MIPI_CSI1_LN1_N		–	AI, AO	MIPI camera serial interface 1 lane 1 – negative
AH4	MIPI_CSI1_LN0_P		–	AI, AO	MIPI camera serial interface 1 lane 0 – positive
AG4	MIPI_CSI1_LN0_N		–	AI, AO	MIPI camera serial interface 1 lane 0 – negative

Table 2-3 APQ8064E pin descriptions – multimedia functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
3D camera serial interface – 1-lane MIPI-CSI (CSI2) [2]					
AF6	MIPI_CSI2_CLK_P	MIPI_CSI0_LN2_P	– –	AI AI, AO	MIPI camera serial interface 2 clock – positive MIPI camera serial interface 0 lane 2 – positive
AE6	MIPI_CSI2_CLK_N	MIPI_CSI0_LN2_N	– –	AI AI, AO	MIPI camera serial interface 2 clock – negative MIPI camera serial interface 0 lane 2 – negative
AF5	MIPI_CSI2_LN0_P	MIPI_CSI0_LN1_P	– –	AI, AO AI, AO	MIPI camera serial interface 2 lane 0 – positive MIPI camera serial interface 0 lane 1 – positive
AE5	MIPI_CSI2_LN0_N	MIPI_CSI0_LN1_N	– –	AI, AO AI, AO	MIPI camera serial interface 2 lane 0 – negative MIPI camera serial interface 0 lane 1 – negative
Camera-related timing signals					
AG23	CAM_MCLK2	GPIO_2	P3	DO B-PD:nppukp	Camera master clock 2 Configurable I/O
AG24	CAM_MCLK1	GPIO_4	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
AG25	CAM_MCLK0	GPIO_5	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
B3	CAM_MCLK0_B	GPIO_34	P3	DO B-PD:nppukp	Camera master clock 0 (B) Configurable I/O
AF25	VFE_CAM_TIMER_7C	GPIO_11	P3	DO BW-PD:nppukp	VFE camera I/F timer 7C; sync or async configurable Configurable I/O
F7	VFE_CAM_TIMER_7B	GPIO_1	P3	DO B-PD:nppukp	VFE camera I/F timer 7B; sync or async configurable Configurable I/O
V7	VFE_CAM_TIMER_7A	GPIO_47	P3	DO BW-PD:nppukp	VFE camera I/F timer 7A; sync or async configurable Configurable I/O
AD26	VFE_CAM_TIMER_6C	GPIO_10	P3	DO BW-PD:nppukp	VFE camera I/F timer 6C; sync or async configurable Configurable I/O
E6	VFE_CAM_TIMER_6B	GPIO_0	P3	DO B-PD:nppukp	VFE camera I/F timer 6B; sync or async configurable Configurable I/O
V4	VFE_CAM_TIMER_6A	GPIO_51	P3	DO B-PD:nppukp	VFE camera I/F timer 6A; sync or async configurable Configurable I/O
AF27	VFE_CAM_TIMER_5B	GPIO_19	P3	DO BW-PD:nppukp	VFE camera I/F timer 5B; sync or async configurable Configurable I/O
AB5	VFE_CAM_TIMER_5A	GPIO_46	P3	DO B-PD:nppukp	VFE camera I/F timer 5A; sync or async configurable Configurable I/O
AC24	VFE_CAM_TIMER_4C	GPIO_6	P3	DO BW-PD:nppukp	VFE camera I/F timer 4C; sync or async configurable Configurable I/O
H15	VFE_CAM_TIMER_4B	GPIO_88	P4	DO BW-PD:nppukp	VFE camera I/F timer 4B; sync or async configurable Configurable I/O
AA5	VFE_CAM_TIMER_4A	GPIO_45	P3	DO BW-PD:nppukp	VFE camera I/F timer 4A; sync or async configurable Configurable I/O
H17	VFE_CAM_TIMER_3B	GPIO_89	P4	DO B-PD:nppukp	VFE camera I/F timer 3B; sync or async configurable Configurable I/O
AG24	VFE_CAM_TIMER_3A	GPIO_4	P3	DO B-PD:nppukp	VFE camera I/F timer 3A; sync or async configurable Configurable I/O
AE22	VFE_CAM_TIMER_2	GPIO_3	P3	DO B-PD:nppukp	VFE camera I/F timer 2; sync or async configurable Configurable I/O

Table 2-3 APQ8064E pin descriptions – multimedia functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
AA20	VFE_CAM_TIMER_1B	GPIO_18	P3	DO BW-PD:nppukp	VFE camera I/F timer 1B; sync or async configurable Configurable I/O
AG23	VFE_CAM_TIMER_1A	GPIO_2	P3	DO B-PD:nppukp	VFE camera I/F timer 1A; sync or async configurable Configurable I/O
Mobile display processor (MDP) vertical sync					
AF25	MDP_VSYNC_E	GPIO_11	P3	B BW-PD:nppukp	MDP vertical sync – external Configurable I/O
E6	MDP_VSYNC_P	GPIO_0	P3	B B-PD:nppukp	MDP vertical sync – primary Configurable I/O
F7	MDP_VSYNC_S	GPIO_1	P3	B B-PD:nppukp	MDP vertical sync – secondary Configurable I/O
Primary display serial interface – 4-lane MIPI-DSI (DSI0)					
AH9	MIPI_DSI0_CLK_P		–	AO	MIPI display serial interface 0 clock – positive
AG9	MIPI_DSI0_CLK_N		–	AO	MIPI display serial interface 0 clock – negative
AD9	MIPI_DSI0_LN3_P		–	AI, AO	MIPI display serial interface 0 lane 3 – positive
AC9	MIPI_DSI0_LN3_N		–	AI, AO	MIPI display serial interface 0 lane 3 – negative
AB7	MIPI_DSI0_LN2_P		–	AI, AO	MIPI display serial interface 0 lane 2 – positive
AB9	MIPI_DSI0_LN2_N		–	AI, AO	MIPI display serial interface 0 lane 2 – negative
AH10	MIPI_DSI0_LN1_P		–	AI, AO	MIPI display serial interface 0 lane 1 – positive
AG10	MIPI_DSI0_LN1_N		–	AI, AO	MIPI display serial interface 0 lane 1 – negative
AF9	MIPI_DSI0_LN0_P		–	AI, AO	MIPI display serial interface 0 lane 0 – positive
AE9	MIPI_DSI0_LN0_N		–	AI, AO	MIPI display serial interface 0 lane 0 – negative
Y9	MIPI_DSI_CAL		–	AI, AO	MIPI display serial interface 0 & 1 calibration
Y10	MIPI_DSI_LDO		–	AI, AO	MIPI display serial interface 0 & 1 low dropout regulator
Secondary display serial interface – 4-lane MIPI-DSI (DSI1)					
AH8	MIPI_DSI1_CLK_P		–	AI	MIPI display serial interface 1 clock – positive
AG8	MIPI_DSI1_CLK_N		–	AI	MIPI display serial interface 1 clock – negative
AF7	MIPI_DSI1_LN3_P		–	AI, AO	MIPI display serial interface 1 lane 3 – positive
AE7	MIPI_DSI1_LN3_N		–	AI, AO	MIPI display serial interface 1 lane 3 – negative
AH7	MIPI_DSI1_LN2_P		–	AI, AO	MIPI display serial interface 1 lane 2 – positive
AG7	MIPI_DSI1_LN2_N		–	AI, AO	MIPI display serial interface 1 lane 2 – negative
AD7	MIPI_DSI1_LN1_P		–	AI, AO	MIPI display serial interface 1 lane 1 – positive
AC7	MIPI_DSI1_LN1_N		–	AI, AO	MIPI display serial interface 1 lane 1 – negative
AD8	MIPI_DSI1_LN0_P		–	AI, AO	MIPI display serial interface 1 lane 0 – positive
AC8	MIPI_DSI1_LN0_N		–	AI, AO	MIPI display serial interface 1 lane 0 – negative
Y9	MIPI_DSI_CAL		–	AI, AO	MIPI display serial interface 0 & 1 calibration
Y10	MIPI_DSI_LDO		–	AI, AO	MIPI display serial interface 0 & 1 low dropout regulator
High-definition multimedia interface (HDMI)					
AH14	HDMI_TCLK_P		–	AO	HDMI differential clock – plus
AG14	HDMI_TCLK_M		–	AO	HDMI differential clock – minus
AB15	HDMI_TX2_P		–	AO	HDMI differential transmit 2 – plus

Table 2-3 APQ8064E pin descriptions – multimedia functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
AC15	HDMI_TX2_M		–	AO	HDMI differential transmit 2 – minus
AH15	HDMI_TX1_P		–	AO	HDMI differential transmit 1 – plus
AG15	HDMI_TX1_M		–	AO	HDMI differential transmit 1 – minus
AB14	HDMI_TX0_P		–	AO	HDMI differential transmit 0 – plus
AA14	HDMI_TX0_M		–	AO	HDMI differential transmit 0 – minus
AA13	HDMI_REXT		–	AI, AO	HDMI external calibration resistor
A3	HDMI_CEC	GPIO_69	P3	B B-PU:nppdkp	HDMI consumer electronics control Configurable I/O
C4	HDMI_DDC_CLK	GPIO_70	P3	B B-PU:nppdkp	HDMI display data channel – clock Configurable I/O
A4	HDMI_DDC_DATA	GPIO_71	P3	B B-PU:nppdkp	HDMI display data channel – data Configurable I/O
H12	HDMI_HPLUG_DET	GPIO_72	P3	DI BW-PD:nppukp	HDMI hot plug detect Configurable I/O
Alternate primary display interface - low-voltage differential signaling (LVDS) interface					
AH12	LVDS_CLK1_P		P3	DO	LVDS clock 1 – plus
AG12	LVDS_CLK1_M		P3	DO	LVDS clock 1 – minus
AG11	LVDS_CLK0_P		P3	DO	LVDS clock 0 – plus
AH11	LVDS_CLK0_M		P3	DO	LVDS clock 0 – minus
AG13	LVDS_TX7_P		P3	DO	LVDS differential transmit 7 – plus
AH13	LVDS_TX7_M		P3	DO	LVDS differential transmit 7 – minus
AE13	LVDS_TX6_P		P3	DO	LVDS differential transmit 6 – plus
AF13	LVDS_TX6_M		P3	DO	LVDS differential transmit 6 – minus
AC13	LVDS_TX5_P		P3	DO	LVDS differential transmit 5 – plus
AD13	LVDS_TX5_M		P3	DO	LVDS differential transmit 5 – minus
AB13	LVDS_TX4_P		P3	DO	LVDS differential transmit 4 – plus
AC14	LVDS_TX4_M		P3	DO	LVDS differential transmit 4 – minus
AF11	LVDS_TX3_P		P3	DO	LVDS differential transmit 3 – plus
AE11	LVDS_TX3_M		P3	DO	LVDS differential transmit 3 – minus
AD12	LVDS_TX2_P		P3	DO	LVDS differential transmit 2 – plus
AC11	LVDS_TX2_M		P3	DO	LVDS differential transmit 2 – minus
AA12	LVDS_TX1_P		P3	DO	LVDS differential transmit 1 – plus
Y12	LVDS_TX1_M		P3	DO	LVDS differential transmit 1 – minus
AA11	LVDS_TX0_P		P3	DO	LVDS differential transmit 0 – plus
Y11	LVDS_TX0_M		P3	DO	LVDS differential transmit 0 – minus
Also see Table 2-4 for connectivity ports that are used for multimedia applications: *Audio – I^2S, MI^2S, SLIMbus, PCM; controls – I^2C*					

1. See Table 2-1 for parameter and acronym definitions.
2. MIPI_CSI2 is muxed behind MIPI_CSI0 for 3D camera usage.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in Table 2-3), designers must identify all their application's requirements and map each GPIO to its function, carefully avoiding conflicts in GPIO assignments. See Table 2-8 for a list of all supported functions for each GPIO.

Table 2-4 APQ8064E pin descriptions – connectivity functions [1]

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
Audio I²S interface – primary speaker					
AD3	CDC_SPKR_I2S_ DOUT	GPIO_41	P3	DO BW-PD:nppukp	Primary speaker codec I²S data output Configurable I/O
AD2	CDC_SPKR_I2S_SCK	GPIO_40	P3	B B-PD:nppukp	Primary speaker codec I²S bit clock Configurable I/O
V6	CDC_SPKR_I2S_WS	GPIO_42	P3	B BW-PD:nppukp	Primary speaker codec I²S word select (L/R) Configurable I/O
AA6	CDC_SPKR_I2S_ MCLK	GPIO_39	P3	DO BW-PD:nppukp	Primary speaker codec I²S master clock Configurable I/O
Audio I²S interface – secondary speaker					
W2	SPKR_I2S_DOUT	GPIO_49	P3	DO BW-PD:nppukp	Secondary speaker codec I²S data output Configurable I/O
V7	SPKR_I2S_SCK	GPIO_47	P3	B BW-PD:nppukp	Secondary speaker codec I²S bit clock Configurable I/O
V1	SPKR_I2S_WS	GPIO_48	P3	B B-PD:nppukp	Secondary speaker codec I²S word select (L/R) Configurable I/O
V3	SPKR_I2S_MCLK	GPIO_50	P3	DO BW-PD:nppukp	Secondary speaker codec I²S master clock Configurable I/O
Audio MI²S interface – 8-channel (7.1 speaker, 5.1 microphone)					
Y3	MI2S_SD3	GPIO_29	P3	B BW-PD:nppukp	Multiple I²S interface serial data channel 3 Configurable I/O
AC1	MI2S_SD2	GPIO_30	P3	B BW-PD:nppukp	Multiple I²S interface serial data channel 2 Configurable I/O
AD1	MI2S_SD1	GPIO_31	P3	B B-PD:nppukp	Multiple I²S interface serial data channel 1 Configurable I/O
Y1	MI2S_SD0	GPIO_32	P3	B BW-PD:nppukp	Multiple I²S interface serial data channel 0 Configurable I/O
Y6	MI2S_SCK	GPIO_28	P3	B B-PD:nppukp	Multiple I²S interface bit clock Configurable I/O
AA2	MI2S_WS	GPIO_27	P3	B B-PD:nppukp	Multiple I²S interface word select (L/R) Configurable I/O
AA1	MI2S_MCLK	GPIO_33	P3	DO B-PD:nppukp	Multiple I²S interface master clock Configurable I/O
Audio I²S interface – primary microphone (quad mic support)					
B4	CDC_MIC_I2S_DIN1	GPIO_38	P3	DI BW-PD:nppukp	Primary microphone codec I²S data input 1 Configurable I/O
E5	CDC_MIC_I2S_DIN0	GPIO_37	P3	DI B-PD:nppukp	Primary microphone codec I²S data input 0 Configurable I/O

Table 2-4 APQ8064E pin descriptions – connectivity functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
H10	CDC_MIC_I2S_SCK	GPIO_35	P3	B B-PD:nppukp	Primary microphone codec I2S bit clock Configurable I/O
B5	CDC_MIC_I2S_WS	GPIO_36	P3	B BW-PD:nppukp	Primary microphone codec I2S word select (L/R) Configurable I/O
B3	CDC_MIC_I2S_MCLK	GPIO_34	P3	DO BW-PD:nppukp	Primary microphone codec I2S master clock Configurable I/O
Audio I2S interface – secondary microphone					
V4	MIC_I2S_DIN	GPIO_51	P3	DI B-PD:nppukp	Secondary microphone codec I2S data input Configurable I/O
V5	MIC_I2S_SCK	GPIO_52	P3	B BW-PD:nppukp	Secondary microphone codec I2S bit clock Configurable I/O
U1	MIC_I2S_WS	GPIO_53	P3	B B-PD:nppukp	Secondary microphone codec I2S word select (L/R) Configurable I/O
U2	MIC_I2S_MCLK	GPIO_54	P3	DO B-PD:nppukp	Secondary microphone codec I2S master clock Configurable I/O
Audio PCM interface					
AB1	AUDIO_PCM_DIN	GPIO_44	P3	DI BW-PD:nppukp	Audio PCM data input Configurable I/O
W1	AUDIO_PCM_DOUT	GPIO_43	P3	DO-Z B-PD:nppukp	Audio PCM data output Configurable I/O
AB5	AUDIO_PCM_CLK	GPIO_46	P3	B B-PD:nppukp	Audio PCM clock Configurable I/O
AA5	AUDIO_PCM_SYNC	GPIO_45	P3	B BW-PD:nppukp	Audio PCM sync Configurable I/O
Audio SLIMbus – bidirectional multiplexed audio					
AD3	AUD_SB1_DATA_A	GPIO_41	P3	B BW-PD:nppukp	Audio bidirectional data (A) via SLIMbus 1 Configurable I/O
AC1	AUD_SB1_DATA_B	GPIO_30	P3	B BW-PD:nppukp	Audio bidirectional data (B) via SLIMbus 1 Configurable I/O
AD2	AUD_SB1_CLK_A	GPIO_40	P3	B B-PD:nppukp	Audio clock (A) for SLIMbus 1 Configurable I/O
AD1	AUD_SB1_CLK_B	GPIO_31	P3	B B-PD:nppukp	Audio clock (B) for SLIMbus 1 Configurable I/O
AA6	AUD_SB1_MCLK	GPIO_39	P3	DO BW-PD:nppukp	Audio master clock for SLIMbus 1 Configurable I/O
Inter-integrated circuit (I2C) interface					
F7	GSBI1_I2C_SCL	GPIO_1	P3	B B-PD:nppukp	General SBI 1 – I2C serial clock Configurable I/O
B4	GSBI4_I2C_SCL	GPIO_38	P3	B BW-PD:nppukp	General SBI 4 – I2C serial clock Configurable I/O
E6	GSBI1_I2C_SDA	GPIO_0	P3	B B-PD:nppukp	General SBI 1 – I2C serial data Configurable I/O
E5	GSBI4_I2C_SDA	GPIO_37	P3	B B-PD:nppukp	General SBI 4 – I2C serial data Configurable I/O

Table 2-4 APQ8064E pin descriptions – connectivity functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
Secure digital controller 1 (SDC1) interface – supports eMMC NAND					
A26	SDC1_DATA_7		P3	B	Secure digital controller 1 data bit 7
A25	SDC1_DATA_6		P3	B	Secure digital controller 1 data bit 6
C25	SDC1_DATA_5		P3	B	Secure digital controller 1 data bit 5
E24	SDC1_DATA_4		P3	B	Secure digital controller 1 data bit 4
B26	SDC1_DATA_3		P3	B	Secure digital controller 1 data bit 3
A24	SDC1_DATA_2		P3	B	Secure digital controller 1 data bit 2
B25	SDC1_DATA_1		P3	B	Secure digital controller 1 data bit 1
E23	SDC1_DATA_0		P3	B	Secure digital controller 1 data bit 0
D24	SDC1_CMD		P3	B	Secure digital controller 1 command
C24	SDC1_CLK		P3	DO	Secure digital controller 1 clock
Secure digital controller 2 (SDC2) interface					
G6	SDC2_DATA_3	GPIO_58	P3	B BW-PD:nppukp	Secure digital controller 2 data bit 3 Configurable I/O
H8	SDC2_DATA_2	GPIO_60	P3	B B-PD:nppukp	Secure digital controller 2 data bit 2 Configurable I/O
C6	SDC2_DATA_1	GPIO_61	P3	B BW-PD:nppukp	Secure digital controller 2 data bit 1 Configurable I/O
D1	SDC2_DATA_0	GPIO_62	P3	B B-PD:nppukp	Secure digital controller 2 data bit 0 Configurable I/O
E1	SDC2_CMD	GPIO_57	P3	B B-PD:nppukp	Secure digital controller 2 command Configurable I/O
H5	SDC2_CLK	GPIO_59	P3	DO B-PD:nppukp	Secure digital controller 2 clock Configurable I/O
Secure digital controller 3 (SDC3) interface					
F1	SDC3_DATA_3		P2	B	Secure digital controller 3 data bit 3 (dual voltage)
G1	SDC3_DATA_2		P2	B	Secure digital controller 3 data bit 2 (dual voltage)
F2	SDC3_DATA_1		P2	B	Secure digital controller 3 data bit 1 (dual voltage)
G2	SDC3_DATA_0		P2	B	Secure digital controller 3 data bit 0 (dual voltage)
H2	SDC3_CMD		P2	B	Secure digital controller 3 command (dual voltage)
G3	SDC3_CLK		P2	DO	Secure digital controller 3 clock (dual voltage)
Secure digital controller 4 (SDC4) interface					
AC2	SDC4_DATA_3	GPIO_63	P3	B BW-PD:nppukp	Secure digital controller 4 data bit 3 Configurable I/O
AB4	SDC4_DATA_2	GPIO_64	P3	B B-PD:nppukp	Secure digital controller 4 data bit 2 Configurable I/O
AB2	SDC4_DATA_1	GPIO_65	P3	B BW-PD:nppukp	Secure digital controller 4 data bit 1 Configurable I/O
AB3	SDC4_DATA_0	GPIO_66	P3	B B-PD:nppukp	Secure digital controller 4 data bit 0 Configurable I/O
AC3	SDC4_CMD	GPIO_67	P3	B B-PD:nppukp	Secure digital controller 4 command Configurable I/O
Y2	SDC4_CLK	GPIO_68	P3	DO B-PD:nppukp	Secure digital controller 4 clock Configurable I/O

Table 2-4 APQ8064E pin descriptions – connectivity functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
Serial peripheral interface (SPI) extra chip selects (supplements GSBI ports configured for SPI protocol)					
AC1	GSBI5_SPI_CS1A_N GSBI6_SPI_CS1A_N GSBI7_SPI_CS1A_N	GPIO_30	P3	DO-Z DO-Z DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 1A for SPI on GSBI 5, 6 and 7 Configurable I/O
ADI	GSBI5_SPI_CS2A_N GSBI6_SPI_CS2A_N GSBI7_SPI_CS2A_N	GPIO_31	P3	DO-Z DO-Z DO-Z B-PD:nppukp	Serial peripheral interface chip-select 2A for SPI on GSBI 5, 6, and 7 Configurable I/O
YI	GSBI5_SPI_CS3A_N GSBI6_SPI_CS3A_N GSBI7_SPI_CS3A_N	GPIO_32	P3	DO-Z DO-Z DO-Z B-PD:nppukp	Serial peripheral interface chip-select 3A for SPI on GSBI 5, 6, and 7 Configurable I/O
V7	GSBI5_SPI_CS1B_N GSBI6_SPI_CS1B_N GSBI7_SPI_CS1B_N	GPIO_47	P3	DO-Z DO-Z DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 1B for SPI on GSBI 5, 6, and 7 Configurable I/O
W2	GSBI5_SPI_CS3B_N GSBI6_SPI_CS3B_N GSBI7_SPI_CS3B_N	GPIO_49	P3	DO-Z DO-Z DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 3B for SPI on GSBI 5, 6, and 7 Configurable I/O
AB4	GSBI6_SPI_CS1C_N	GPIO_64	P3	DO-Z B-PD:nppukp	Serial peripheral interface chip-select 1 for SPI on GSBI6 Configurable I/O
AE26	GSBI1_SPI_CS1A_N GSBI1_SPI_CS3B_N	GPIO_7	P3	DO-Z DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 1A for SPI on GSBI1 Configurable I/O
AD26	GSBI1_SPI_CS1B_N	GPIO_10	P3	DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 1B for SPI on GSBI1 Configurable I/O
B5	GSBI1_SPI_CS1C_N	GPIO_36	P3	DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 1C for SPI on GSBI1 Configurable I/O
AC2	GSBI6_SPI_CS2C_N	GPIO_63	P3	DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 2 for SPI on GSBI6 Configurable I/O
AC24	GSBI1_SPI_CS2A_N	GPIO_6	P3	DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 2A for SPI on GSBI1 Configurable I/O
AF25	GSBI1_SPI_CS2B_N	GPIO_11	P3	DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 2B for SPI on GSBI1 Configurable I/O
V1	GSBI1_SPI_CS2C_N GSBI5_SPI_CS2B_N GSBI6_SPI_CS2B_N GSBI7_SPI_CS2B_N	GPIO_48	P3	DO-Z DO-Z DO-Z DO-Z B-PD:nppukp	Serial peripheral interface chip-select: 2B for SPI on GSBI 1, 5, 6 and 7; chip-select 2C for GSBI 1. Configurable I/O
H6	GSBI1_SPI_CS3A_N	GPIO_56	P3	DO-Z BW-PD:nppukp	Serial peripheral interface chip-select 3A for SPI on GSBI1 Configurable I/O

Table 2-4 APQ8064E pin descriptions – connectivity functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
Touch screen interface					
AF24	TS_PENIRQ_N	GPIO_26	P3	DI BW-PU:nppdkp	Touch screen pen-down interrupt Configurable I/O
AE26	TS_EOC	GPIO_7	P3	DI BW-PD:nppdkp	Touch screen end-of-conversion interrupt Configurable I/O
AC24	SSBI_TS	GPIO_6	P3	B BW-PD:nppdkp	Single-wire serial bus interface for touch screen Configurable I/O
Transport stream interface 1 (TSIF1)					
E1	TSIF1_DATA	GPIO_57	P3	DI B-PD:nppukp	Transport stream interface 1 data Configurable I/O
G5	TSIF1_CLK	GPIO_55	P3	DI BW-PD:nppukp	Transport stream interface 1 clock Configurable I/O
D1	TSIF1_SYNC	GPIO_62	P3	DI B-PD:nppukp	Transport stream interface 1 sync Configurable I/O
H6	TSIF1_EN	GPIO_56	P3	DI BW-PD:nppukp	Transport stream interface 1 enable Configurable I/O
Transport stream interface 2 (TSIF2)					
C6	TSIF2_DATA	GPIO_61	P3	DI BW-PD:nppukp	Transport stream interface 2 data Configurable I/O
H5	TSIF2_CLK	GPIO_59	P3	DI B-PD:nppukp	Transport stream interface 2 clock Configurable I/O
G6	TSIF2_SYNC	GPIO_58	P3	DI BW-PD:nppukp	Transport stream interface 2 sync Configurable I/O
H8	TSIF2_EN	GPIO_60	P3	DI B-PD:nppukp	Transport stream interface 2 enable Configurable I/O
Universal asynchronous receiver transmitter (UART) interface					
E3	GSBI1_UART_RX	GPIO_81	P3	DI BW-PD:nppukp	General SBI 1 – UART receive data Configurable I/O
C26	GSBI2_UART_RX	GPIO_75	P3	DI BW-PU:nppukp	General SBI 2 – UART receive data Configurable I/O
AB3	GSBI3_UART_RX	GPIO_66	P3	DI B-PD:nppukp	General SBI 3 – UART receive data Configurable I/O
B5	GSBI4_UART_RX	GPIO_36	P3	DI BW-PD:nppukp	General SBI 4 – UART receive data Configurable I/O
AB2	GSBI3_UART_TX	GPIO_65	P3	DO BW-PD:nppukp	General SBI 3 – UART transmit data Configurable I/O
H10	GSBI4_UART_TX	GPIO_35	P3	DO B-PD:nppukp	General SBI 4 – UART transmit data Configurable I/O
AC3	GSBI3_UART_CTS	GPIO_67	P3	DI B-PD:nppukp	General SBI 3 – UART clear-to-send Configurable I/O
Y2	GSBI3_UART_RFR_N	GPIO_68	P3	DO B-PD:nppukp	General SBI 3 – UART ready-for-receive Configurable I/O

Table 2-4 APQ8064E pin descriptions – connectivity functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
USB UICC interface					
U1	UICC_DP	GPIO_53	P3	B B-PD:nppukp	UICC data plus Configurable I/O
U2	UICC_DM	GPIO_54	P3	B B-PD:nppukp	UICC data minus Configurable I/O
USB HS PHY interface 1 (USB1)					
R1	USB1_HS_DP		–	AI, AO	USB1 HS data plus
R2	USB1_HS_DM		–	AI, AO	USB1 HS data minus
T5	USB1_HS_VBUS		–	AI	USB1 HS bus voltage (5 V)
T4	USB1_HS_ID		–	AI, AO	USB1 HS ID (differentiates between mini A or B plugs)
N3	USB1_3_4_HS_ SYSCLK		–	DI	USB1, USB3, and USB4 HS system clock (19.2 MHz)
T3	USB1_HS_REXT		–	AI, AO	USB1 HS external resistor – Kelvin connection
USB HS PHY interface 3 (USB3)					
K1	USB3_HS_DP		–	AI, AO	USB3 HS data plus
K2	USB3_HS_DM		–	AI, AO	USB3 HS data minus
L5	USB3_HS_VBUS		–	AI	USB3 HS bus voltage (5 V)
L4	USB3_HS_ID		–	AI, AO	USB3 HS ID (differentiates between mini A or B plugs)
N3	USB1_3_4_HS_ SYSCLK		–	DI	USB1, USB3, and USB4 HS system clock (19.2 MHz)
L7	USB3_HS_REXT		–	AI, AO	USB3 HS external resistor – Kelvin connection
USB HS PHY interface 4 (USB4)					
M1	USB4_HS_DP		–	AI, AO	USB4 HS data plus
M2	USB4_HS_DM		–	AI, AO	USB4 HS data minus
N5	USB4_HS_VBUS		–	AI	USB4 HS bus voltage (5 V)
N4	USB4_HS_ID		–	AI, AO	USB4 HS ID (differentiates between mini A or B plugs)
N3	USB1_3_4_HS_ SYSCLK		–	DI	USB1, USB3, and USB4 HS system clock (19.2 MHz)
N1	USB4_HS_REXT		–	AI, AO	USB4 HS external resistor – Kelvin connection
HSIC interface (USB2)					
H15	USB2_HSIC_STROBE	GPIO_88	P4	AI, AO B-PD:nppukp	HSIC strobe configurable I/O
H17	USB2_HSIC_DATA	GPIO_89	P4	AI, AO B-PD: nppukp	HSIC data configurable I/O
H18	USB2_HSIC_CAL		P4	AI, AO	HSIC calibration

Table 2-4 APQ8064E pin descriptions – connectivity functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
PCI Express interface (PCIe)					
AH20	PCI_E_REFCLK_P		–	B	PCIe reference clock – plus
AG20	PCI_E_REFCLK_N		–	B	PCIe reference clock – minus
AH21	PCI_E_HSO_P		–	B	PCIe transmit lane – plus
AG21	PCI_E_HSO_N		–	B	PCIe transmit lane – minus
AH19	PCI_E_HSI_P		–	B	PCIe receive lane – plus
AG19	PCI_E_HSI_N		–	B	PCIe receive lane – minus
AC18	PCI_E_REXT		–	B	PCIe external resistor
AD22	PCI_E_PWRFLT_N	GPIO_86	P3	DI B-PD:nppukp	PCIe power-fault indication Configurable I/O
AF26	PCI_E_PWREN_N	GPIO_85	P3	DI B-PD:nppukp	PCIe interface signal to power up/down the transceiver Configurable I/O
Y20	PCI_E_PRSNT_2_N	GPIO_84	P3	DO BW-PD:nppukp	PCIe interface power presence detection Configurable I/O
AA21	PCI_E_WAKE_N	GPIO_83	P3	DO BW-PD:nppukp	PCIe interface link reactivation Configurable I/O
Y21	PCI_E_RST_N	GPIO_82	P3	DI B-PD:nppukp	PCIe interface core reset Configurable I/O
Serial ATA interface (SATA)					
AF16	SATA_CLKP		–	DO	SATA clock - plus
AE16	SATA_CLKM		–	DO	SATA clock - minus
AH16	SATA_TXP		–	AO	SATA transmit - plus
AG16	SATA_TXM		–	AO	SATA transmit - minus
AG17	SATA_RXP		–	AI	SATA receive - plus
AH17	SATA_RXM		–	AI	SATA receive - minus
AD16	SATA_REXT		–	AI, AO	SATA external resistor
AD17	SATA_TPA		–	AO	SATA test access point
General serial bus interface 1 – see Table 2-9 for application-specific pin assignments					
AA20	GSBI1_3	GPIO_18	P3	B BW-PD:nppukp	General SBI 1 bit 3; UART, UIM, SPI, or I^2C Configurable I/O
AF27	GSBI1_2	GPIO_19	P3	B BW-PD:nppukp	General SBI 1 bit 2; UART, UIM, SPI, or I^2C Configurable I/O
AG26	GSBI1_1	GPIO_20	P3	B B-PD:nppukp	General SBI 1 bit 1; UART, UIM, SPI, or I^2C Configurable I/O
AF23	GSBI1_0	GPIO_21	P3	B B-PD:nppukp	General SBI 1 bit 0; UART, UIM, SPI, or I^2C Configurable I/O
General serial bus interface 2 – see Table 2-9 for application-specific pin assignments					
AE21	GSBI2_3	GPIO_22	P3	B BW-PD:nppukp	General SBI 2 bit 3; UART, UIM, SPI, or I^2C Configurable I/O
AD24	GSBI2_2	GPIO_23	P3	B BW-PD:nppukp	General SBI 2 bit 2; UART, UIM, SPI, or I^2C Configurable I/O
AC23	GSBI2_1	GPIO_24	P3	B B-PD:nppukp	General SBI 2 bit 1; UART, UIM, SPI, or I^2C Configurable I/O

Table 2-4 APQ8064E pin descriptions – connectivity functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
AC22	GSBI2_0	GPIO_25	P3	B B-PD:nppukp	General SBI 2 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 3 – see Table 2-9 for application-specific pin assignments					
AC24	GSBI3_3	GPIO_6	P3	B BW-PD:nppukp	General SBI 3 bit 3; UART, UIM, SPI, or I2C Configurable I/O
AE26	GSBI3_2	GPIO_7	P3	B BW-PD:nppukp	General SBI 3 bit 2; UART, UIM, SPI, or I2C Configurable I/O
AD21	GSBI3_1	GPIO_8	P3	B B-PD:nppukp	General SBI 3 bit 1; UART, UIM, SPI, or I2C Configurable I/O
AD23	GSBI3_0	GPIO_9	P3	B B-PD:nppukp	General SBI 3 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 4 – see Table 2-9 for application-specific pin assignments					
AD26	GSBI4_3	GPIO_10	P3	B BW-PD:nppukp	General SBI 4 bit 3; UART, UIM, SPI, or I2C Configurable I/O
AF25	GSBI4_2	GPIO_11	P3	B BW-PD:nppukp	General SBI 4 bit 2; UART, UIM, SPI, or I2C Configurable I/O
AD25	GSBI4_1	GPIO_12	P3	B B-PD:nppukp	General SBI 4 bit 1; UART, UIM, SPI, or I2C Configurable I/O
AF22	GSBI4_0	GPIO_13	P3	B B-PD:nppukp	General SBI 4 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 5 – see Table 2-9 for application-specific pin assignments					
V4	GSBI5_3	GPIO_51	P3	B B-PD:nppukp	General SBI 5 bit 3; UART, UIM, SPI, or I2C Configurable I/O
V5	GSBI5_2	GPIO_52	P3	B BW-PD:nppukp	General SBI 5 bit 2; UART, UIM, SPI, or I2C Configurable I/O
U1	GSBI5_1	GPIO_53	P3	B B-PD:nppukp	General SBI 5 bit 1; UART, UIM, SPI, or I2C Configurable I/O
U2	GSBI5_0	GPIO_54	P3	B B-PD:nppukp	General SBI 5 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 6 – see Table 2-9 for application-specific pin assignments					
H9	GSBI6_3	GPIO_14	P3	B B-PD:nppukp	General SBI 6 bit 3; UART, UIM, SPI, or I2C Configurable I/O
F6	GSBI6_2	GPIO_15	P3	B BW-PD:nppukp	General SBI 6 bit 2; UART, UIM, SPI, or I2C Configurable I/O
C3	GSBI6_1	GPIO_16	P3	B B-PD:nppukp	General SBI 6 bit 1; UART, UIM, SPI, or I2C Configurable I/O
D3	GSBI6_0	GPIO_17	P3	B B-PD:nppukp	General SBI 6 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 7 – see Table 2-9 for application-specific pin assignments					
Y21	GSBI7_3	GPIO_82	P3	B B-PD:nppukp	General SBI 7 bit 3; UART, UIM, SPI, or I2C Configurable I/O
AA21	GSBI7_2	GPIO_83	P3	B BW-PD:nppukp	General SBI 7 bit 2; UART, UIM, SPI, or I2C Configurable I/O

Table 2-4 APQ8064E pin descriptions – connectivity functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
Y20	GSBI7_1	GPIO_84	P3	B BW-PD:nppukp	General SBI 7 bit 1; UART, UIM, SPI, or I2C Configurable I/O
AF26	GSBI7_0	GPIO_85	P3	B B-PD:nppukp	General SBI 7 bit 0; UART, UIM, SPI, or I2C Configurable I/O

1. See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in Table 2-4), designers must identify all their application's requirements and map each GPIO to its function, carefully avoiding conflicts in GPIO assignments. See Table 2-8 for a list of all supported functions for each GPIO.

Table 2-5 APQ8064E pin descriptions – internal functions [1]

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
Clocks and related signals, resets, and mode controls					
E27	SLEEP_CLK		P3	DI	Sleep clock
E4	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz)
C2	CXO_EN		P3	DO	Dual function: core crystal oscillator enable
W15	PXO_IN		–	AI	Platform crystal oscillator input (24.576 MHz or 27 MHz)
W14	PXO_OUT		–	AO	Platform crystal oscillator output (24.576 MHz or 27 MHz)
Y1	GP_CLK_2A	GPIO_32	P3	DO BW-PD:nppukp	General-purpose clock output 2A Configurable I/O
AC22	GP_CLK_2B	GPIO_25	P3	DO B-PD:nppukp	General-purpose clock output 2B Configurable I/O
AG24	GP_CLK_1A	GPIO_4	P3	DO B-PD:nppukp	General-purpose clock output 1A Configurable I/O
V3	GP_CLK_1B	GPIO_50	P3	DO BW-PD:nppukp	General-purpose clock output 1B Configurable I/O
AE22	GP_CLK_0A	GPIO_3	P3	DO B-PD:nppukp	General-purpose clock output 0A Configurable I/O
B3	GP_CLK_0B	GPIO_34	P3	DO BW-PD:nppukp	General-purpose clock output 0B Configurable I/O
AG23	GP_MN	GPIO_2	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
W2	GP_PDM_2A	GPIO_49	P3	DO BW-PD:nppukp	General-purpose PDM output 2A, 12-bit, clocked at XO/4 Configurable I/O
AA1	GP_PDM_2B	GPIO_33	P3	DO B-PD:nppukp	General-purpose PDM output 2B, 12-bit, clocked at XO/4 Configurable I/O
AE21	GP_PDM_1A	GPIO_22	P3	DO BW-PD:nppukp	General-purpose PDM output 1A, 12-bit, clocked at XO/4 Configurable I/O
AB1	GP_PDM_1B	GPIO_44	P3	DO BW-PD:nppukp	General-purpose PDM output 1B, 12-bit, clocked at XO/4 Configurable I/O
B4	GP_PDM_0A	GPIO_38	P3	DO BW-PD:nppukp	General-purpose PDM output 0A, 12-bit, clocked at XO/4 Configurable I/O

Table 2-5 APQ8064E pin descriptions – internal functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
AA20	GP_PDM_0B	GPIO_18	P3	DO BW-PD:nppukp	General-purpose PDM output 0B, 12-bit, clocked at XO/4 Configurable I/O
Resets and mode controls – also see the list of APQ8064 pins (Table 2-6) that can wake up the device (thereby supporting MPM)					
T21	MODE_1		P3	DI	Mode control bit 1
R21	MODE_0		P3	DI	Mode control bit 0
U21	RESIN_N		P3	DI	Reset input
P21	RESOUT_N		P3	DO	Reset output
AE22	WDOG_DISABLE	GPIO_3	P3	DI B-PD:nppukp	Watchdog timer disable input Configurable I/O
AG24	BOOT_CONFIG_6	GPIO_4	P3	DI B-PD:nppukp	Boot configuration bit 6 (depends on security fuse state) Configurable I/O
AG25	BOOT_CONFIG_5	GPIO_5	P3	DI B-PD:nppukp	Boot configuration bit 5 (depends on security fuse state) Configurable I/O
AA1	BOOT_CONFIG_4	GPIO_33	P3	DI B-PD:nppukp	Boot configuration bit 4 (depends on security fuse state) Configurable I/O
B3	BOOT_CONFIG_3	GPIO_34	P3	DI BW-PD:nppukp	Boot configuration bit 3 (depends on security fuse state) Configurable I/O
AA6	BOOT_CONFIG_2	GPIO_39	P3	DI BW-PD:nppukp	Boot configuration bit 2 (depends on security fuse state) Configurable I/O
V3	BOOT_CONFIG_1	GPIO_50	P3	DI BW-PD:nppukp	Boot configuration bit 1 (depends on security fuse state) Configurable I/O
W21	BOOT_CONFIG_0	GPIO_87	P3	DI B-PD:nppukp	Boot configuration bit 0 (depends on security fuse state) Configurable I/O
AG23	BOOT_FROM_ROM	GPIO_2	P3	DI B-PD:nppukp	Boot configuration bit to select boot from ROM option Configurable I/O
JTAG interfaces					
K21	RTCK		P3	DO	JTAG return clock
D26	SRST_N		P3	DI	JTAG reset for debug
L21	TCK/SWD_CLK		P3	DI	JTAG clock input; SWD clock input
F24	TDI		P3	DI	JTAG data input
D28	TDO		P3	DO-Z	JTAG data output
D25	TMS/SWD_DATA		P3	DI	JTAG mode select input; SWD test data input
D27	TRST_N		P3	DI	JTAG reset

1. See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in Table 2-5), designers must identify all their application's requirements and map each GPIO to its function, carefully avoiding conflicts in GPIO assignments. See Table 2-8 for a list of all supported functions for each GPIO.

Table 2-6 APQ8064E wakeup pins[1]

Pin #	Pin name	Pin voltage	Pin type	Functional description
AC24	GPIO_6	P3	BW-PD:nppukp	Configurable I/O
AE26	GPIO_7	P3	BW-PD:nppukp	Configurable I/O
AD26	GPIO_10	P3	BW-PD:nppukp	Configurable I/O
AF25	GPIO_11	P3	BW-PD:nppukp	Configurable I/O
F6	GPIO_15	P3	BW-PD:nppukp	Configurable I/O
AA20	GPIO_18	P3	BW-PD:nppukp	Configurable I/O
AF27	GPIO_19	P3	BW-PD:nppukp	Configurable I/O
AE21	GPIO_22	P3	BW-PD:nppukp	Configurable I/O
AD24	GPIO_23	P3	BW-PD:nppukp	Configurable I/O
AF24	GPIO_26	P3	BW-PU:nppukp	Configurable I/O
Y3	GPIO_29	P3	BW-PD:nppukp	Configurable I/O
AC1	GPIO_30	P3	BW-PD:nppukp	Configurable I/O
Y1	GPIO_32	P3	BW-PD:nppukp	Configurable I/O
B3	GPIO_34	P3	BW-PD:nppukp	Configurable I/O
B5	GPIO_36	P3	BW-PD:nppukp	Configurable I/O
B4	GPIO_38	P3	BW-PD:nppukp	Configurable I/O
AA6	GPIO_39	P3	BW-PD:nppukp	Configurable I/O
AD3	GPIO_41	P3	BW-PD:nppdkp	Configurable I/O
V6	GPIO_42	P3	BW-PD:nppukp	Configurable I/O
AB1	GPIO_44	P3	BW-PD:nppukp	Configurable I/O
AA5	GPIO_45	P3	BW-PD:nppukp	Configurable I/O
V7	GPIO_47	P3	BW-PD:nppukp	Configurable I/O
W2	GPIO_49	P3	BW-PD:nppukp	Configurable I/O
V3	GPIO_50	P3	BW-PD:nppukp	Configurable I/O
V5	GPIO_52	P3	BW-PD:nppukp	Configurable I/O
G5	GPIO_55	P3	BW-PD:nppukp	Configurable I/O
H6	GPIO_56	P3	BW-PD:nppukp	Configurable I/O
G6	GPIO_58	P3	BW-PD:nppukp	Configurable I/O
C6	GPIO_61	P3	BW-PD:nppukp	Configurable I/O
AC2	GPIO_63	P3	BW-PD:nppukp	Configurable I/O
AB2	GPIO_65	P3	BW-PD:nppukp	Configurable I/O
H12	GPIO_72	P3	BW-PD:nppukp	Configurable I/O
C27	GPIO_73	P3	BW-PU:nppdkp	Configurable I/O
G23	GPIO_74	P3	BW-PU:nppdkp	Configurable I/O
C26	GPIO_75	P3	BW-PU:nppdkp	Configurable I/O
F22	GPIO_76	P3	BW-PU:nppdkp	Configurable I/O
J21	GPIO_77	P3	BW-PU:nppdkp	Configurable I/O
E3	GPIO_81	P3	BW-PD:nppukp	Configurable I/O
AA21	GPIO_83	P3	BW-PD:nppukp	Configurable I/O
Y20	GPIO_84	P3	BW-PD:nppukp	Configurable I/O

Table 2-6 APQ8064E wakeup pins[1] (cont.)

Pin #	Pin name	Pin voltage	Pin type	Functional description
H15	GPIO_88	P4	BW-PD:nppukp	Configurable I/O
B26	SDC1_DATA_3	P3	B	Secure digital controller 1 data bit 3
B25	SDC1_DATA_1	P3	B	Secure digital controller 1 data bit 1
F1	SDC3_DATA_3	P2	B	Secure digital controller 3 data bit 3 (dual-voltage)
F2	SDC3_DATA_1	P2	B	Secure digital controller 3 data bit 1 (dual-voltage)
D26	SRST_N	P3	DI	JTAG reset for debug

1. See Table 2-1 for parameter and acronym definitions.

Table 2-7 APQ8064E pin descriptions – chipset interface functions [1]

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
GPS RF receiver IC – GNSS Rx baseband interface					
N9	GNSS_BB_IP		–	AI	GNSS receiver baseband input, in-phase plus
N8	GNSS_BB_IM		–	AI	GNSS receiver baseband input, in-phase minus
M9	GNSS_BB_QP		–	AI	GNSS receiver baseband input, quadrature plus
M8	GNSS_BB_QM		–	AI	GNSS receiver baseband input, quadrature minus
AE23	GNSS_BLANKING	GPIO_80	P3	DO B-PD:nppukp	GNSS Rx blanking control Configurable I/O
E3	SSBI_EXT_GPS	GPIO_81	P3	B BW-PD:nppukp	Single-wire serial bus interface for external GPS Configurable I/O
AC24	GPS_PPS_OUT	GPIO_6	P3	DO BW-PD:nppukp	GPS one pulse per second output Configurable I/O
AC24	GPS_PPS_IN	GPIO_6	P3	DI BW-PD:nppukp	GPS one pulse per second input Configurable I/O
PMIC interfaces					
E27	SLEEP_CLK		P3	DI	Sleep clock
E4	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz)
C2	CXO_EN		P3	DO	Core crystal oscillator enable
U21	RESIN_N		P3	DI	Reset input
C28	PS_HOLD	GPIO_78	P3	DO B-PD:nppukp	Power supply hold signal to PMIC Configurable I/O
E25	SSBI_PMIC1		P3	B	Single-wire serial bus interface for PMIC1
F23	SSBI_PMIC2	GPIO_79	P3	B B-PD:nppukp	Single-wire serial bus interface for PMIC2 Configurable I/O
H14	SSBI_PMIC_FCLK		P3	DO	Alternate PMIC SSBI clock when CXO is disabled
C26	PMIC1_MDM_INT_N	GPIO_75	P3	DI BW-PU:nppdkp	Modem interrupt request from PMIC1 Configurable I/O
C27	PMIC1_SEC_INT_N	GPIO_73	P3	DI BW-PU:nppdkp	Secure apps μP interrupt request from PMIC1 Configurable I/O
G23	PMIC1_USR_INT_N	GPIO_74	P3	DI BW-PU:nppdkp	User (nonsecure) apps μP interrupt request from PMIC1 Configurable I/O
F22	PMIC2_SEC_INT_N	GPIO_76	P3	DI BW-PU:nppdkp	Secure apps μP interrupt request from PMIC2 Configurable I/O

Table 2-7 APQ8064E pin descriptions – chipset interface functions [1] (cont.)

Pin #	Pin name and/or function	Pin name or alt function	Pin voltage	Pin type	Functional description
J21	PMIC2_USR_INT_N	GPIO_77	P3	DI BW-PU:nppdkp	User (nonsecure) apps μP interrupt request from PMIC2 Configurable I/O
–	*Also see Table 2-4 for UIM connectivity ports that can use the PMIC for level translation.*				
–	*Also see Table 2-4 for UART connectivity ports that can use the PMIC as a 3:1 UART multiplexer.*				
Wireless connectivity IC – WLAN signals					
T9	WLAN_BB_IP		–	AI, AO	WLAN baseband ADC/DAC switched, in-phase plus
R9	WLAN_BB_IM		–	AI, AO	WLAN baseband ADC/DAC switched, in-phase minus
T8	WLAN_BB_QP		–	AI, AO	WLAN baseband ADC/DAC switched, quadrature plus
R8	WLAN_BB_QM		–	AI, AO	WLAN baseband ADC/DAC switched, quadrature minus
U8	WLAN_VREF		–	AI	Reference voltage for WLAN DAC
T7	WLAN_REXT		–	AI	WLAN external resistor
Y2	WLAN_CLK	GPIO_68	P3	DO B-PD:nppukp	WLAN synchronization clock Configurable I/O
AC3	WLAN_CMD	GPIO_67	P3	DO B-PD:nppukp	WLAN command Configurable I/O
AB4	WLAN_DATA_2	GPIO_64	P3	DI B-PD:nppukp	WLAN data bit 2 Configurable I/O
AB2	WLAN_DATA_1	GPIO_65	P3	DI BW-PD:nppukp	WLAN data bit 1 Configurable I/O
AB3	WLAN_DATA_0	GPIO_66	P3	DI B-PD:nppukp	WLAN data bit 0 Configurable I/O
Wireless connectivity IC – BT signals					
AC2	SSBI_BT	GPIO_63	P3	B BW-PD:nppukp	Single-wire serial bus interface for Bluetooth Configurable I/O
D3	BT_DATA_STROBE	GPIO_17	P3	B B-PD:nppukp	Bluetooth dual-function signal – serial data and strobe Configurable I/O
C3	BT_CTL	GPIO_16	P3	DO B-PD:nppukp	Bluetooth control signal for the modem interface Configurable I/O
Wireless connectivity IC – FM radio signals					
H9	SSBI_FM	GPIO_14	P3	B B-PD:nppukp	Single-wire serial bus interface for FM radio Configurable I/O
F6	FM_SDI	GPIO_15	P3	B BW-PD:nppukp	FM radio serial data interface Configurable I/O
Audio codec IC interfaces					
AC4	WCN_XO		P3	DI	Shared XO for the wireless connectivity subsystem
–	*See Table 2-4 for SLIMbus bidirectional mutliplexed audio (AUD_SB1).*				
–	*Also see Table 2-4 for I^2C connectivity ports that can used as the status and control interface.*				
Mobile broadcast platform interfaces					
–	*See Table 2-4 for SD connectivity ports that can used as the host controller interface.*				
–	*Also see Table 2-4 for SPI connectivity ports (via GSBI) that can used as the host controller interface.*				
–	*Also see Table 2-4 for TSIF connectivity ports that can used for MPEG packet transfers in ISDB-T applications.*				

1. See Table 2-1 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in Table 2-7, designers must identify all their application's requirements and map each GPIO to its function, carefully avoiding conflicts in GPIO assignments. See Table 2-8 for a list of all supported functions for each GPIO.

NOTE System designers must examine each GPIO's external connection and programmed configuration, and take any steps necessary to avoid excessive leakage current. The combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pullup or pulldown
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

Table 2-8 APQ8064E pin descriptions – general-purpose input/output ports [1]

Pin #	Pin name	Configurable function	Pin voltage	Pin type	Functional description
H17	GPIO_89	USB2_HSIC_DATA VFE_CAMIF_TIMER_3B	P4	B-PD:nppukp B DO	Configurable I/O HSIC data VFE camera I/F timer 3B; sync or async configurable
H15	GPIO_88	USB2_HSIC_STROBE VFE_CAMIF_TIMER_4B	P4	BW-PD:nppukp B DO	Configurable I/O HSIC strobe VFE camera I/F timer 4B; sync or async configurable
W21	GPIO_87	SATA_LED BOOT_CONFIG_0	P3	B-PD:nppukp DI DI	Configurable I/O SATA status LED Boot configuration bit 0 (depends upon security fuse state)
AD22	GPIO_86	PCI_E_PWRFLT_N	P3	B-PD:nppukp DI	Configurable I/O PCIe power-fault indication
AF26	GPIO_85	GSBI7_0 PCI_E_PWREN_N	P3	B-PD:nppukp B DI	Configurable I/O General SBI 7 bit 0; UART, UIM, SPI, or I^2C PCIe interface signal to power up/down the transceiver
Y20	GPIO_84	GSBI7_1 PCI_E_PRSNT_2_N	P3	BW-PD:nppukp B DO	Configurable I/O General SBI 7 bit 1; UART, UIM, SPI, or I^2C PCIe interface power presence detection
AA21	GPIO_83	GSBI7_2 PCI_E_WAKE_N	P3	BW-PD:nppukp B DO	Configurable I/O General SBI 7 bit 2; UART, UIM, SPI, or I^2C PCIe interface link reactivation
Y21	GPIO_82	GSBI7_3 PCI_E_RST_N	P3	B-PD:nppukp B DI	Configurable I/O General SBI 7 bit 3; UART, UIM, SPI, or I^2C PCIe interface core reset
E3	GPIO_81	GSBI1_UART_RX [2] SSBI_EXT_GPS	P3	BW-PD:nppukp DI B	Configurable I/O General SBI 1 – UART receive data Single-wire serial bus interface for external GPS
AE23	GPIO_80	GNSS_BLANKING	P3	B-PD:nppukp DO	Configurable I/O GNSS Rx blanking control

Table 2-8 APQ8064E pin descriptions – general-purpose input/output ports [1] (cont.)

Pin #	Pin name	Configurable function	Pin voltage	Pin type	Functional description
F23	GPIO_79	SSBI_PMIC2	P3	B-PD:nppukp B	Configurable I/O Single-wire serial bus interface for PMIC 2
C28	GPIO_78	PS_HOLD	P3	B-PD:nppukp DO	Configurable I/O Power-supply hold signal to PMIC
J21	GPIO_77	PMIC2_USR_INT_N	P3	BW-PU:nppukp DI	Configurable I/O User (nonsecure) apps µP interrupt request from PMIC2
F22	GPIO_76	PMIC2_SEC_INT_N	P3	BW-PU:nppukp DI	Configurable I/O Secure apps µP interrupt request from PMIC2
C26	GPIO_75	GSBI2_UART_RX [2] PMIC1_MDM_INT_N	P3	BW-PU:nppukp DI DI	Configurable I/O General SBI 2 – UART receive data Modem interrupt request from PMIC1
G23	GPIO_74	PMIC1_USR_INT_N	P3	BW-PU:nppukp DI	Configurable I/O User (nonsecure) apps µP interrupt request from PMIC1
C27	GPIO_73	PMIC1_SEC_INT_N	P3	BW-PU:nppukp DI	Configurable I/O Secure apps µP interrupt request from PMIC1
H12	GPIO_72	HDMI_HPLUG_DET	P3	BW-PD:nppukp DI	Configurable I/O HDMI hot plug detect
A4	GPIO_71	HDMI_DDC_DATA	P3	B-PU:nppukp B	Configurable I/O HDMI display data channel – data
C4	GPIO_70	HDMI_DDC_CLK	P3	B-PU:nppukp B	Configurable I/O HDMI display data channel – clock
A3	GPIO_69	HDMI_CEC	P3	B-PU:nppukp B	Configurable I/O HDMI consumer electronics control
Y2	GPIO_68	GSBI3_UART_RFR_N [2] SDC4_CLK WLAN_CLK	P3	B-PD:nppukp DO DO DO	Configurable I/O General SBI 3 – UART ready-for-receive Secure digital controller 4 clock WLAN synchronization clock
AC3	GPIO_67	GSBI3_UART_CTS [2] SDC4_CMD WLAN_CMD	P3	B-PD:nppukp DI B DO	Configurable I/O General SBI 3 – UART clear-to-send Secure digital controller 4 command WLAN command
AB3	GPIO_66	GSBI3_UART_RX [2] SDC4_DATA_0 WLAN_DATA_0	P3	B-PD:nppukp DI B DI	Configurable I/O General SBI 3 – UART receive data Secure digital controller 4 data bit 0 WLAN data bit 0
AB2	GPIO_65	GSBI3_UART_TX [2] SDC4_DATA_1 WLAN_DATA_1	P3	BW-PD:nppukp DO B DI	Configurable I/O General SBI 3 – UART transmit data Secure digital controller 4 data bit 1 WLAN data bit 1
AB4	GPIO_64	SDC4_DATA_2 GSBI6_SPI_CS1C_N[2] WLAN_DATA_2	P3	B-PD:nppukp B DO-Z DI	Configurable I/O Secure digital controller 4 data bit 2 Serial peripheral interface chip-select 1 for SPI on GSBI6 WLAN data bit 2
AC2	GPIO_63	SDC4_DATA_3 GSBI6_SPI_CS2C_N[2] SSBI_BT	P3	BW-PD:nppukp B DO-Z B	Configurable I/O Secure digital controller 4 data bit 3 Serial peripheral interface chip-select 2 for SPI on GSBI6 Single-wire serial bus interface for Bluetooth
D1	GPIO_62	TSIF1_SYNC SDC2_DATA_0	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 1 sync Secure digital controller 2 data bit 0

Table 2-8 APQ8064E pin descriptions – general-purpose input/output ports [1] (cont.)

Pin #	Pin name	Configurable function	Pin voltage	Pin type	Functional description
C6	GPIO_61	TSIF2_DATA SDC2_DATA_1	P3	BW-PD:nppukp DI B	Configurable I/O Transport stream interface 2 data Secure digital controller 2 data bit 1
H8	GPIO_60	TSIF2_EN SDC2_DATA_2	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 enable Secure digital controller 2 data bit 2
H5	GPIO_59	TSIF2_CLK SDC2_CLK	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 clock Secure digital controller 2 clock
G6	GPIO_58	TSIF2_SYNC SDC2_DATA_3	P3	BW-PD:nppukp DI B	Configurable I/O Transport stream interface 2 sync Secure digital controller 2 data bit 3
E1	GPIO_57	TSIF1_DATA SDC2_CMD	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 1 data Secure digital controller 2 command
H6	GPIO_56	TSIF1_EN SPI_CS3A_N_GSBI1	P3	BW-PD:nppukp DI DO-Z	Configurable I/O Transport stream interface 1 enable Serial peripheral interface chip-select 3A for SPI on GSBI1
G5	GPIO_55	TSIF1_CLK	P3	BW-PD:nppukp DI	Configurable I/O Transport stream interface 1 clock
U2	GPIO_54	MIC_I2S_MCLK GSBI5_0 UICC_DM USB_FS1_SE0_A	P3	B-PD:nppukp DO B B B	Configurable I/O Secondary microphone codec I^2S master clock General SBI 5 bit 0; UART, UIM, SPI, or I^2C UICC data minus Full-speed USB SE0 for diagnostics
U1	GPIO_53	MIC_I2S_WS GSBI5_1 UICC_DP USB_FS1_DAT_A	P3	B-PD:nppukp B B B B	Configurable I/O Secondary microphone codec I^2S word select (L/R) General SBI 5 bit 1; UART, UIM, SPI, or I^2C UICC data plus Full-speed USB data for diagnostics
V5	GPIO_52	MIC_I2S_SCK GSBI5_2 USB_FS1_OE_A_N	P3	BW-PD:nppukp B B DO	Configurable I/O Secondary microphone codec I^2S bit clock General SBI 5 bit 2; UART, UIM, SPI, or I^2C Full-speed USB output enable for diagnostics
V4	GPIO_51	MIC_I2S_DIN GSBI5_3 VFE_CAMIF_TIMER_6A	P3	B-PD:nppukp DI B DO	Configurable I/O Secondary microphone codec I^2S data input General SBI 5 bit 3; UART, UIM, SPI, or I^2C VFE camera I/F timer 6A; sync or async configurable
V3	GPIO_50	SPKR_I2S_MCLK GP_CLK_1B BOOT_CONFIG_1	P3	BW-PD:nppukp DO DO DI	Configurable I/O Secondary speaker codec I^2S master clock General-purpose clock output 1B Boot configuration bit 1(depends upon security fuse state)
W2	GPIO_49	SPKR_I2S_DOUT GP_PDM_2A GSBI5_SPI_CS3B_N GSBI6_SPI_CS3B_N GSBI7_SPI_CS3B_N	P3	BW-PD:nppukp DO DO DO-Z DO-Z DO-Z	Configurable I/O Secondary speaker codec I^2S data output General-purpose PDM output 2A, 12-bit, clocked at XO/4 Serial peripheral interface chip-select 3B for SPI on GSBI 5, 6, and 7
V1	GPIO_48	SPKR_I2S_WS SPI_CS2C_N_GSBI1	P3	B-PD:nppukp B DO-Z	Configurable I/O Secondary speaker codec I^2S word select (L/R) Serial peripheral interface chip-select 2C for SPI on GSBI1

Table 2-8 APQ8064E pin descriptions – general-purpose input/output ports [1] (cont.)

Pin #	Pin name	Configurable function	Pin voltage	Pin type	Functional description
V7	GPIO_47	SPKR_I2S_SCK VFE_CAMIF_TIMER_7A GSBI5_SPI_CS1B_N GSBI6_SPI_CS1B_N GSBI7_SPI_CS1B_N	P3	BW-PD:nppukp B DO DO-Z DO-Z DO-Z	Configurable I/O Secondary speaker codec I2S bit clock VFE camera I/F timer 7A; sync or async configurable Serial peripheral interface chip-select 1B for SPI on GSBI 5, 6, and 7
AB5	GPIO_46	AUDIO_PCM_CLK VFE_CAMIF_TIMER_5A	P3	B-PD:nppdkp B DO	Configurable I/O Audio PCM clock VFE camera I/F timer 5A; sync or async configurable
AA5	GPIO_45	AUDIO_PCM_SYNC VFE_CAM_TIMER_4A	P3	BW-PD:nppukp B DO	Configurable I/O Audio PCM sync VFE camera I/F timer 4A; sync or async configurable
AB1	GPIO_44	AUDIO_PCM_DIN GP_PDM_1B	P3	BW-PD:nppukp DI DO	Configurable I/O Audio PCM data input General-purpose PDM output 1B, 12-bit, clocked at XO/4
W1	GPIO_43	AUDIO_PCM_DOUT	P3	B-PD:nppukp DO-Z	Configurable I/O Audio PCM data output
V6	GPIO_42	CDC_SPKR_I2S_WS	P3	BW-PD:nppukp B	Configurable I/O Primary speaker codec I2S word select (L/R)
AD3	GPIO_41	CDC_SPKR_I2S_DOUT AUD_SB1_DATA_A	P3	BW-PD:nppukp DO B	Configurable I/O Primary speaker codec I2S data output Audio bidirectional data (A) via SLIMbus 1
AD2	GPIO_40	CDC_SPKR_I2S_SCK AUD_SB1_CLK_A	P3	B-PD:nppukp B B	Configurable I/O Primary speaker codec I2S bit clock Audio clock (A) via SLIMbus 1
AA6	GPIO_39	CDC_SPKR_I2S_MCLK AUD_SB1_MCLK BOOT_CONFIG_2	P3	BW-PD:nppukp DO DO DI	Configurable I/O Primary speaker codec I2S master clock Audio master clock for SLIMbus 1 Boot configuration bit 2 (depends on security fuse state)
B4	GPIO_38	CDC_MIC_I2S_DIN1 GP_PDM_0A GSBI4_I2C_SCL [2] USB_FS1_SE0_B	P3	BW-PD:nppukp DI DO B B	Configurable I/O Primary microphone codec I2S data input 1 General-purpose PDM output 0A, 12-bit, clocked at XO/4 General SBI 4 – I2C serial clock Full-speed USB SE0 for diagnostics
E5	GPIO_37	CDC_MIC_I2S_DIN0 GSBI4_I2C_SDA [2] USB_FS1_DAT_B	P3	B-PD:nppukp DI B B	Configurable I/O Primary microphone codec I2S data input 0 General SBI 4 – I2C serial data Full-speed USB data for diagnostics
B5	GPIO_36	CDC_MIC_I2S_WS GSBI4_UART_RX [2] GSBI1_SPI_CS1C_N USB_FS1_OE_B_N	P3	BW-PD:nppukp B DI DO-Z DO	Configurable I/O Primary microphone codec I2S word select (L/R) General SBI 4 – UART receive data Serial peripheral interface chip-select 1C for SPI on GSBI1 Full-speed USB output enable for diagnostics
H10	GPIO_35	CDC_MIC_I2S_SCK GSBI4_UART_TX [2]	P3	B-PD:nppukp B DO	Configurable I/O Primary microphone codec I2S bit clock General SBI 4 – UART transmit data
B3	GPIO_34	CAM_MCLK0_B [2] CDC_MIC_I2S_MCLK GP_CLK_0B BOOT_CONFIG_3	P3	BW-PD:nppukp DO DO DO DI	Configurable I/O Camera master clock 0 (B) Primary microphone codec I2S master clock General-purpose clock output 0B Boot configuration bit 3 (depends on security fuse state)

Table 2-8 APQ8064E pin descriptions – general-purpose input/output ports [1] (cont.)

Pin #	Pin name	Configurable function	Pin voltage	Pin type	Functional description
AA1	GPIO_33	MI2S_MCLK GP_PDM_2B BOOT_CONFIG_4	P3	B-PD:nppukp B DO DI	Configurable I/O Multiple I2S interface master clock General-purpose PDM output 2B, 12-bit, clocked at XO/4 Boot configuration bit 4 (depends on security fuse state)
Y1	GPIO_32	MI2S_SD0 GP_CLK_2A GSBI5_SPI_CS3A_N GSBI6_SPI_CS3A_N GSBI7_SPI_CS3A_N	P3	BW-PD:nppukp B DO DO-Z DO-Z DO-Z	Configurable I/O Multiple I2S interface serial data channel 0 General-purpose clock output 2A Serial peripheral interface chip-select 3A for SPI on GSBI 5, 6, and 7
AD1	GPIO_31	MI2S_SD1 AUD_SB1_CLK_B GSBI5_SPI_CS2A_N GSBI6_SPI_CS2A_N GSBI7_SPI_CS2A_N	P3	B-PD:nppukp B B DO-Z DO-Z DO-Z	Configurable I/O Multiple I2S interface serial data channel 1 Audio clock (B) via SLIMbus 1 Serial peripheral interface chip-select 2A for SPI on GSBI 5, 6, and 7
AC1	GPIO_30	MI2S_SD2 AUD_SB1_DATA_B GSBI5_SPI_CS1A_N GSBI6_SPI_CS1A_N GSBI7_SPI_CS1A_N	P3	BW-PD:nppukp B B DO-Z DO-Z DO-Z	Configurable I/O Multiple I2S interface serial data channel 2 Audio bidirectional data (B) via SLIMbus 1 Serial peripheral interface chip-select 1A for SPI on GSBI 5, 6, and 7
Y3	GPIO_29	MI2S_SD3	P3	BW-PD:nppukp B	Configurable I/O Multiple I2S interface serial data channel 3
Y6	GPIO_28	MI2S_SCK	P3	B-PD:nppukp B	Configurable I/O Multiple I2S interface bit clock
AA2	GPIO_27	MI2S_WS	P3	B-PD:nppukp B	Configurable I/O Multiple I2S interface word select (L/R)
AF24	GPIO_26	TS_PENIRQ_N	P3	BW-PU:nppukp DI	Configurable I/O Touch screen pen interrupt
AC22	GPIO_25	GSBI2_0 GP_CLK_2B	P3	B-PD:nppukp B DO	Configurable I/O General SBI 2 bit 0; UART, UIM, SPI, or I2C General-purpose clock output 2B
AC23	GPIO_24	GSBI2_1	P3	B-PD:nppukp B	Configurable I/O General SBI 2 bit 1; UART, UIM, SPI, or I2C
AD24	GPIO_23	GSBI2_2	P3	BW-PD:nppukp B	Configurable I/O General SBI 2 bit 2; UART, UIM, SPI, or I2C
AE21	GPIO_22	GSBI2_3 GP_PDM_1A	P3	BW-PD:nppukp B DO	Configurable I/O General SBI 2 bit 3; UART, UIM, SPI, or I2C General-purpose PDM output 1A, 12-bit, clocked at XO/4
AF23	GPIO_21	GSBI1_0	P3	B-PD:nppukp B	Configurable I/O General SBI 1 bit 0; UART, UIM, SPI, or I2C
AG26	GPIO_20	GSBI1_1	P3	B-PD:nppukp B	Configurable I/O General SBI 1 bit 1; UART, UIM, SPI, or I2C
AF27	GPIO_19	GSBI1_2 VFE_CAM_TIMER_5B	P3	BW-PD:nppukp B DO	Configurable I/O General SBI 1 bit 2; UART, UIM, SPI, or I2C VFE camera I/F timer 5B; sync or async configurable
AA20	GPIO_18	GSBI1_3 GP_PDM_0B VFE_CAM_TIMER_1B	P3	BW-PD:nppukp B DO DO	Configurable I/O General SBI 1 bit 3; UART, UIM, SPI, or I2C General-purpose PDM output 0B, 12-bit, clocked at XO/4 VFE camera I/F timer 1B; sync or async configurable

Table 2-8 APQ8064E pin descriptions – general-purpose input/output ports [1] (cont.)

Pin #	Pin name	Configurable function	Pin voltage	Pin type	Functional description
D3	GPIO_17		P3	B-PD:nppukp	Configurable I/O
		GSBI6_0		B	General SBI 6 bit 0; UART, UIM, SPI, or I2C
		BT_DATA_STROBE		B	Bluetooth dual-function signal – serial data and strobe
C3	GPIO_16		P3	B-PD:nppukp	Configurable I/O
		GSBI6_1		B	General SBI 6 bit 1; UART, UIM, SPI, or I2C
		BT_CTL		DO	Bluetooth control signal for the modem interface
F6	GPIO_15		P3	BW-PD:nppukp	Configurable I/O
		GSBI6_2		B	General SBI 6 bit 2; UART, UIM, SPI, or I2C
		FM_SDI		B	FM radio serial data interface
H9	GPIO_14		P3	B-PD:nppukp	Configurable I/O
		GSBI6_3		B	General SBI 6 bit 3; UART, UIM, SPI, or I2C
		SSBI_FM		B	Single-wire serial bus interface for FM radio
AF22	GPIO_13		P3	B-PD:nppukp	Configurable I/O
		GSBI4_0		B	General SBI 4 bit 0; UART, UIM, SPI, or I2C
AD25	GPIO_12		P3	B-PD:nppukp	Configurable I/O
		GSBI4_1		B	General SBI 4 bit 1; UART, UIM, SPI, or I2C
AF25	GPIO_11		P3	BW-PD:nppukp	Configurable I/O
		GSBI4_2		B	General SBI 4 bit 2; UART, UIM, SPI, or I2C
		MDP_VSYNC_E		B	MDP vertical sync – external
		VFE_CAM_TIMER_7C		DO	VFE camera I/F timer 7C; sync or async configurable
		GSBI1_SPI_CS2B_N		DO-Z	Serial peripheral interface chip-select 2B for SPI on GSBI1
AD26	GPIO_10		P3	BW-PD:nppukp	Configurable I/O
		GSBI4_3		B	General SBI 4 bit 3; UART, UIM, SPI, or I2C
		VFE_CAM_TIMER_6C		DO	VFE camera I/F timer 6C; sync or async configurable
		GSBI1_SPI_CS1B_N		DO-Z	Serial peripheral interface chip-select 1B for SPI on GSBI1
AD23	GPIO_9		P3	B-PD:nppukp	Configurable I/O
		GSBI3_0		B	General SBI 3 bit 0; UART, UIM, SPI, or I2C
AD21	GPIO_8		P3	B-PD:nppukp	Configurable I/O
		GSBI3_1		B	General SBI 3 bit 1; UART, UIM, SPI, or I2C
AE26	GPIO_7		P3	BW-PD:nppukp	Configurable I/O
		GSBI3_2		B	General SBI 3 bit 2; UART, UIM, SPI, or I2C
		TS_EOC		DI	Touch screen end-of-conversion
		GSBI1_SPI_CS1A_N		DO-Z	Serial peripheral interface chip-select 1A for SPI on GSBI1
		GSBI1_SPI_CS3B_N		DO-Z	Serial peripheral interface chip-select 3B for SPI on GSBI1
AC24	GPIO_6		P3	BW-PD:nppukp	Configurable I/O
		GSBI3_3		B	General SBI 3 bit 3; UART, UIM, SPI, or I2C
		GPS_PPS_OUT		DO	GPS one pulse per second output
		GPS_PPS_IN		DI	GPS one pulse per second input
		VFE_CAM_TIMER_4C		DO	VFE camera I/F timer 4C; sync or async configurable
		GSBI1_SPI_CS2A_N		DO-Z	Serial peripheral interface chip-select 2A for SPI on GSBI1
		SSBI_TS		B	Single-wire serial bus interface for touch screen
AG25	GPIO_5		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK0		DO	Camera master clock 0
		BOOT_CONFIG_5		DI	Boot configuration bit 5 (depends on security fuse state)
AG24	GPIO_4		P3	B-PD:nppukp	Configurable I/O
		VFE_CAM_TIMER_3A		DO	VFE camera I/F timer 3A; sync or async configurable
		CAM_MCLK1		DO	Camera master clock 1
		GP_CLK_1A		DO	General-purpose clock output 1A
		BOOT_CONFIG_6		DI	Boot configuration bit 6 (depends on security fuse state)

Table 2-8 APQ8064E pin descriptions – general-purpose input/output ports [1] (cont.)

Pin #	Pin name	Configurable function	Pin voltage	Pin type	Functional description
AE22	GPIO_3		P3	B-PD:nppukp	Configurable I/O
		VFE_CAM_TIMER_2		DO	VFE camera I/F timer 2; sync or async configurable
		GP_CLK_0A		DO	General-purpose clock output 0A
		WDOG_DISABLE		DI	Watchdog timer disable input
AG23	GPIO_2		P3	B-PD:nppukp	Configurable I/O
		VFE_CAM_TIMER_1A		DO	VFE camera I/F timer 1A; sync or async configurable
		GP_MN		DO	General-purpose M/N:D counter output
		CAM_MCLK2		DO	Camera master clock 2
		BOOT_FROM_ROM		DI	Boot configuration bit to select boot from ROM option
F7	GPIO_1		P3	B-PD:nppukp	Configurable I/O
		GSBI1_I2C_SCL [2]		B	General SBI 1 – I^2C serial clock
		MDP_VSYNC_S		B	MDP vertical sync – secondary
		VFE_CAM_TIMER_7B		DO	VFE camera I/F timer 7B; sync or async configurable
E6	GPIO_0		P3	B-PD:nppukp	Configurable I/O
		GSBI1_I2C_SDA [2]		B	General SBI 1 – I^2C serial data
		MDP_VSYNC_P		B	MDP vertical sync – primary
		VFE_CAM_TIMER_6B		DO	VFE camera I/F timer 6B; sync or async configurable

1. See Table 2-1 for parameter and acronym definitions.
2. This function is only applicable to v2 devices.

NOTE Seven 4-pin sets of GPIOs are available as general serial bus interface (GSBI) ports that can be configured for UART, UIM, SPI, or I^2C operation. Detailed pin assignments are presented in Table 2-9 for each configuration.

Table 2-9 GSBI configurations [1] [2]

Option	Configuration	GSBI bit 3	GSBI bit 2	GSBI bit 1	GSBI bit 0
	GSBI1 GPIO pins = GSBI2 GPIO pins = GSBI3 GPIO pins = GSBI4 GPIO pins = [3] GSBI5 GPIO pins = GSBI6 GPIO pins = GSBI7 GPIO pins = [3]	GPIO_18 GPIO_22 GPIO_6 (GPIO_65 - UART_TX) [4] GPIO_10 (GPIO_35 - UART_TX) [4] GPIO_51 GPIO_14 GPIO_82	GPIO_19 (GPIO_81 - UART_RX) [4] GPIO_23 (GPIO_75 - UART_RX) [4] GPIO_7 (GPIO_66 - UART_RX) [4] GPIO_11 (GPIO_36 - UART_RX) [4] GPIO_52 GPIO_15 GPIO_83	GPIO_20 (GPIO_0 - I2C_SDA) [4] GPIO_24 GPIO_8 (GPIO_67 - UART_CTS) [4] GPIO_12 (GPIO_37 - I2C_SDA) [4] GPIO_53 GPIO_16 GPIO_84	GPIO_21 (GPIO_1 - I2C_SCL) [4] GPIO_25 GPIO_9 (GPIO_68 - UART_RFR) [4] GPIO_13 (GPIO_38 - I2C_SCL) [4] GPIO_54 GPIO_17 GPIO_85
1	4-pin UART	UART_TX DO 4-pin UART transmit data	UART_RX DI 4-pin UART receive data	UART_CTS DI 4-pin UART clear-to-send	UART_RFR DO 4-pin UART ready-for-receive
2	4-pin SPI	SPI_DATA_MOSI B 4-pin SPI master out/slave in	SPI_DATA_MISO B 4-pin SPI master in/slave out	SPI_CS_N B 4-pin SPI chip select	SPI_CLK B 4-pin SPI clock
3	3-pin UIM + 1 GPIO	UIM_DATA B UIM data	UIM_CLK DO UIM clock	UIM_RESET_N DO UIM reset	GPIO_XX B Configurable I/O
4	2-pin I^2C + 2-pin UART	UART_TX DO 2-pin UART transmit data	UART_RX DI 2-pin UART receive data	I2C_SDA B I^2C serial data	I2C_SCL B I^2C serial clock
5	UIM + I^2C	UIM_DATA B UIM data	UIM_CLK DO UIM clock	I2C_SDA B I^2C serial data	I2C_SCL B I^2C serial clock
6	4 GPIOs	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O

1. The three rows within cell entries are: 1) pin function, 2) pin type, and 3) functional description.
2. Client rate control interfaces (CRCI) allow a data mover (DM) client with limited memory space to throttle data flow. A given CRCI only allows either the primary or the secondary device to access one DM at a time. SPI and UARTDM are GSBI interfaces that require DM access to achieve the higher throughput rates. I^2C, UART, UIM, etc. do not need a DM.
   The design constraints on the GSBI assignment are 1) Two GSBI interfaces sharing the same CRCI cannot both access the DM at the same time. For example, GSBI4 and GSBI7 cannot be both configured as SPI or UARTDM, and still have access to the DM. 2) GSBI1, GSBI2, and GSBI3 cannot be assigned as SPI or UARTDM, since the crypto engine (CE) requires access to the DM to achieve the throughput requirement.
3. I^2C can be time-shared on bits 3/2 and bits 1/0 for GSBI4 and GSBI7. The intended use case is a 3D camera, where both I^2C addresses are expected to be the same.
4. This function is only applicable to v2 devices.

Table 2-10 Channel rate control interface assignments

CRCI #	Primary (a)	Secondary (b)
1	CE_3_INB	TSIF2
2	CE_3_OTB	CE_1_INB
3	RESERVED (GND)	CE_1_OTB
4	RESERVED (GND)	CE_2_INB
5	GSBI_3_IN	CE_2_OTB
6	GSBI_3_OUT	GSBI_6_OUT
7	GSBI_4_IN	GSBI_7_IN
8	GSBI_4_OUT	GSBI_7_OUT
9	GSBI_5_IN	RESERVED (GND)
10	GSBI_5_OUT	RESERVED (GND)
11	GSBI_6_IN	TSIF1/TSIF2
12	GSBI_1_IN	RESERVED (GND)
13	GSBI_1_OUT	RESERVED (GND)
14	GSBI_2_IN	CE_3_INB
15	GSBI_2_OUT	CE_3_OTB

Table 2-11 APQ8064E pin descriptions – no connection and do not connect pins

Pin #	Pin name	Functional description
A1, A2, A27, A28, B1, B2, B27, B28, C1, C8, C10, C12, C14, C15, C17, C19, C21, D2, D4, D8, D10, D12, D14, D15, D17, D19, D21, E2, E10, E14, E15, E19, F10, F12, F17, F19, G10, G12, G17, G19, H3, H4, H25, H26, K3, K4, K5, K6, K7, K23, K24, K25, K26, M3, M4, M6, M7, M25, M26, P3, P4, P5, P24, P25, P26, R3, R4, R5, R24, R25, R26, U3, U4, U6, U7, U25, U26, W3, W4, W5, W6, W7, W23, W24, W25, W26, AA3, AA4, AA7, AA25, AA26, AB8, AB10, AB12, AB17, AB19, AB21, AC10, AC12, AC17, AC19, AC21, AD10, AD14, AD15, AD19, AE8, AE10, AE12, AE14, AE15, AE17, AE19, AF8, AF10, AF12, AF14, AF15, AF17, AF19, AF21, AG1, AG2, AG27, AG28, AH1, AH2, AH27, AH28	DNC	Do not connect; connected internally, do not connect externally

Table 2-12 APQ8064E pin descriptions – power supply pins

Pin #	Pin name	Functional description
AB18	VDD_A2	Power for analog circuits – high voltage
F3, H21, J4, J16, J17, K10, K11, L11, M5, M12, M13, M17, N13, N20, P10, P11, P17, R6, R11, T12, T13, U13, V17, W17	VDD_CORE	Power for digital core circuits
R15, R16, T15, T16	VDD_KR0	Power for Krait application microprocessor 0
U23	VDD_KR0_SNS	Sense node for Krait application microprocessor 0 supply voltage
R18, R19, T18, T19	VDD_KR1	Power for Krait application microprocessor 1
U22	VDD_KR1_SNS	Sense node for Krait application microprocessor 1 supply voltage
L15, L16, M15, M16	VDD_KR2	Power for Krait application microprocessor 2

Table 2-12 APQ8064E pin descriptions – power supply pins (cont.)

Pin #	Pin name	Functional description
M23	VDD_KR2_SNS	Sense node for Krait application microprocessor 2 supply voltage
L18, L19, M18, M19	VDD_KR3	Power for Krait application microprocessor 3
M22	VDD_KR3_SNS	Sense node for Krait application microprocessor 3 supply voltage
J9, J12, J15, J18, J19, L10, M21, N12, N16, N18, R10, U12, U18, V16, V19, W9, W11	VDD_MEM	Power for on-chip memory
G8, G21, H7, H11, H19, H22, M20, V8, V18, V21, Y7, AA22	VDD_P1	Power for pad group 1 – EBI0 and EBI1 pads
F5	VDD_P2	Power for pad group 2 – SDC3 pads
D5, F26, H13, H20, J6, R20, U5, W19, Y5, AC20, AE25	VDD_P3	Power for pad group 3 – most I/O pads
H16	VDD_P4	Power for pad group 4 – HSIC pads
J20, K9	VREF_DDR_C1	VREF for channel 1 of DDR memory
N21, V9, W20	VREF_DDR_C0	VREF for channel 0 of DDR memory
AA15, Y16	VDD_HDMI	Power for HDMI circuits
Y8, AA9, AA10, AC5	VDD_MIPI	Power for MIPI circuits (CSI and DSI)
AD11	VDD_LVDS	Power for LVDS circuits
Y13	VDD_LVDS_PLL	Power for LVDS PLL circuits
V14, N14, J14	VDD_PLL1	Power for PLL circuits – low voltage
K13, K14, K20, N15, U10, U14, U20	VDD_PLL2	Power for PLL circuits – high voltage
W13	VDD_PXO	Power for platform crystal oscillator circuits
J8	VDD_QFUSE_PRG	Power for programming Q-fuses; otherwise connect to ground
U11, V10, V11	VDD_QDSP6	Power for QDSP6 – application processor
T1	VDD_USBPHY1_1P8	Power for USB PHY interface 1 – low voltage
P1	VDD_USBPHY1_3P3	Power for USB PHY interface 1 – high voltage
J3	VDD_USBPHY3_1P8	Power for USB PHY interface 3 – low voltage
J1	VDD_USBPHY3_3P3	Power for USB PHY interface 3 – high voltage
N6	VDD_USBPHY4_1P8	Power for USB PHY interface 4 – low voltage
L1	VDD_USBPHY4_3P3	Power for USB PHY interface 4 – high voltage
N7	VDDA_GPS	Power for GPS circuits
AA18, AD18	VDDA_PCIE	Power for PCIe interface
P9	VDDA_WLAN	Power for WLAN circuits
AA17, AC16	VDD_SATA	Power for Serial ATA circuits
G4	VREF_SDC	Reference voltage for secure digital controller circuits

Table 2-13 APQ8064E pin descriptions – ground pins

Pin #	Pin name	Functional description
C5, C9, C13, C16, C20, C23, E11, E18, E26, F4, G7, G9, G13, G16, G20, G22, H1, J2, J5, J7, J10, J13, J22, J26, K8, K12, K15, K16, K17, K18, K19, K22, L2, L3, L6, L8, L9, L12, L13, L14, L17, L20, L24, M10, M11, M14, N2, N10, N11, N17, N19, N22, N26, P2, P6, P7, P8, P12, P13, P14, P15, P16, P18, P19, R7, R12, R13, R14, R17, T2, T6, T10, T11, T14, T17, T20, T22, T26, U9, U15, U16, U17, U19, V2, V12, V13, V15, V20, V24, W8, W10, W12, W16, W18, W22, Y4, Y14, Y15, Y17, Y18, Y19, Y22, Y26, AA8, AA16, AA19, AB6, AB11, AB16, AB20, AB22, AB23, AC6, AC26, AD4, AD6, AD20, AD28, AE1, AE2, AE3, AE18, AE20, AE24, AE27, AE28, AF3, AF4, AF18, AF20, AF28, AG18, AG22, AH18, AH22, AH23, AH24, AH25, AH26	GND	Ground

3 Electrical specifications

3.1 Absolute maximum ratings

Damage to the device can occur when operating the APQ8064E under conditions beyond its absolute maximum ratings (as listed in Table 3-1). Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure can affect device reliability.

NOTE Electrical specifications in this chapter are preliminary and subject to change.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power-supply voltages				
V_{DD_A2}	Analog circuits	–	V_{DD_A2} × 1.50	V
V_{DD_CORE}	Digital core circuits	–	1.65	V
V_{DD_MEM}	APQE internal memory	–	1.80	V
V_{DD_P1}	Digital P1 pad circuits	–	V_{DD_P1} × 1.50	V
V_{DD_P2}	Digital P2 pad circuits	–	V_{DD_P2} × 1.50	V
V_{DD_P3}	Digital P3 pad circuits	–	V_{DD_P3} × 1.50	V
V_{DD_P4}	Digital P4 pad circuits	–	V_{DD_P4} × 1.50	V
$V_{DD\_QDSP6\_APP}$	QDSP6 circuits	–	1.65	V
V_{DD_KR0}	Krait core circuits	–	1.50	V
V_{DD_KR1}		–	1.50	V
V_{DD_KR2}		–	1.50	V
V_{DD_KR3}		–	1.50	V
$V_{DD\_USBPHY1\_1P8}$	USB PHY low-voltage circuit	–	1.98	V
$V_{DD\_USBPHY3\_1P8}$		–	1.98	V
$V_{DD\_USBPHY4\_1P8}$		–	1.98	V
$V_{DD\_USBPHY1\_3P3}$	USB PHY high-voltage circuit	–	4.95	V
$V_{DD\_USBPHY3\_3P3}$		–	4.95	V
$V_{DD\_USBPHY4\_3P3}$		–	4.95	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
$V_{DD\_QFUSE\_PRG}$	Qfuse programming voltage	–	3.24	V
Signal pins				
V_{IN}	Voltage on any nonpower input or output supply pin	–	V_{DD} + 0.50	V
I_{IN}	Latch-up current	-100	100	mA

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature (Table 3-2). The APQ8064E meets all performance specifications listed in Section 3.4 through Section 3.13 when used within the recommended operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating conditions [1]

Parameter		Min	Typ [2]	Max	Unit
Power-supply voltages					
V_{DD_PXO}	Power supply for platform oscillator (27 MHz)	1.03	1.10	1.17	V
V_{DD_A2}	Analog 2 circuits – high voltage	1.674	1.80	1.98	V
V_{DD_MIPI}	Power for MIPI circuits (CSI and DSI)	1.11	1.17	1.23	V
V_{DD_HDMI}	Power for HDMI circuits	1.70	1.80	1.95	V
V_{DD_PLL1}	Power for low-voltage PLL circuits	0.975	1.05	1.225	V
V_{DD_PLL2}	Power for high-voltage PLL circuits	1.70	1.80	1.95	V
V_{DD_LVDS}	Power for low-voltage differential signals	1.70	1.80	1.90	V
$V_{DD\_LVDS\_PLL}$	Power for LVDS PLL circuits	1.14	1.175	1.21	V
V_{DDA_GPS}	Power for GPS analog circuits	1.15	1.30	1.45	V
V_{DD_PCIE}	Power for PCI Express interface	1.674	1.80	1.98	V
V_{DDA_WLAN}	Power for WLAN analog circuits	1.209	1.3	1.378	V
Power-supply voltages – memory					
V_{DD_MEM} [3]	APQE internal system memory				
High		1.075	1.15	1.225	V
Nominal		0.975	1.05	1.125	V

Table 3-2 Recommended operating conditions [1] (cont.)

Parameter		Min	Typ [2]	Max	Unit
Power-supply voltages – processors					
V_{DD_CORE} [3]	Digital core				
High		1.075	1.15	1.225	V
Nominal		0.975	1.05	1.125	V
V_{DD_QDSP6} [3]	QDSP6 application processor 492 MHz [4]				
PVS = 000		1.000	1.050	1.100	V
PVS = 001		0.95	1.000	1.050	V
PVS = 010		0.900	0.950	1.000	V
V_{DD_KR0}, V_{DD_KR1}, V_{DD_KR2}, V_{DD_KR3} [3]	Krait application microprocessor 0, 1, 2, and 3 operating at 1512 MHz [4]				
PVS = 0000		1.1175	1.2250	1.2750	V
PVS = 0001		1.1150	1.2000	1.2500	V
PVS = 0010		1.1125	1.1750	1.2250	V
PVS = 0011		1.1000	1.1500	1.2000	V
PVS = 0100		1.0750	1.1250	1.1750	V
PVS = 0101		1.0500	1.1000	1.1500	V
PVS = 0110		1.0375	1.0875	1.1375	V
PVS = 0111		1.0250	1.0750	1.1250	V
PVS = 1000		1.0125	1.0625	1.1125	V
PVS = 1001		1.0000	1.0500	1.1000	V
PVS = 1010		0.9875	1.0375	1.0875	V
PVS = 1011		0.975	1.0250	1.0750	V
PVS = 1100		0.9625	1.0125	1.0625	V
PVS = 1101		0.950	1.0000	1.0500	V
PVS = 1110		0.9375	0.9875	1.0375	V
Power-supply voltages – pads					
V_{DD_P1}	Pad group 1 – EBI0 and EBI1				
	DDR3	1.425	1.50	1.575	V
	DDR3L	1.283	1.35	1.450	V
V_{DD_P2}	Pad group 2 – dual voltage SDC3 (1.8 V or 2.95 V)	–	–	–	
2.95 V		2.75	2.95	3.00	V
1.80 V		1.70	1.80	1.95	V
V_{DD_P3}	Pad group 3 – most pads and peripheral I/Os	1.70	1.80	1.95	V

Table 3-2 Recommended operating conditions [1] (cont.)

Parameter		Min	Typ [2]	Max	Unit
V_{DD_P4}	Pad group 4 – HSIC I/O	–	–	–	
Used as GPIO		1.70	1.80	1.95	V
Used as HSIC		1.15	1.20	1.30	V
$V_{DD\_QFUSE\_PRG}$	Qfuse programming voltage	1.65	1.80	1.95	V
$V_{DD\_USBPHY1\_1P8}$	USB PHY pad group (1.8 V)	1.73	1.80	1.87	V
$V_{DD\_USBPHY3\_1P8}$		1.73	1.80	1.87	V
$V_{DD\_USBPHY4\_1P8}$		1.73	1.80	1.87	V
$V_{DD\_USBPHY1\_3P3}$	USB PHY pad group (3.3 V)	2.97	3.3 [5]	3.63	V
$V_{DD\_USBPHY3\_3P3}$		2.97	3.3	3.63	V
$V_{DD\_USBPHY4\_3P3}$		2.97	3.3	3.63	V
Thermal condition					
T_J	Junction temperature	–	–	+105	°C
T_a	Operating temperature	-40	+25	+85	°C

1. The maximum and minimum data are preliminary and are subject to change based on characterization results.
2. Typical voltages represent the recommended output settings of the PMICs.
3. Refer to *Application Note: APQ8064 Clock Plan and PVS* (80-N9344-1) for details.
4. These are special characteristics.
5. The companion PMIC currently sets the USB PHY 3.3 V rail to 3.075 V by default, due to power considerations. Customers need to ensure that, at a minimum, 2.97 V is observed on the VDD_USBPHY_3P3 pin so that it is within the USB PHY design specifications.

3.3 Power distribution network

This section covers the power delivery network (PDN) maximum impedance specification.

3.3.1 PDN system specification (PCB + baseband IC)

Table 3-3 lists the PCB + baseband IC PDN requirements. Meeting this specification requires the use of a commercial circuit simulator program (e.g., ADS) and APQ8064E S-parameter model. *QTI is not releasing the APQ8064E S-parameter model. Therefore, QTI will perform PCB + baseband IC simulation upon request.*

Table 3-3 PCB + baseband IC power distribution network impedance vs. frequency

Power domain	Required PCB routing inductance (caps shorted) [1]	Maximum impedance (mΩ)		
		DC to 300 kHz	300 kHz to 25 MHz	25 MHz to 500 MHz
V_{DD}MX	<500 pH	15	60	250
V_{DD}CX	<500 pH	15	60	250

Table 3-3 PCB + baseband IC power distribution network impedance vs. frequency

Power domain	Required PCB routing inductance (caps shorted) [1]	Maximum impedance (mΩ)		
		DC to 300 kHz	300 kHz to 25 MHz	25 MHz to 500 MHz
V_{DD_APC0}	<500 pH	15	60	250
V_{DD_APC1}	<500 pH	15	60	250
V_{DD_APC2}	<500 pH	15	60	250
V_{DD_APC3}	<500 pH	15	60	250

1. Meeting the PCB routing inductance is the required starting point to reap maximum benefits from the PDN capacitor optimization process described in *PDN Capacitor Optimization Guidelines* (80-VT310-15).

3.3.2 PDN specification (PCB-only)

Table 3-4 lists the PCB-only PDN requirements.

Table 3-4 PCB-only PDN impedance vs. frequency

Power domain	Maximum impedance (mΩ)		
	DC to 300 kHz	300 kHz to 15 MHz	15 MHz to 25 MHz
$V_{DD}MX$	15	60	100
$V_{DD}CX$	15	60	100
V_{DD_APC0}	15	60	100
V_{DD_APC1}	15	60	100
V_{DD_APC2}	15	60	100
V_{DD_APC3}	15	60	100

3.4 DC power characteristics

3.4.1 Average operating current

Operating currents will be detailed in a future application note.

3.4.2 Maximum currents (for selecting source regulators)

Maximum currents will be detailed in a future application note.

3.5 Power sequencing

The PMM8920E includes poweron circuits that provide the proper power sequencing for the entire APQ8064E chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. Refer to the *PMM8920 Power Management Module Device Specification* (LM80-P0598-4) for details.

A high-level summary of the APQ8064E's required early powerup sequence is:

1. V_{DD_MEM} / V_{DD_PLL1} (VREG_L24 on PM8921)
2. V_{DD_CORE} (VREG_S3 on PM8921)
3. $V_{DD\_P3(GPIO)}$(VREG_S4 on PM8921)
4. $V_{DD\_P1(EBI)}$ (VREG_L25 on PM8921)
5. VREF_DDR_C1/VREF_DDR_C2
6. V_{DD_PXO} (VREG_L1 of PM8921)
7. $V_{DD\_USBPHYX\_1P8}$ (HS USB 1.8 V), (VREG_L4 of PM8921)
8. V_{DD_P2} (SDC 2.95 V), (VREG_L7 of PM8921)
9. V_{DD_SDCARD} (SD VDD), (VREG_L6 of PM8921)
10. $V_{DD\_USBPHYX\_3P3}$ (HS USB 3.3 V), (VREG_L3 of PM8921)
11. eMMC VCC (VREG_L5 of PM8921)

Comments regarding this sequence:

- The core voltage (V_{DD_CORE}) needs to power up before the pad circuits (V_{DD_PX}) so that internal circuits can take control of the I/Os and pads.
  - If pad voltages power up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until V_{DD_CORE} powers on.
- The pad voltages need to precede the analog voltages (V_{DD_AX}), since the SSBIs are initialized to their default states before V_{DD_AX} powers up (analog circuits are controlled by SSBI).
- V_{DD_QDSP6}, V_{DD_KR0}, V_{DD_KR1}, V_{DD_KR2} and V_{DD_KR3} (QDSP and Krait core circuits) can be powered up by software after the APQE has completed the boot process.
- Other non-critical supplies are included within the poweron sequence. Any other desired supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when V_{DD_CORE} reaches 90% of its value, the V_{DD_P3} supply can start ramping up.

NOTE $V_{DD\_QFUSE\_PRG}$ must be powered down before any of the pad power supplies are powered down.

3.6 Resource and power manager (RPM)

Main RPM objective: lower the IC's average power consumption – static (1) and dynamic (2)

1. Static power management (primarily to limit leakage current)
   - Avoids using the high-powered processor
   - Executes code exclusively from internal RAM
   - Enables reduced logic supply of 0.5 V
2. Dynamic power management
   - Rapidly configures shared system resources and power-level configurations without impacting active processes and workloads.
   - Achieves optimal clock rate and supply voltage settings according to workload.
   - Improves overall system power efficiency while maintaining quality-of-service.
   - Minimizes overhead and latency needed to make voltage and clock change decisions.

3.6.1 Key RPM features

- Fast response times, low latency – less than 1 ms for clock frequency requests, 10 ms for supply voltage requests
- Autonomous and coordinated controls
  - Adjusts frequency, voltage, and resource usage without impacting other subsystems
  - Controls shared resources without other subsystems being active
  - Supports voting mechanisms for resource management
- Security – RPM is trusted at all times
  - Authenticates and validates trust level of subsystems calling RPM
  - Employs QFPROM
  - The Krait applications processor is assumed to be the secure root-of-trust (SROT) after initial boot
- Performs initial boot, coordinates other subsystems' boot-ups
- Resources controlled include: power management; clock sources and routing (CXO, PXO, sleep); supply voltages; clock frequencies; temperature compensation; and elements of the other APQ subsystems

3.6.2 RPM system operation

- Highly flexible microprocessor-based engine
  - Algorithms can be modified to achieve optimal power efficiency over a product's range of concurrent operations.
  - Facilitates security features like memory protection and safely sharing resources with nonsecure processors (LPA, QDSP6, etc.).

- System's sleep controller
  - Puts other subsystems into various sleep states to reduce leakage currents.
  - Upon wakeup, resources are enabled as needed to meet the requested operations, and base security levels are restored (effectively a warm boot).
- Optimizes system performance
  - Dynamic clock and voltage scaling for shared clocks and voltage domains minimizes power dissipation.
  - Arbitrates requests from all subsystems for shared resources like CXO, PXO, supply voltages, PLLs, memory, peripherals, and clocks for better efficiency.
  - Enables, disables, and/or scales shared resources on demand.
  - Intelligent power management using data from processors, resources, and applications, plus reports from performance, temperature, and process monitors

3.7 Digital logic characteristics

Specifications for the digital I/Os depend on the pad voltage being used. Logic specifications are listed in Table 3-5, Table 3-6, and Table 3-8 for V_{DD_P2} , V_{DD_P3} , and V_{DD_P4}= 1.8 V, V_{DD_P1} = 1.5 V (PC-DDR3), V_{DD_P1} = 1.35 (PC-DDR3L), and V_{DD_P2} at 2.95 V (SD card interface), respectively.

Table 3-5 Digital I/O characteristics for V_{DD_PX} = 1.8 V nominal

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 × V_{DD_PX}	V_{DD_PX} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.35 × V_{DD_PX}	V
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
I_{IH}	Input high leakage current [1, 2]	No pulldown	–	2	µA
I_{IL}	Input low leakage current [1, 2]	No pullup	-2	–	µA
I_{IHPD}	Input high leakage current [1, 3]	With pulldown	5	30	µA
I_{ILPU}	Input low leakage current [2, 3]	With pullup	-30	-5	µA
V_{OH}	High-level output voltage [4]	CMOS, at pin-rated drive strength	V_{DD_PX} - 0.45	V_{DD_PX}	V
V_{OL}	Low-level output voltage [4]	CMOS, at pin-rated drive strength	0	0.45	V
I_{OZH}	Tri-state leakage current [1]	Logic high output, no pulldown	–	1	µA
I_{OZL}	Tri-state leakage current [2]	Logic low output, no pullup	-1	–	µA
I_{OZHPD}	Tri-state leakage current [1, 3]	Logic high output with pulldown	5	30	µA
I_{OZLPU}	Tri-state leakage current [2, 3]	Logic low output with pullup	-30	-5	µA
I_{OZHKP}	Tri-state leakage current [1, 3]	Logic high output with keeper	-15	-3	µA
I_{OZLKP}	Tri-state leakage current [2, 3]	Logic low output with keeper	3	15	µA

Table 3-5 Digital I/O characteristics for V_{DD_PX} = 1.8 V nominal

Parameter		Comments	Min	Max	Unit
I_{ISL}	Sleep crystal input leakage		-0.15	0.15	µA
I_{IHVKP}	High-V tolerant input leakage	With keeper	-1	–	µA
C_{IN}	Input capacitance [5]		–	5	pF

1. Pin voltage = V_{DD_PX} max. For keeper pins, pin voltage = V_{DD_PX} max - 0.45 V.
2. Pin voltage = GND and supply = V_{DD_PX} max. For keeper pins, pin voltage = 0.45 V and supply = V_{DD_PX} max.
3. See Table 2-1 for pullup, pulldown, and keeper details.
4. See Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
5. Input capacitance is guaranteed by design, but is not 100% tested.

Table 3-6 Digital I/O characteristics for V_{DD_P1}

Parameter		Comments	Min	Max	Unit
V_{DD_P1} = 1.5 V nominal (PC-DDR3)					
V_{IH}	High-level input voltage	CMOS	V_{ref} + 0.15 V	VDD_P1	V
V_{IL}	Low-level input voltage	CMOS	VSS	V_{ref} - 0.15 V	V
V_{IH} (AC)	High-level input voltage (AC)	V_{IH} (AC)	V_{ref} + 0.175	See Note 6	V
V_{IL} (AC)	Low-level input voltage (AC)	V_{IL} (AC)	See Note 6	V_{ref} - 0.175	V
V_{ref}	Reference voltage		0.49 × V_{DD_P1}	0.51 × V_{DD_P1}	
V_{IHD}(AC)	AC differential input high		2 × (V_{IH}(AC) - V_{ref})	See Note 6	V
V_{ILD}(AC)	AC differential input low		See Note 6	2 × (V_{IL}(AC) - V_{ref})	V
I_{IH}	Input high leakage current [1]	No pulldown	–	2	µA
I_{IL}	Input low leakage current [2]	No pullup	-2	–	µA
I_{IHPD}	Input high leakage current [1, 3]	With pulldown	40	200	µA
I_{ILPU}	Input low leakage current [2, 3]	With pullup	-200	-40	µA
V_{OH}	High-level output voltage [4]	CMOS, at pin rated drive strength	0.8 × V_{DD_P1}	–	V
V_{OL}	Low-level output voltage [4]	CMOS, at pin rated drive strength	–	0.2 × V_{DD_P1}	V
V_{IHD}	DC differential input high		2 × (V_{IH} - V_{ref})	See Note 6	V
V_{ILD}	DC differential input low		See Note 6	2 × (V_{IL} - V_{ref})	V
I_{OZH}	Tri-state leakage current	Logic high output, with pulldown	40	200	µA
I_{OZL}	Tri-state leakage current	Logic low output, with pullup	-200	-40	µA
C_{IN}	Input capacitance [5]		1	2	pF
$C_{I/O}$	I/O capacitance [5]	I/O, DQS, DQ, or clock pins	1.25	2.5	pF
V_{DD_P1} = 1.35 V nominal (PC-DDR3L)					
V_{IH}	High-level input voltage	CMOS	V_{ref} + 0.15 V	VDD_P1	V
V_{IL}	Low-level input voltage	CMOS	VSS	V_{ref} - 0.15 V	V
V_{ref}	Reference voltage		0.49 × V_{DD_P1}	0.51 × V_{DD_P1}	
V_{IHD}(AC)	AC differential input high		2 × (V_{IH}(AC) - V_{ref})	See Note 6	V
V_{ILD}(AC)	AC differential input low		See Note 6	2 × (V_{IL}(AC) - V_{ref})	V
V_{OH}	High-level output voltage [4]	CMOS, at pin rated drive strength	0.8 × V_{DD_P1}	–	V
V_{OL}	Low-level output voltage [4]	CMOS, at pin rated drive strength	–	0.2 × V_{DD_P1}	V
V_{IHD}	Differential input high	–	2 × (V_{IH} - V_{ref})	See Note 6	V

Table 3-6 Digital I/O characteristics for V_{DD_P1} (cont.)

Parameter		Comments	Min	Max	Unit
V_{ILD}	Differential input low	–	See Note 6	2 × (V_{IL} - V_{ref})	V
I_{OZH}	Tri-state leakage current	Logic high output, with pulldown	40	200	µA
I_{OZL}	Tri-state leakage current	Logic low output, with pullup	-200	-40	µA
C_{IN}	Input capacitance 5	–	1	2	pF
$C_{I/O}$	I/O capacitance 5	I/O, DQS, DQ, or clock pins	1.25	2.5	pF

1. Pin voltage = V_{DD_P1} max.
2. Pin voltage = GND and supply = V_{DD_P1} max.
3. See Table 2-1 for pullup, pulldown, and keeper details.
4. See Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
5. Input and I/O capacitances are guaranteed by design, but are not 100% tested.
6. Undefined, however single-ended signals need to be within their respective limits (V_{IH}, V_{IL}) as well as the limitations for overshoot and undershoot. See Table 3-7 and Figure 3-1.

Table 3-7 PC-DDR overshoot and undershoot limits

Parameter	PC-DDR3/3L	Units
Maximum peak amplitude allowed for overshoot area	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	V
Maximum overshoot area above V_{DDQ}	0.5	V
Maximum undershoot area below V_{SSQ}	0.5	V

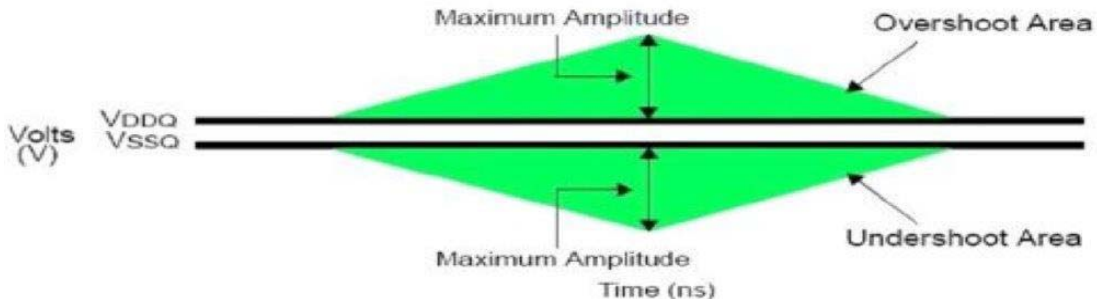


Figure 3-1 Overshoot and undershoot diagram

Table 3-8 Digital I/O characteristics for V_{DD_PX} = 2.95 V nominal (SD card interface)

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 × V_{DD_PX}	V_{DD_PX} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.35 × V_{DD_PX}	V
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
I_{IH}	Input high leakage current [1, 2]	No pulldown	–	10	µA
I_{IL}	Input low leakage current [1, 2]	No pullup	-10	–	µA
I_{IHPD}	Input high leakage current [1, 3]	With pulldown	10	60	µA
I_{ILPU}	Input low leakage current [2, 3]	With pullup	-60	-10	µA
I_{OZH}	Tri-state leakage current [1]	Logic high output, no pulldown	–	10	µA
I_{OZL}	Tri-state leakage current [2]	Logic low output, no pullup	-10	–	µA
I_{OZHPD}	Tri-state leakage current [1, 3]	Logic high output with pulldown	10	60	µA
I_{OZHPU}	Tri-state leakage current [2, 3]	Logic high output with pullup	-60	-10	µA
I_{OZHKP}	Tri-state leakage current [1, 3]	Logic high output with keeper	-25	-5	µA
I_{OZLKP}	Tri-state leakage current [2, 3]	Logic low output with keeper	5	25	µA
V_{OH}	High-level output voltage [4]	CMOS, at pin rated drive strength	V_{DD_PX} - 0.45	V_{DD_PX}	V
V_{OL}	Low-level output voltage [4]	CMOS, at pin rated drive strength	0	0.45	V
C_{IN}	Input capacitance [5]		–	5	pF

1. Pin voltage = V_{DD_PX} max. For keeper pins, pin voltage = V_{DD_PX} max - 0.45 V.
2. Pin voltage = GND and supply = V_{DD_PX} max. For keeper pins, pin voltage = 0.45 V and supply = V_{DD_PX} max.
3. See Table 2-1 for pullup, pulldown, and keeper details.
4. See Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
5. Input capacitance is guaranteed by design, but is not 100% tested.

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-2) with respect to the drive current (see Table 2-1). They can be calculated using these relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100} \right)$$

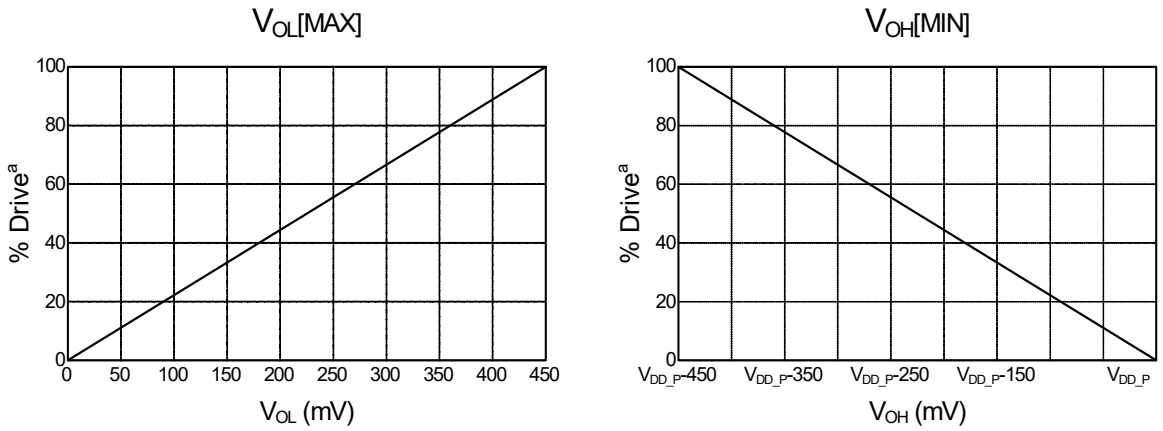


Figure 3-2 IV curve for V_{OL} and V_{OH} (valid for all V_{DD_PX})

3.8 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics are included here.

NOTE All APQ8064E devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.8.2.

3.8.1 Timing diagram conventions

The conventions used throughout this document for timing diagrams are shown in Figure 3-3. For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown, the meaning depends on the signal.
  - A single signal indicates *don't care*.
  - In the case of bus activity, the display of both high and low levels indicates that the processor or external interface is driving a value, but that this value may or may not be valid.

To account for external load conditions, rise or fall times must be added to parameters that start timing at the APQ device and terminate at an external device (or vice versa). Adding the rise and fall times is equivalent to applying capacitive load-derating factors.

NOTE Board designers: use the relevant APQ8016E IBIS file for this analysis.

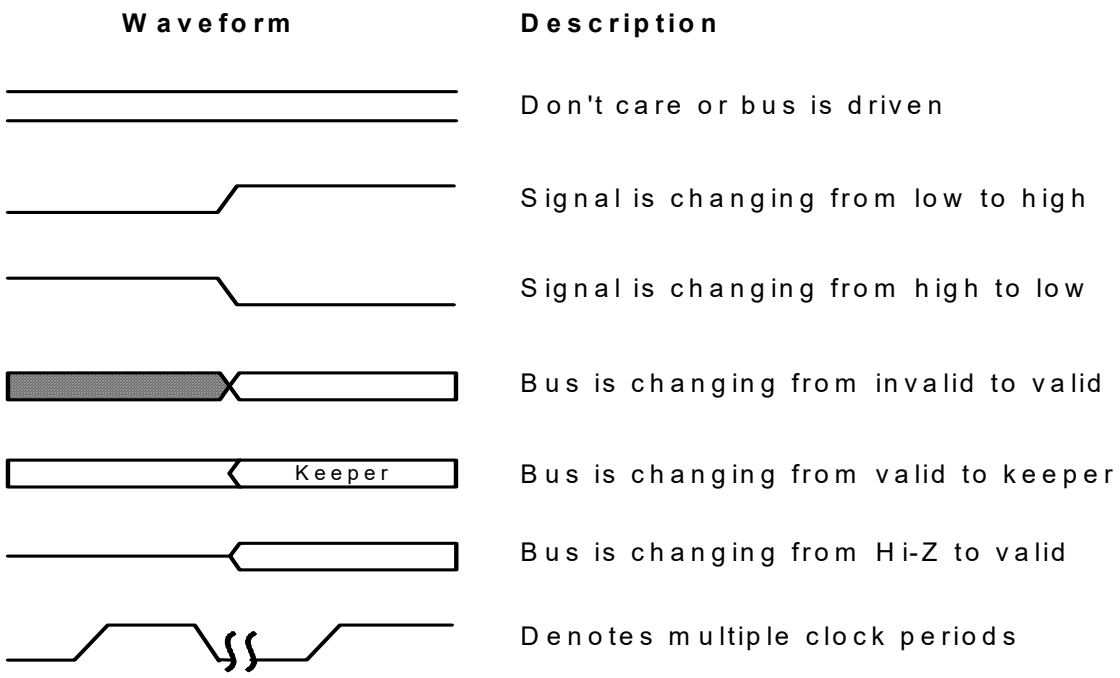


Figure 3-3 Timing diagram conventions

3.8.2 Rise and fall time specifications

The testers that characterize APQ8064E have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-4.

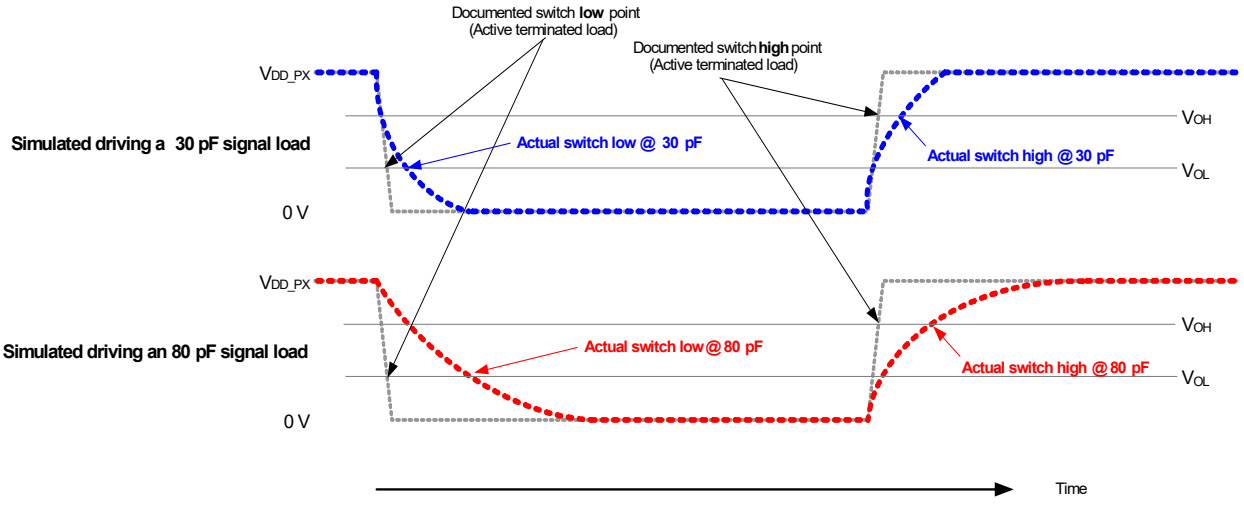


Figure 3-4 Rise and fall times under different load conditions

3.9 Memory controllers

APQ8064E contains two 32-bit memory controllers, EBI0 and EBI1. Each controller provides control signals, multiplexed addresses, and a bi-directional data bus. All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup-time numbers can get worse and hold-time numbers can get better.

3.9.1 Key DDR memory controller features

- Supports DDR on address bus
- Two major clock domains (AXI slave and DDR controller)
- Multiple AXI-to-DDR clock modes
  - Synchronous (1:1), iso-synchronous (1:2), asynchronous
- Highly flexible with many configurable parameters, including interface timing
- Flexible memory page management with various page open/close policies
- Out-of-order command execution and read data return
- Multiple high-priority tiers for sophisticated handling of priority requests
- Dynamic clock frequency switching
- 512-byte write data buffer and 512-byte read data FIFO
- Embedded memory protection unit (XPU) guards against unauthorized access
- Sequential burst support; no interleave burst support
- Auto-refresh, temperature adjusted auto-refresh, posted auto-refresh, and self-timed refresh
- I/O calibration
- DIMs handle center-aligning of memory controls and data
- Performance monitors with event outputs to SPDM
- Powerdown and deep powerdown (DPD) support

3.9.2 Secure digital card (SDC) controller

The APQ8064E IC provides up to four SD interfaces that provide the following features or functions.

- Clock output up to 104 MHz on SDC1/SDC2 and up to 208 MHz on SDC3; up to 67 MHz on the other interfaces
- 1.8 V/2.85 V dual-voltage operation on SDC3; 1.8 V operation on the other three
- Support for SDIO host mode
- SDIO compatible WLAN (802.11)
- Interface with SD/MMC memory cards up to 2 TB
- 10 k pull-up resistor on command pin; placeholder pull-ups are recommended on the data lines

Table 3-9 Secure digital card

SDC	Function	Width	Maximum clock rate
SDC1	eMMC	8-bits	104 MHz SDR at 1.8 V 152 MHz DDR at 1.8 V
SDC2	Available	4-bits	104 MHz SDR at 1.8
SDC3	SD/MMC	4-bits	208 MHz SDR at 1.8 V 52 MHz DDR at 1.8 V
SDC4	Available	4-bits	52 MHz DDR at 1.8 V

3.9.3 EBI0 and EBI1

3.9.3.1 EBI0 and EBI1 pad drive strengths

Pads for EBI0 and EBI1 are tailored for the 1.5 V/1.35 V interface and are source-terminated. Before the source termination, the pad drive strength is 15 mA to 60 mA. But at the pads, after the source termination, the drive strength at I_{OL}, IOH is equivalent to 1.3 mA to 5.15 mA for DDR3 configuration in non-linear steps when the JEDEC standard range (90% to 10%) is followed.

3.9.3.1.1 DDR3 SDRAM clock

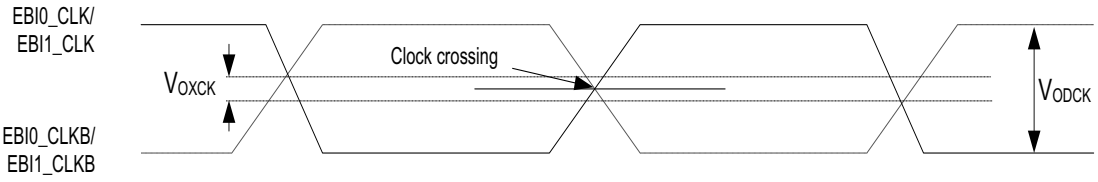


Figure 3-5 DDR3 SDRAM differential clock signal

Table 3-10 DDR3 SDRAM differential clock timing parameters

Parameter		Min	Max	Unit
1/t(ck)	DDR3 clock frequency	400	533	MHz
V_{IXCK}	Differential input cross-point voltage relative to VDD/2 for CK, CK# [1]	-0.15	0.15	V
V_{ODCK}	AC differential output voltage	0.35		V

1. Assumes full optimization of PCB system design.

3.9.3.1.2 DDR3 SDRAM strobe signal

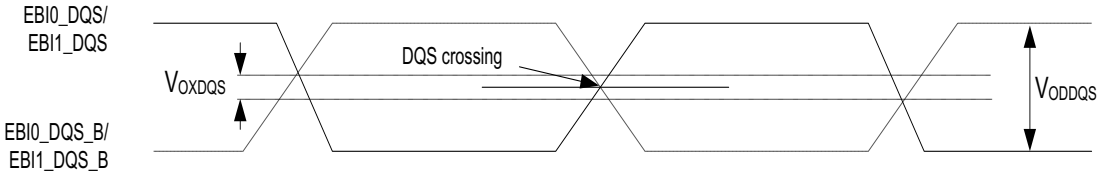


Figure 3-6 DDR3 SDRAM differential strobe signals

Table 3-11 DDR3 SDRAM differential strobe timing parameters

Parameter		Min	Max	Unit
V_{ODDQS}	AC differential output voltage	–	0.35	V
V_{IXDQS}	Differential input cross-point voltage relative to VDD/2 for DQS, DQS# [1]	-0.15	0.15	V

1. Assumes full optimization of PCB system design.

3.9.3.1.3 DDR3 SDRAM timing

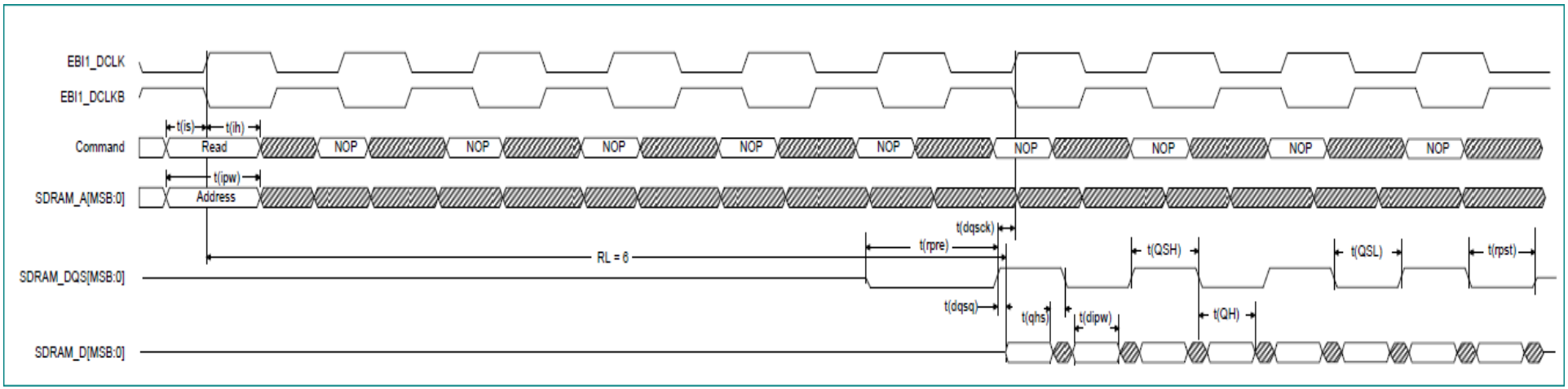


Figure 3-7 DDR3 SDRAM read timing

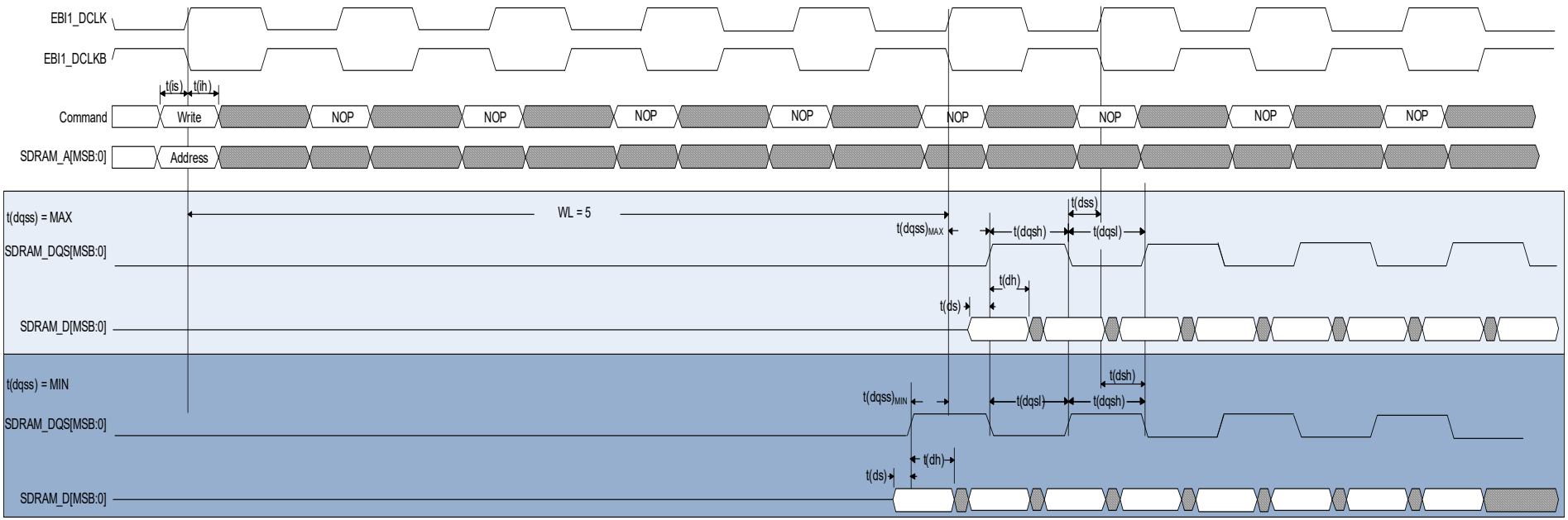


Figure 3-8 DDR3 SDRAM write timing

Table 3-12 DDR3/DDR3L SDRAM memory specification

Parameter	Symbol	Min	Max	Units
Average clock period	tCK(avg)	1.875		nS
Average high pulse width	tCK(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.43		tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.43		tCK(avg)
Cycle-to-cycle period jitter	tJIT(cc)	180		ps
Clock period jitter	tJIT(per)	-90	90	ps
Command and address setup time to CK, CK#	tIS (DDR3)	275	–	ps [1]
Command and address setup time to CK, CK#	tIS (DDR3L)	275	–	ps [1]
Command and address hold time from CK, CK#	tIH(DDR3)	200	–	ps [1]
Command and address hold time from CK, CK#	tIH(DDR3L)	200	–	ps [1]
Control and address input pulse width for each input	tIPW	780	–	ps
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	tCK(avg) [2]
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	–	tCK(avg) [2]
DQS, DQS# falling edge hold time to CK, CK# rising edge	tDSH	0.2	–	tCK(avg) [2]
DQS, DQS# differential output high pulse width	tDQSH	0.45	0.55	tCK(avg)
DQS, DQS# differential output low pulse width	tDQSL	0.45	0.55	tCK(avg)
DQS, DQS# differential WRITE preamble	tWPRE	0.9	–	tCK(avg)
DQS, DQS# differential WRITE postamble	tWPST	0.3	–	tCK(avg)
Data setup time to DQS, DQS# referenced to $V_{ih(ac)}/W_{il(ac)}$ levels	tDS (DDR3)	75	–	ps [1]
Data setup time to DQS, DQS# referenced to $V_{ih(ac)}/W_{il(ac)}$ levels	tDS (DDR3L)	75	–	ps [1]
Data hold time from DQS, DQS# referenced to $V_{ih(dc)}/W_{il(dc)}$ levels	tDH (DDR3)	100	–	ps [1]
Data hold time from DQS, DQS# referenced to $V_{ih(dc)}/W_{il(dc)}$ levels	tDH (DDR3L)	100	–	ps [1]
DQ and DM output pulse width for each output	tDIPW (OUT)	490	–	ps
DQS, DQS# rising edge input access time from rising CK, CK#	tDQSCK	-300	300	ps
DQS, DQS# differential input high time	tQSH	0.38	–	tCK avg)
DQS, DQS# differential input low time	tQSL	0.38	–	tCK(avg)
DQS, DQS# to DQ skew, per group, per access	tDQSQ	–	150	ps
DQ input hold time from DQS, DQS#	tQH	0.38	–	tCK(avg)
DQS, DQS# differential READ preamble	tRPRE	0.9	–	tCK(avg)
DQS, DQS# postamble	tRPST	0.3	–	tCK(avg)

1. Measurement at the APQE output pin with 50-ohm termination to $V_{DD\_P1/2}$.
2. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied (that is, tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing.

3.9.4 eMMC NAND flash on SDIO

NAND flash can be supported through the SDIO ports. See Section 3.11.6 for SDIO details.

- Fourth-generation SD card controller, known as SDCC4
- Supports eMMC and eSD devices; MMC v4.5 and SDIO v3.0
  - eMMC will be tested on in-house evaluation platforms
- Up to 104 MHz (SDR)
- Requires 10 k to 100 k pull-up resistors on DATA[7:0] and CMD signals
- Internal pull-up resistors can be used if power consumption and BOM count are concerns
  - Include placeholders for external pull-up resistors, to ensure compliance is met on a reference board design.

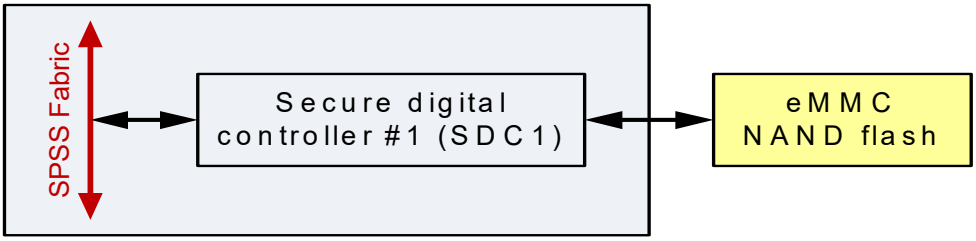


Figure 3-9 SCD1 and eMMC

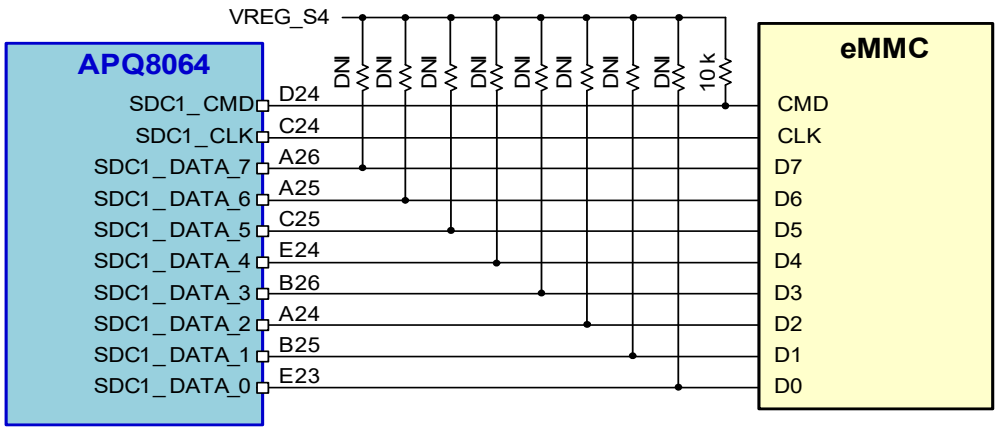


Figure 3-10 SDC1 high-level diagram

- The SDC1 port connects to an embedded NAND flash memory device.
  - 1.8 V interface (VREG_S4).
  - The memory device also requires 2.95 V (VREG_L5, not shown).
  - eMMC NAND via SDC1 is the primary boot device

See Section 3.11.6 for secure digital card controller interfaces.

3.10 Multimedia

The multimedia functions supported by the APQ8064E that require external access (and therefore I/O specification) include:

- Camera interfaces
- Audio/visual (A/V) outputs
- Display support

Pertinent specifications for the associated I/Os are stated in the following subsections.

In addition, the APQE supports the I^2S (Section 3.11.8.1) interface.

3.10.1 Camera serial interfaces (CSI)

The APQ8064E chipset supports a primary camera, a webcam, and 3D camera capability.

Key camera features include:

- Primary (using 4-lane MIPI_CSI) – supports CMOS and CCD sensors
  - Up to 20 MP in-line JPEG encode at 15 fps
  - 60 fps WXGA viewfinder frame rate
  - A wide variety of pixel manipulation, camera modes, image effects, and post-processing techniques are supported, including defective pixel correction.
  - VFE raw dump of CSI data at line rate (4 Gbps) to PCDDR3
  - SMIA++ support
  - Plus inter-integrated circuit (I2C) or SPI control
  - Per Mobile Industry Processor Interface (MIPI) specification
  - One high-speed clock lane and one to four data lanes
  - Low-voltage differential signaling (LVDS)
  - PHY block provides physical interface to camera sensor
- Secondary (using 2-lane MIPI_CSI) – provides webcam functions
  - Up to 8 MP
- 3D camera (using 1-lane MIPI_CSI)
  - Up to 8 MP
  - 3D camera support (using CSI0 and CSI1 plus webcam using CSI2)
- In-line JPEG processing
  - No external RAM requirement for image snapshot processing
  - Reduced shot-to-shot latency for multi-shot photos

Table 3-13 Camera interfaces

Parameter	Characteristic
Maximum sensor resolution	20 MP
Sensor input rate	228 MHz
Sensor pixel depth	8/10/12 bits per pixel
Supported input formats	Bayer RGB YCbCr 4:2:2 interleaved 12-8, 12-6, 10-8, 10-6 MIPI compression 8/10/12 MIPI raw
3D camera support	8 MP per channel (left and right)
Web camera support	8 MP

3.10.1.1 4-lane MIPI_CSI

Table 3-14 Summary of 4-lane MIPI_CSI support

Applicable standard	Feature exceptions	APQE variations
MIPI Alliance Specification v1.00 for Camera Serial Interface	None	None

3.10.1.2 2-lane MIPI_CSI

Table 3-15 Summary of 2-lane MIPI_CSI support

Applicable standard	Feature exceptions	APQE variations
MIPI Alliance Specification v1.00 for Camera Serial Interface	None	None

3.10.1.3 Image processing details

- MIPI camera serial interface (CSI)
  - 4-lane for primary camera
  - 2-lane for secondary camera such as web cam
  - 2-lane for 3D camera
- Camera operation data flow examples
- Video front-end (VFE)
- In-line JPEG
- HD codec
- Video pre-processing engine (VPE)
- Image processing examples

NOTE Parallel camera interface is not supported.

3.10.1.4 Video front-end (VFE)

VFE is the common interface between camera sensors and a variety of image and video compression standards (MPEG-4, H.263, and others).

Key VFE features include:

- Dedicated hardware blocks – like true DSC
- PCLK up 228 MHz in normal mode and 266 MHz in high clock mode
- Improves a DSP bandwidth and performance by offloading video processing tasks
- Entire image processing pipeline implemented with dedicated hardware blocks
- High programmability improves image quality and performance
- High-resolution, flexible image statistics for accurate and robust AWB/AE/AF
- AWB/color conversion statistics are collected and used to control VFE blocks
- AE/AF statistics for sensor compensation through I^2C
- Multiple simultaneous outputs
- Image sensor inputs are routed directly to external memory for bandwidth-efficient off-line processing

3.10.1.5 In-line JPEG

The in-line JPEG encoder reduces latency, useful as a frame-based encoder for encoding rotated pictures and for frame-based processing.

3.10.1.6 Video preprocessing engine (VPE)

Provides processing in real-time before encoding, including:

- Digital image stabilization
- Digital zoom
- Rotation
- Overlay

3.10.1.7 HD video codec

The HD video codec can encode or decode multiple 30 fps image streams of up to 1080p resolution (1920 x 1080). The support standards include:

- ITU-T H.264, ISO/IEC 14496-10
- ITU-T H.263
- ISO/IEC 14496-2 MPEG4 and DivX®
- ISO/IEC 13818-2 MPEG2
- SMPTE 421M VC-1

3.10.1.8 Example image processing capabilities

Table 3-16 Viewfinder/video mode

Parameter	Capability
Maximum viewfinder resolution	1080p
Maximum viewfinder refresh rate	30 fps
Max viewfinder / video output resolution	1080p
Comprehensive scaling and cropping	1080p
Viewfinder ASF	5x5
3A	Version 2.2
50/60 Hz beating	Auto flicker detect and correct
Lens roll-off correction	Mesh-based
Memory color enhancement	Viewfinder-based / WYSIWYG with snapshot
Real-time histogram	Y, RGB
Special effects	Sepia, B/W, solarization, etc.

Table 3-17 Snapshot / JPEG mode

Parameter	Capability
Maximum snapshot resolution	20 MP
Maximum input data rate	4096 Mbps 4-lane CSI 2048 Mbps 2-lane CSI
Simultaneous snapshot + 1080p encode	Yes
JPEG processing latency	TBD (to be provided in a future revision of this document)
Flash	Xenon and white LED
Mechanical shutter	Not supported
GPS capability via OEM application	Insert GPS lat/long into JPEG EXIF header
JPEG file control	By file size, by quality

3.10.2 A/V outputs

3.10.2.1 High-definition multimedia interface (HDMI)

The APQ8064E high-definition multimedia interface (HDMI) transmitter drives television sets, projectors, etc.

Table 3-18 Summary of HDMI support

Applicable standard	Feature exceptions	APQE variations
HDMI Specification Ver.1.4a	None	None

3.10.2.2 HDMI features

- HDMI Rev. 1.4a (w/HDCP)
- Integrated HDMI Tx core and HDMI PHY
- 1080p at 60 Hz refresh; 24-bit RGB color
- Up to 8-channel audio for 7.1 surround sound
- Dolby Digital Plus, Dolby True-HD, and DTS-HD Master
- Supported specifications: HDMI version 1.3b and HDCP system version 1.3
- Video pixel encoding: RGB444
- Video color depth: 24 bpp
- Video formats per CEA-861-D:
  - 640 × 480p, 1280 × 720p, 1920 × 1080i, 720 × 480p, 720 (1440) × 480i, all at 60 Hz
  - 1280 × 720p, 1920 × 1080i, 720 × 576p, 720(1440) × 576i, all at 50 Hz
  - 1280 × 720p, 1920 × 1080p at 24, 25, 30, 50, and 60 Hz
- Audio channels supported:
  - 2 (L, R; 2 channel L-PCM)
  - 8 (7.1 surround sound; 8 channel L-PCM 24-bit /192 kHz)
- Audio sample rates:
  - 32 kHz
  - 44.1 kHz
  - 48 kHz
  - 88.2 kHz
  - 96 kHz
  - 144 kHz
  - 176.4 kHz
  - 192 kHz

3.10.3 Display interfaces

Table 3-19 Display interfaces

Display interface	Target capabilities	Comment
4-lane MIPI DSI	Up to WQXGA (2048 × 1536), 24 bpp, 60 Hz refresh	Primary
LVDS	Up to WQXGA (2048 × 1536), 24 bpp, 60 Hz refresh	Alternate primary
4-lane MIPI DSI	Up to QHD (960 × 540), 24 bpp, 60 Hz refresh	Secondary
HDMI v1.4a w/HDCP	1080p, 60 Hz refresh	External (enable one at a time)
Concurrent dual display	2048 × 1536 (primary) + 960 × 540 (secondary)	

Table 3-19 Display interfaces

Display interface	Target capabilities	Comment
Processing support	**Comment**	
MDP 4.4	Latest version of fourth-generation mobile display processor hardware accelerator with support for 2048 × 1536 display resolution	

3.10.3.1 Example dual display

Table 3-20 Example dual display configurations

Example	Configuration
1	Primary panel using 4-lane DSI or LVDS + HDMI Tx; GUI on primary panel + 1080p video over HDMI
2	Primary panel using 4-lane DSI or LVDS + secondary panel using 4-lane DSI; Independent content on both displays (like video on one and GUI on other)

3.10.3.2 4-lane MIPI_DSI

Table 3-21 Summary of 4-lane MIPI_DSI support

Applicable standard	Feature exceptions	APQE variations
MIPI Alliance Specification v1.01 for Display Serial Interface	None	None

3.10.3.3 Low-voltage differential signaling support

Table 3-22 Summary of low-voltage differential signaling (LVDS) support

Applicable standard	Feature exceptions	APQE variations
This information will be included in a future revision of this document.		

3.10.3.4 Mobile display processors

Mobile display processors (MDP) is the latest version of fourth-generation mobile display processor hardware accelerator with support for 2048 × 1536 display resolution. Figure 3-11 shows an MDP high-level diagram.

- Dedicated accelerator hardware for transfers updated images from memory to display interfaces
- While the MDP transfers an image, it performs a final set of operations to that image
- Reduces circuit redundancy, offloads ARM and aDSP, improves system efficiency, and saves DC power.

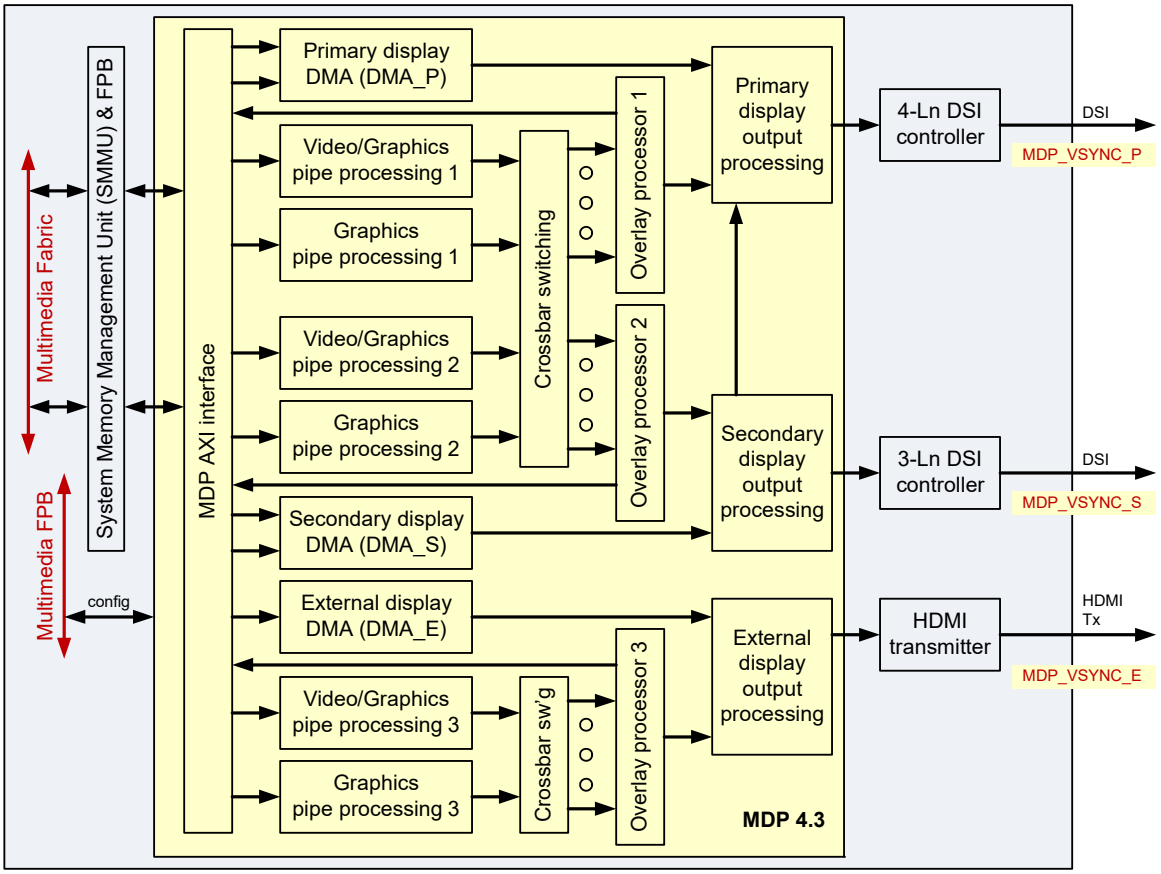


Figure 3-11 MDP high-level diagram

Table 3-23 Key MDP 4.4 features

Feature	Description
Graphics layer	
Input format	8/16/24-bit alpha RGB
Max resolution	2048 × 1536 LVDS or DSI; 1920 × 1200 other interfaces
Scaling	1x/8 to 20x
Filtering	Horizontal and vertical
Bit-depth promotion	Source cropping
Source cropping	
Video layer	
Input format	1/2-plane YUV
Max resolution	1080p each layer
Scaling	1x/8 to 20x
Filtering	Horizontal and vertical
Source cropping	

Table 3-23 Key MDP 4.4 features

Feature	Description
De-interlacing	
Sharpening	
Histogram data collect	
Noise inject (dithering)	
Contrast enhancement	
Noise filtering	
Blending	
V / G layer alignment	Arbitrary
Blend order constraints	None
Color keying	Video and graphics
Layer allocation for dual displays	4 layers, each can be allocated to primary or secondary display
Pre-multiplied alpha support	
LCD processing	
Integrated LCD controller	
HW cursor support (64 x 64 max)	
Gamma correction	
Up to 24 bits per pixel	
Color correction	
Dithering	
Histogram data collection	
HW-based ABL for power savings	
Background color	

3.10.3.5 Mobile Industry Processor Interface (MIPI) display serial interfaces

- Display serial interfaces
  - Per Mobile Industry Processor Interface (MIPI) specification
  - One high-speed clock lane and one to four data lanes
  - Low-voltage differential signaling (LVDS)
  - PHY block provides physical interface to display device
- DSI transmitter features
  - MIPI DSI specification version 1.01
  - MIPI D-PHY specification versions 0.65, 0.81, and 0.90
  - Video and command modes
    - Four data lanes, up to four virtual channels

- Up to 1 Gbps per lane high-speed mode bandwidth
- Video color depths
  - 24-bpp RGB888
  - 18-bpp RGB666 loose or packed
  - 16-bpp RGB565

3.10.3.6 Graphics

Graphic features include:

- Adreno 320™ graphics core
  - Supports high end dual displays (1080p + WQXGA)
  - Fully programmable unified shader architecture rendering
    - GPGPU shader program
  - Better pixel performance
    - Support for higher resolutions
    - Double pixel/texel throughput
    - Faster resolve rate
  - Dedicated on-chip memory for graphics
  - Better 2D performance
- 2D/3D graphics acceleration:
  - Adreno 320 graphics: 200 M peak triangles/sec; 6.4 B vector shader instructions/sec; 3.2 BP/sec; 3.2 B texel/sec
  - APIs include OpenGL ES 1.x, 2.0, and 3.0; Direct3D Dx9.x; C2D for 2D composition; OpenCL for Adreno 320
- Adreno 320 hardware acceleration of Web and UI applications:
  - Flash applications and fonts accelerated with native OpenCL 1.1 hardware
  - 2D bitmap elements rendered concurrent with 3D rendering
  - 2D rendered elements can be texture mapped to 3D UI concurrently

Table 3-24 Graphic specifications

Parameter	Capability
Clock	400 MHz / 325 MHz (turbo / nominal)
Peak vector shader instruction rate	6400M instructions per second
Peak 3D triangle rate	200M triangles per second
Peak 3D pixel draw rate	3200M pixels per second
2D pixel draw rate concurrent w/ peak 3D	TBD pixels per second

Table 3-24 Graphic specifications

Parameter	Capability
Combined 2D + 3D pixel draw rate	TBD pixels per second
Primary LCD max resolution	WSXGA
Dedicated hardware for 2D	Yes
APIs provided	OpenGLES 1.x, 2.0, 3.0 Direct3D Dx9.0 w/ Shader model 2.0 HLSL Direct3D Dx9.3 w/ Shader model 3.0+ HLSL OpenCL 1.1 embedded profile (for GPGPU) C2D (for 2D composition)

3.11 Connectivity

The connectivity functions supported by the APQ8064E include:

- High-speed USB port with built-in PHY and full-speed USB port (for USB-UICC only)
- PCI Express (PCIe) port
- Universal asynchronous receiver transmitter (UART) serial ports
- User identity module (UIM) ports
- Secure digital card controller (SDCC) ports
- Inter-integrated circuit (I^2C) interfaces for peripheral devices
- Inter-IC sound (I^2S) interfaces for digital audio support
- Serial peripheral interface (SPI) ports

Pertinent specifications for these functions, where appropriate, are stated in the following subsections.

The following interfaces are multiplexed to output pins by properly configuring the seven generic serial bus interface (GSBI) ports: UART, UIM, I^2C, and SPI.

NOTE In addition to the following hardware specifications, consult the latest software release notes for software-based performance features or limitations.

3.11.1 USB interfaces

Table 3-25 Summary of USB support

Applicable standard	Feature exceptions	APQE variations
Universal Serial Bus Specification, Rev. 2.0 (April 27, 2000 or later)	None	Operating voltages, system clock, and VBUS – see Table 3-26

Table 3-26 APQE-specific USBPHY specifications

Parameter	Comments	Min	Typ	Max	Unit
Supply voltages					
Dual-supply (see Table 3-2 for specifications)	–				
VDD_USBPHYX_1P8 pin		1.73	1.80	1.87	V
VDD_USBPHYX_3P3 pin		2.97	3.30	3.63	V
USBPHY_SYSCLK					
Frequency	19.2 MHz clock is required.	–	19.2	–	MHz
Clock deviation	–	-400	–	400	ppm
Jitter (peak-to-peak)	0.5 to 1.75 MHz	0	–	60	ppm
Duty cycle	–	40	–	60	%
Low-level input voltage (V_{IL})	–	–	–	0.6	V
High-level input voltage (V_{IH})	–	1.27	–	–	V
USBPHY_VBUS					
B-session valid	–	2.0	–	5.25	V

3.11.2 HSIC interfaces

Table 3-27 Supported HSIC standards and exceptions

Applicable standard	Feature exceptions	APQE variations
High-Speed Inter-Chip USB Electrical Specification, Version 1.0 (a supplement to the USB 2.0 specification – see Section 3.11.1)	Device mode not supported	None

3.11.3 PCIe interface

Table 3-28 Summary of PCIe support

Applicable standard	Feature exceptions	APQE variations
PCI Express Specification, Revision 2.0 (January 15, 2007 or later)	None	None

3.11.4 High-speed UART interface

Table 3-29 Summary of UART support

Applicable standard	Feature exceptions	APQE variations
EIA RS232-C	None	None

3.11.4.1 UART advantages

The UART_DM is used to support high-speed UART operations up to 4 Mbps and medium data-rate IrDA operations up to 1.152 Mbps.

Advantages of the UART_DM block include:

- Rate-controlled data mover with separate channel rate control interface (CRCI) channels for Rx and Tx
- 256 byte Rx and Tx FIFOs
- Access to the fast peripheral bus (32-bit wide AHB interface) rather than the slow bus
- Maintains traditional level interrupts directly to the microprocessor when the data mover is not available

Note that the UART_DM Tx and Rx channels are similar to the basic UART channels, except that the FIFOs are implemented in SRAM and the FIFO controls and IRQ generation are in the DM controller block.

3.11.5 UIM interface

Table 3-30 Summary of UIM support

Applicable standard	Feature exceptions	APQE variations
ISO/IEC 7816-3	None	None

3.11.5.1 UIM initialization

The APQ device can recognize and initialize a UIM only during its powerup sequence, not during regular operation.

During a powerup sequence, whether a true powerup or a soft-reset, the UIM clock and data lines are active as they execute their initialization process one UIM slot at a time (if more than one is used). After initialization, the slots' operation depends upon whether a module is detected.

- If a module is detected:
  - The data line stays active, even if data is not being transmitted (between accesses). It maintains its marking state (logic high) between accesses.
  - The clock is only active during accesses; it is turned off between accesses to save power. The state of the clock when off is programmable, and must be selected to support the module's characteristics.
  - Even though the clock is turned off between accesses, the interface is still active. The data, reset, and power lines all remain high (assuming an active-low reset).
  - Note that the interface stays on once the module is detected, even during APQ sleep modes; the current consumption continues.

- If a module is not detected (module not inserted, not recognized, or broken connection, etc.):
  - The interface is deactivated.
  - All lines are low and there is no chance to operate or communicate with a module until the next powerup sequence.

3.11.6 Secure digital card controller interfaces

Table 3-31 Summary of SDCC support

Applicable standard	Feature exceptions	APQE variations
Multi-Media Card Host Specification version 4.4.1 and 4.5	None	Timing specifications – see Figure 3-12 and Figure 3-13
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 3.0	None	

Single Data Rate - SDR

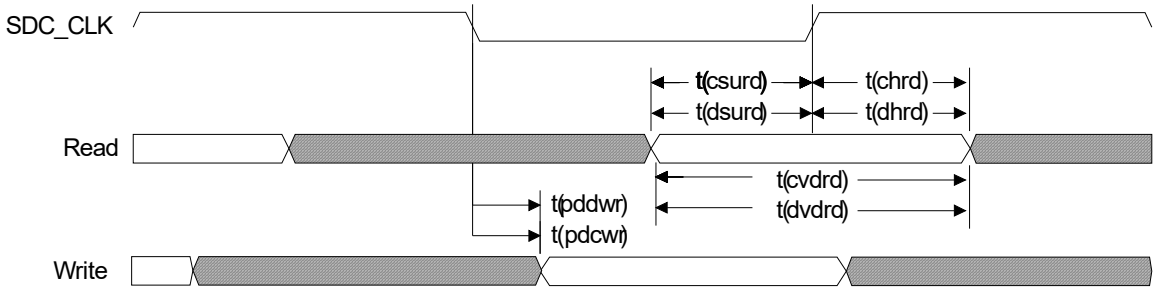


Figure 3-12 SDCC SDR timing waveforms

Double Data Rate - DDR

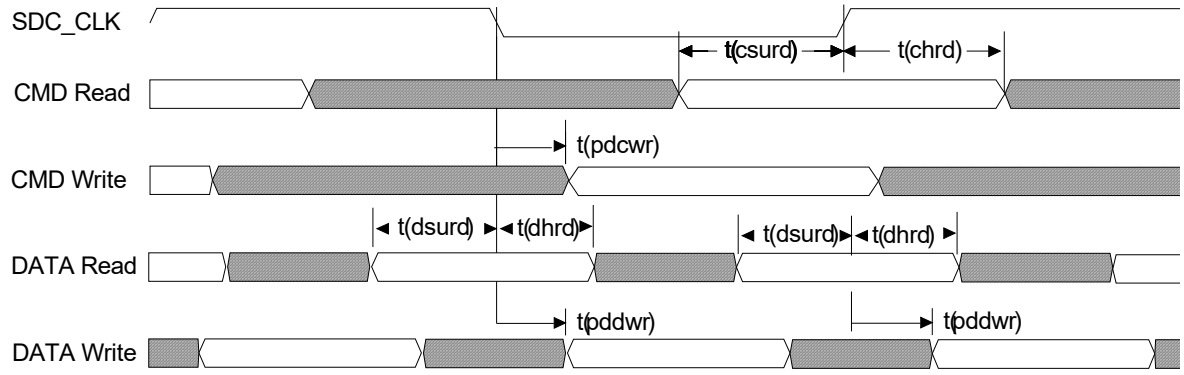


Figure 3-13 SDCC DDR timing waveforms

Table 3-32 SDC1/SDC3 DDR mode timing parameters [1]

Parameter		Min	Max	Unit
t(chrd)	Command hold	1.5	–	ns
t(csurd)	Command setup	6.3	–	ns
t(dhrd)	Data hold	1.5	–	ns
t(dsurd)	Data setup	2	–	ns
t(pddwr)	Propagation delay on data write	0.8	6	ns
t(pdcwr)	Propagation delay on command write	2.5	3	ns

1. SDC1 and SDC3 DDR mode timing parameters are for clock frequencies up to 52 MHz.

Table 3-33 SDC1 SDR mode timing parameters [1]

Parameter		Min	Max	Unit
t(chrd)	Command hold	1.50	–	ns
t(csurd)	Command setup	2.50	–	ns
t(dhrd)	Data hold	1.50	–	ns
t(dsurd)	Data setup	2.50	–	ns
t(pddwr)	Propagation delay on data write	-3.7	1.50	ns
t(pdcwr)	Propagation delay on command write	-3.7	1.50	ns

1. SDC1 SDR timing parameters is for the clock frequencies up to 104 MHz.

Table 3-34 SDC1/SDC3 SDR104 mode timing parameters [1]

Parameter		Min	Max	Unit
t(cvdrd)	Command valid	2.50	–	ns
t(dvdrd)	Data valid	2.50	–	ns
t(pddwr)	Propagation delay on data write	-1.45	0.85	ns
t(pdcwr)	Propagation delay on command write	-1.45	0.85	ns

1. SDC1/SDC3 SDR104 mode timing parameters are for the clock frequencies up to 104 MHz.

Table 3-35 SDC2/SDC4 SDR33 mode timing parameters [1]

Parameter		Min	Max	Unit
t(chrd)	Command hold	1.50	–	ns
t(csurd)	Command setup	7.65	–	ns
t(dhrd)	Data hold	1.50	–	ns
t(dsurd)	Data setup	7.65	–	ns
t(pddwr)	Propagation delay on data write	-6.0	3.82	ns
t(pdcwr)	Propagation delay on command write	-6.0	3.82	ns

1. SDC2/SDC4 SDR33 mode timing parameters are for the clock frequencies up to 66 MHz.

3.11.7 Audio interface

Two 2-pin SLIMbus interfaces and I^2S/I^2C bus are provided for audio and sensor usage.

The audio codec supports two control modes:

- MIPI SLIMbus: Data and control on the same data line
- I^2S/I^2C: Control over I^2C and data over I^2S

The SLIMbus core manages the Serial Low-power Inter-chip Media Bus (SLIMbus) audio interface. The SLIMbus complies with MIPI Alliance Specification for Serial Low-power Inter-chip Media Bus Version 1.01.01.

3.11.7.1 SLIMbus

- Two-wire, multi-drop interface that supports a wide range of digital audio and control solutions for mobile terminals
- Defined by the MIPI Alliance
- External framer mode not supported

3.11.7.2 SLIMbus features

- Audio, data, and control on single bus
- Lower pin count
- Supports 10+ components at typical bus lengths and speeds
- Supports multiple high-quality audio channels
- Multiple concurrent sample rates on one bus
- Efficient peer-to-peer communications
- Standardized message set
- Improved software reuse
- Increased interoperability
- Dynamic clock rates for optimizing power
- Maximum SLIMbus clock = 28.8 MHz

3.11.8 I^2C interface

Table 3-36 Summary of I^2C support

Applicable standard	Feature exceptions	APQE variations
I^2C Specification, version 2.1, January 2000 (Philips Semiconductor document number 9398 393 40011)	■ High-speed mode (3.4 Mbps) is not supported. ■ 10-bit addressing is not supported. ■ Fast mode plus (1 Mbps) is not supported.	None

3.11.8.1 I²C features

- Two-wire bus for inter-IC communications supports any IC fabrication process.
  - Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending upon the device function.
- The I²C controller provides an interface between the CPSS fast peripheral bus (FPB), an advanced high-performance bus (AHB), and the industry standard I²C serial bus.
  - It handles the I²C protocol and frees up the on-chip processor (and AHB) to handle other operations
  - It is I²C-compliant, high-speed mode (HS-mode)-compliant, and a master-only device
- I²C pins use GPIOs configured as open-drain outputs; the slave provides the pull-up resistor.
- Camera auto-focus control through I²C originates with the aDSP; a separate hardware request port is required at the I²C controller.

3.11.9 I²S interface

The APQ8064E has five separate I²S interfaces and they meet the timing given in this section.

- Multichannel I²S (MI²S)
- Codec microphone I²S
- Secondary microphone I²S
- Codec speaker I²S
- Secondary speaker I²S

Table 3-37 Supported I²S standards and exceptions

Applicable standard	Feature exceptions	APQ8064E variations
Philips Semiconductor, *I²S Bus Specification*, revised June 5, 1996		The APQ8064E meets or exceeds this standard. The only exception is the APQ8064E requires a 45/55 duty cycle when the SCK clock source is from an external source.

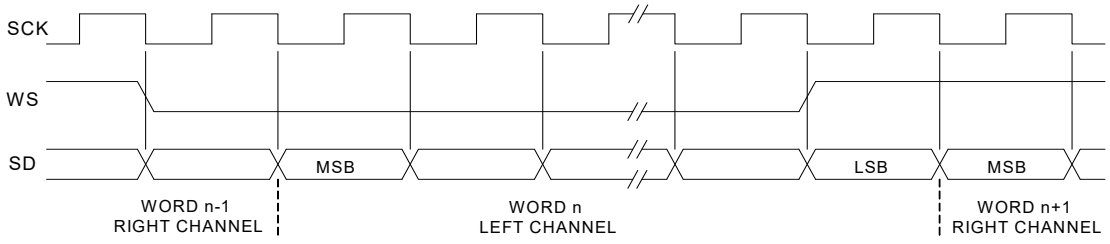


Figure 3-14 I²S interface basic timing

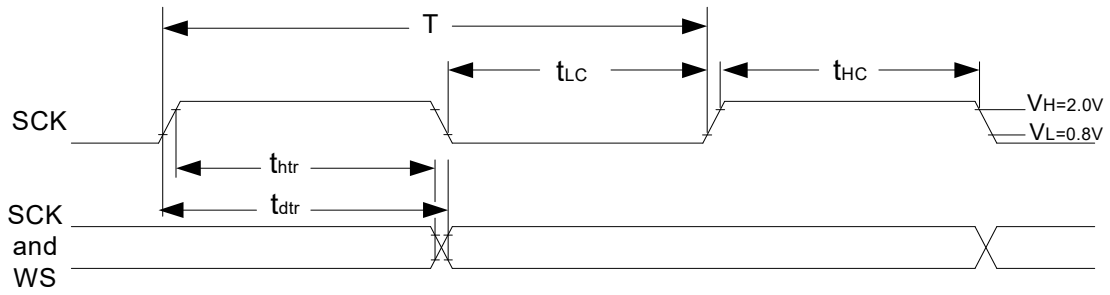


Figure 3-15 I²S interface transmitter timing

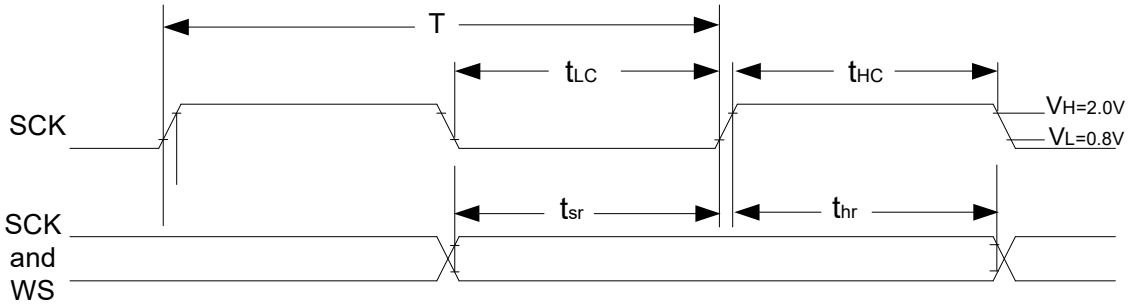


Figure 3-16 I²S interface receiver timing

Table 3-38 I²S interface timing using internal SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		12.288	MHz	C_L = 10 pF - 40 pF
Clock period	T	0		81.38	ns	C_L = 10 pF - 40 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF - 40 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF - 40 pF
Inputs SD*, WS						
Setup time	t_{sr}	16.276	–	–	ns	–
Hold time	t_{hr}	0	–	–	ns	–
Outputs SD*, WS						
Delay	t_{dtr}	–	–	65.1	ns	C_L = 10 pF - 40 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF - 40 pF

Table 3-39 I²S interface timing using external SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		12.288	MHz	C_L = 10 pF - 40 pF
Clock period	T	0		81.38	ns	C_L = 10 pF - 40 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF - 40 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF - 40 pF
Inputs SD*, WS						
Setup time	t_{sr}	16.27	–	–	ns	–
Hold time	t_{hr}	0	–	–	ns	–
Outputs SD*, WS						
Delay	t_{dtr}	–	–	65.1	ns	C_L = 10 pF - 40 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF - 40 pF

3.11.10 Serial peripheral interface

3.11.10.1 SPI protocol requirements

1. As an SPI master, the core supports several SPI system configurations, including 1 through 5 and multimaster.
2. As an SPI master, the core supports SPI_CS0_N, SPI_CS1_N, SPI_CS2_N, and SPI_CS3_N.
3. As an SPI master, the core supports SPI_CLK.
4. As an SPI master, when no transfers are taking place (IDLE), the core supports SPI_CLK_ IDLE_LOW and SPI_CLK_IDLE_HIGH.
5. As an SPI master, the core supports leaving the SPI_CLK running when no SPI_CS#_N is asserted (during IDLE).
6. As an SPI master, the core supports SPI_MOSI tri-state during IDLE (optional).
7. As an SPI master, the core supports Input_First_Mode.
8. As an SPI master, the core supports Output_First_Mode.
9. As an SPI master, the core supports any value of N between 4 and 32.
10. As an SPI master or slave, the core supports the following half-duplex modes (MDM is master-only):
    a. SPI_MOSI only with SPI_MISO held low
    b. SPI_MISO only with SPI_MOSI held low
    c. Half-duplex on a bidirectional signal (defined for system configuration 3 only).
11. As an SPI master, the core supports a mechanism to control the number of SPI_CLK ticks between the assertion of different SPI_CS signals. Even though there is no formal flow control

mechanism, a slave may require dead time between SPI_CS assertions – this capability meets that potential requirement.

12. As an SPI master, the core supports the SPI_CS_N master requirements.
13. As an SPI master, the core supports assertion of SPI_CS#_N between each transfer of size N (CS is normally de-asserted). As an option, SPI_CS#_N can be asserted for a “first transfer” and left asserted for T transfers through the “last transfer” T. Under this option, requirement #11 above still applies, but the SPI_CLK is turned off every N bits while SPI_CS#_N is left asserted. This corresponds to the multitransfer chip-select (MX_CS).
14. As an SPI master, the core supports configuring SPI_CS#_N as active high (optional).

3.11.10.2 Serial peripheral interface (master only)

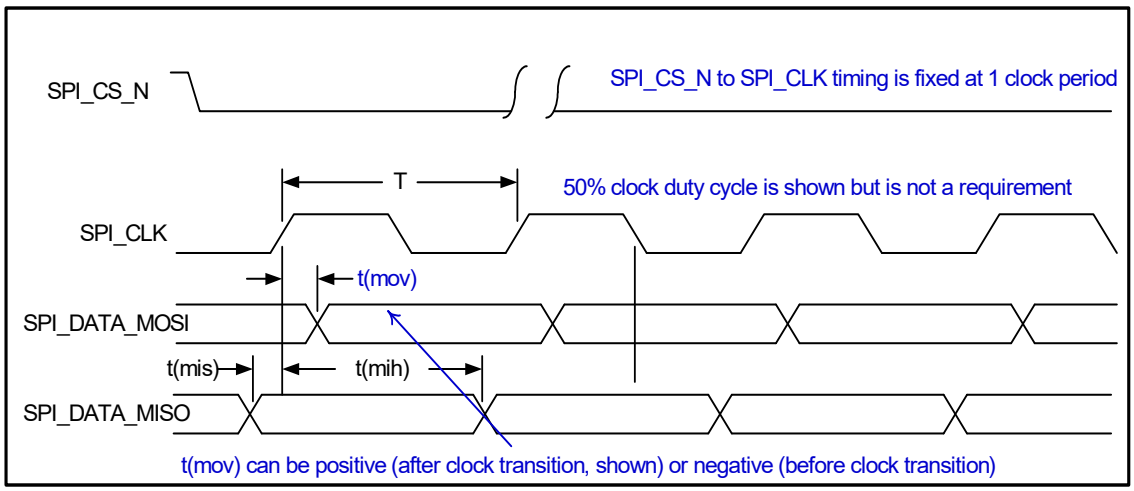


Figure 3-17 SPI master timing diagram

Table 3-40 SPI master timing characteristics (52 MHz max)

Parameter	Comments	Min	Typ	Max	Unit
SPI clock frequency		–	–	52	MHz
T (SPI clock period)		19.0	–	–	ns
t(ch)	Clock high	8.65	–	–	ns
t(cl)	Clock low	8.65	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

3.11.11 Transport stream interfaces

Table 3-41 Summary of TSIF support

Applicable standard	Feature exceptions	APQE variations
ITU-T H.222.0 Transport Stream (HTS); also known as ISO/IEC 13818-1	None	None

Table 3-42 Transport stream timing characteristics (96 MHz max)

Parameter	Comments	Min	Typ	Max	Unit
TSIF (clock frequency)		–	–	96	MHz
t(hddata)	Data hold	0.1	–	–	ns
t(hden)	Data enable hold	0.1	–	–	ns
t(hdsync)	Data sync hold	0.1	–	–	ns
t(sudata)	Data setup	4	–	–	ns
t(suenable)	Data enable setup	4	–	–	ns
t(susync)	Data sync setup	4	–	–	ns

3.11.12 Keypad interface

The PMIC hardware supports key press detection. The GPIOs can be configured to implement a keypad interface supporting a matrix of up to 18 rows by 8 columns. Performance specifications that are specific to the keypad interface are listed in Table 3-43.

Table 3-43 Keypad interface performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage		–	1.8	–	V
Load capacitance		–	–	100	pF
Sense lines					
Pull-up current		20.8	31.5	42.2	µA
Pull-down current		400	600	800	µA
Key-stuck delay	Number of 32 kHz cycles = 325,000	7.94	9.92	13.60	sec
Drive lines					
Drive strength	Open-drain outputs	–	0.6	–	mA

3.12 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, motor control, modes and resets, and JTAG and SWD functions as specified in this section.

3.12.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Other clocks are specified in this section.

3.12.1.1 LPASS clocks

- The LPASS PLL circuit is within the APQ's clock generation and distribution block.
- The LPASS clock controller (LCC) generates all the clocks needed for APQ audio functions, including the new SLIMbus and digital microphone interfaces.

3.12.1.1.1 Primary clock configuration

- The platform crystal oscillator (PXO, 27 MHz) is the reference source.
- The LPASS PLL output is routed to the LPASS, and selected as the LCC input signal.
- The LCC generates all audio clocks.
- Individual audio interfaces route the clocks to their functional blocks.
- Each interface allows an external clock source to be used and allows the generated clock to be routed externally.

3.12.1.2 Source oscillators and external clock connections

- GP_CLK outputs – direct clock signal
- GP_MN output – M/N:D counter output signal
- GP_PDM outputs – pulse density modulated (PDM) signal with configuration options:
  - Input source: PXO or CXO; without dividing (or with divide-by-4)
  - Enable/disable
  - Output polarity
  - Pulse density (number of output high counts versus low counts)

Table 3-44 Clock summary

Clock	Frequency	Usage
CXO – core crystal oscillator	19.2 MHz	Optional reference for LPASS, GSS, WCSS, and HSIC PLLs
PXO – platform crystal oscillator	27 MHz	Reference for all other PLLs
SLEEP_CLK – sleep clock	32.768 MHz	Reference during sleep mode

3.12.1.3 19.2 MHz core XO input

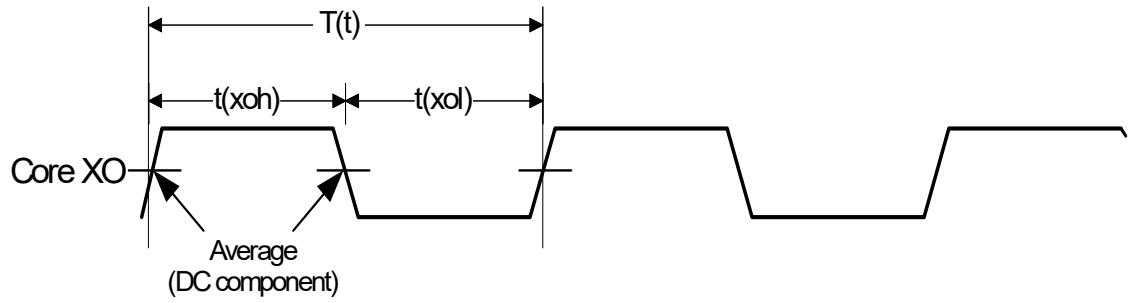


Figure 3-18 Core XO timing parameters

Table 3-45 Core XO timing parameters [1]

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Core XO logic high		22.6	–	29.5	ns
t(xol)	Core XO logic low		22.6	–	29.5	ns
T(t)	Core XO clock period		–	52.083	–	ns
1/T(t)	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. Refer to *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH+Xtal Mini-Specification (LM80-P0598-8)* for more details.

3.12.1.4 Sleep clock

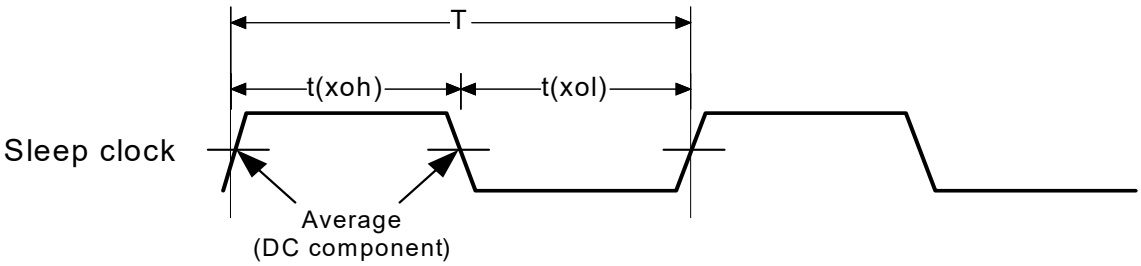


Figure 3-19 Sleep-clock timing parameters

Table 3-46 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T(t)	Sleep-clock period		–	30.518	–	µs
1/T(t)	Frequency		–	32.768	–	kHz

3.12.1.5 PXO (27 MHz) crystal oscillator

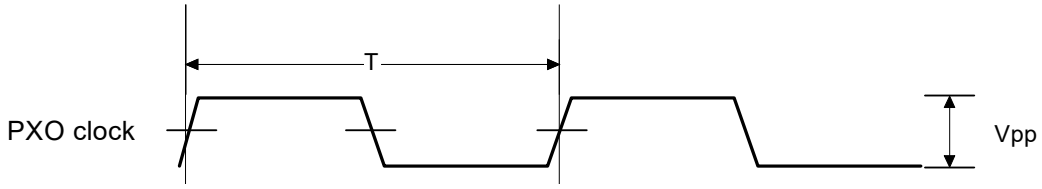


Figure 3-20 PXO (27 MHz) crystal oscillator timing parameters

Parameters for the 27 MHz crystal oscillator are listed in Table 3-47.

Table 3-47 PXO (27 MHz) crystal oscillator parameters

Parameter	Min	Typ	Max	Unit
Frequency	–	27	–	MHz
Frequency tolerance	-30	–	30	ppm
Series resistance (ESR)	–	–	60	Ω
Load capacitance	11	15	17	pF
Shunt capacitance	–	–	5	pF

3.12.2 Motor control

The PMIC supports silent incoming call alarms with its vibration motor driver. The vibration driver is a programmable voltage output that is referenced to V_{DD}; when off, its output voltage is V_{DD}. The motor is connected between V_{DD} and the VIB_DRV_N pin.

Performance specifications for the vibration motor driver circuit are listed in Table 3-48.

Table 3-48 Vibration motor driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Output voltage (V_m) error[1]	V_{DD} > 3.2 V; I_m = 0 to 175 mA;				
Relative error	V_m setting = 1.2 to 3.1 V	-6	–	+6	%
Absolute error	Total error = relative + absolute	-60	–	+60	mV
Headroom[2]	I_m = 175 mA	–	–	200	mV
Short circuit current	VIB_DRV_N = V_{DD}	225	–	600	mA

1. The vibration motor driver circuit is a low-side driver. The motor is connected directly to VDD, and the voltage across the motor is $V_m = V_{DD} - V_{out}$, where V_{out} is the PMIC voltage at VIB_DRV_N.
2. Adjust the programmed voltage until the lowest motor voltage occurs while still meeting the voltage accuracy specification. This lowest motor voltage ($V_m = V_{DD} - V_{out}$) is the headroom.

Some vibration motor features are:

- Vibration motor driver programmable from 1.2 to 3.1 V in 100 mV increments
- Programmable voltage output referenced to V_{DD}
- When off, its output voltage is V_{DD}
- Motor connected between V_{DD} and VIB_DRV_N

- Voltage across motor is $V_m = V_{DD} - V_{out}$
- V_{out} is the voltage at the PMIC pin.

3.12.3 Modes and resets

The mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.12.4 JTAG

The JTAG interface to the APQ8064E chipset provides debug, factory test, and board-level test support independent of the system logic. The JTAG interface provides control and observation of the boundary scan register and other scan registers used for device programming, security, and debug. The JTAG interface conforms to the ANSI/IEEE 1149.1 - 2001 and IEEE 1149.6 - 2003.

The chip has a primary JTAG interface on dedicated pins and an auxiliary interface (AUX JTAG) behind GPIOs. Both JTAG ports can be simultaneously run in various modes to allow simultaneous debugging of ARM9, Krait, and ARM7 processors.

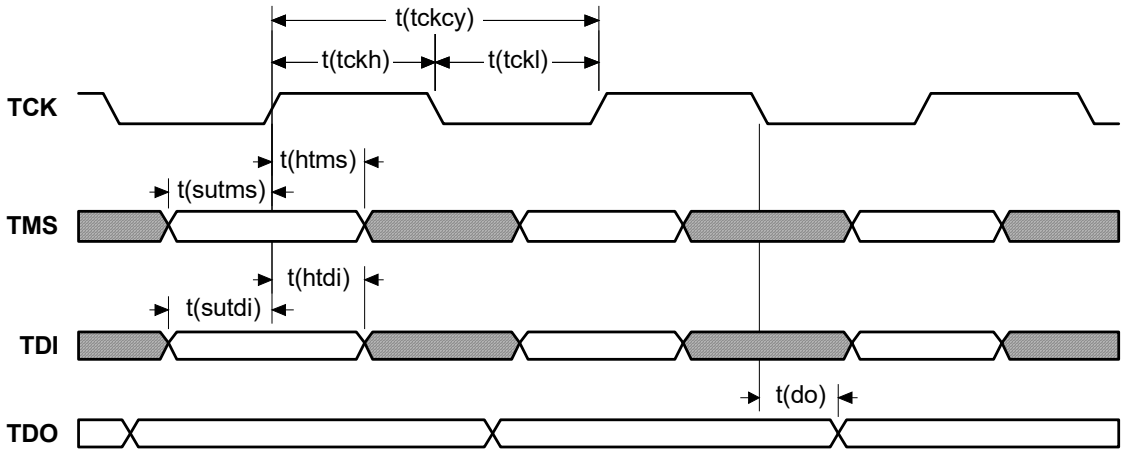


Figure 3-21 JTAG interface timing diagram

Table 3-49 JTAG interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period		50	–	–	ns
t(tckh)	TCK pulse width high		20	–	–	ns
t(tckl)	TCK pulse width low		20	–	–	ns
t(sutms)	TMS input setup time		5	–	–	ns
t(htms)	TMS input hold time		20	–	–	ns
t(sutdi)	TDI input setup time		5	–	–	ns

Table 3-49 JTAG interface timing characteristics (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(htdi)	TDI input hold time		20	–	–	ns
t(do)	TDO data-output delay		–	–	15	ns

3.12.5 Single wire debug (SWD)

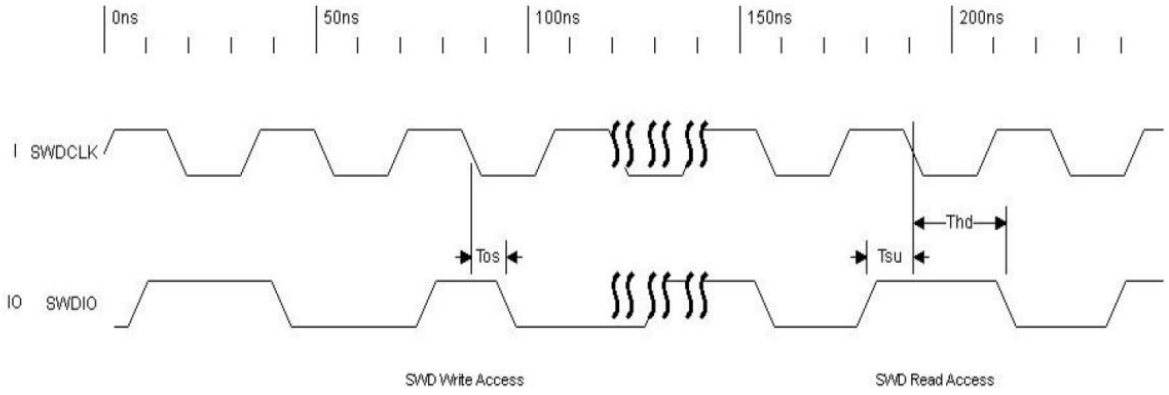


Figure 3-22 SWD write and read AC timing diagram

Table 3-50 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to falling edge of SWDCLK	0	17.5	ns
T_{su}	Input setup time between SWDIO and rising edge of SWDCLK	4	--	ns
T_{hd}	Input hold time between SWDIO and rising edge of SWDCLK	1	--	ns

3.13 RF and PM interfaces

The RF and PM interfaces supported by the APQ8064E are listed in Table 2-7. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

4 Mechanical information

Simplified mechanical information for the APQ8064E is presented in this chapter, including physical dimensions, visible markings, ordering information, moisture-sensitivity level, and thermal characteristics.

4.1 Device physical dimensions

4.1.1 23 × 23 package

The APQ8064E is available in a 784 pin flip chip ball grid array (FCBGA+HS)* package with body dimensions of 23 mm × 23 mm and maximum height of 2.57 mm. This package includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package and by the ball pattern when viewed from below.

NOTE Length, width, height and co-planarity are designated as special characteristics.

4.2 Part marking

4.2.1 Specification-compliant devices

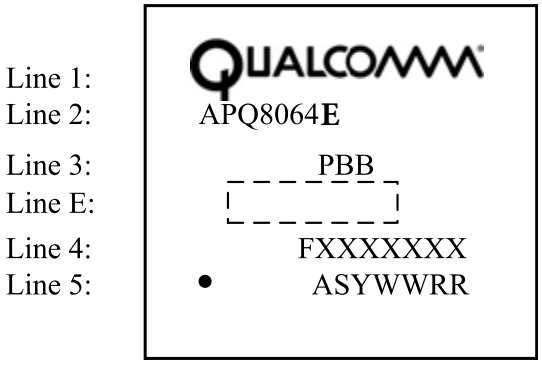


Figure 4-1 APQ8064E marking (top view, not to scale)

Table 4-1 APQ8064E marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	APQ8064E	QTI product name
3	PBB	P = product configuration code (see Table 4-2) BB = feature code ■ BB = VV
E	Blank or random	Additional content as necessary
4	FXXXXXXX	F = supply source code ■ F = A (TSMC) XXXXXXX = traceability number
5	ASYWWRR	A = assembly site code ■ APQ8064E package □ A = E (for ASE-KH) S = traceability number Y = single-digit year WW = work week (based on calendar year) RR = product revision (see Table 4-2)
Additional lines can appear on the part marking for some samples; this is manufacturing information that is only relevant to QTI and QTI suppliers.		

NOTE For complete marking definitions of all APQ8064E variants and revisions, refer to the *APQ8064 Device Revision Guide* (LM80-P0598-X).

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Figure 4-2.

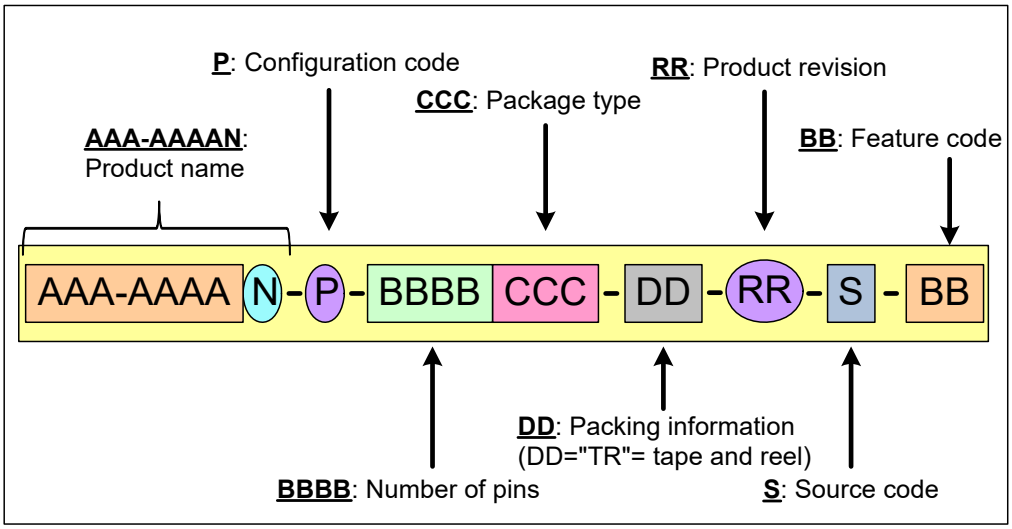


Figure 4-2 Device identification code

The product revision code (RR) reflects only die revisions. A source configuration code (S) has been added to reflect all qualified sourcing combinations (that is, multiple F codes).

An example for the APQ8064E can be as follows: APQ-8064E-01-784FCBGA+HS-TR-00-0.

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code/ordering information details

Product config code (*P*)	Product revision (*RR*)	Year/ work week (YWW)	Hardware revision number	Sample type	Hardware version	Comments
1	00	All	209600E1	ES1	v2.0.1 1.5 GHz	DDR3, 23 × 23 package, with HDCP, metal HS
1	01	< 538	309600E1	ES2	v3.0 1.5 GHz	DDR3, 23 × 23 package, with HDCP, metal HS
1	01	≥ 538	309600E1	CS	v3.0 1.5 GHz	DDR3, 23 × 23 package, with HDCP, metal HS

Table 4-3 Source configuration code

S value	Die	F = A
0	Digital	TSMC

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-4.

Table 4-4 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	≤ 30°C / 60% RH

The latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification are followed. The APQ8064E is classified as MSL3; the qualification temperature was 260ºC +0/-5°C. Do not confuse this qualification temperature with the peak temperature in the recommended solder reflow profile (see Section 5.2.2 for details).

4.5 Package loading during heat sink attachment

Heat sink attachment requires that a compressive load be applied to the package. Apply heat sinks in a manner to ensure uniform compressive loading across the lid of the package; avoid point loading. We recommend the following load specifications for 784 FCBGA+HS packages:

- < 153 N during heat sink attachment
- < 78 N under static loading

The specifications above have been determined through limited compressive testing of FCBGA+HS packages at 125°C up to 2000 hours. Packages were mounted to PCBs and uniformly compressed with loads up to 385 N. It was determined that the above loading specifications were within safe working limits to ensure negligible solder ball collapse and BGA shorting risk.

5 PCB mounting guidelines

5.1 RoHS compliance

The APQ8064E is externally lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC305 composition. Lead-free (or Pb-free) semiconductor products are defined as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

5.2 SMT parameters

This section describes QTI board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

5.2.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based on QTI internal characterizations.

Characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production is recommended. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability
- Keep the solderable area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array
- Avoid large solder mask openings over ground planes
- Traces for external routing are recommended to be less than or equal to half the pad diameter to ensure consistent solder joint shapes

One key parameter to be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). Square apertures are recommended for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness. Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil; otherwise, paste deposits can bridge.

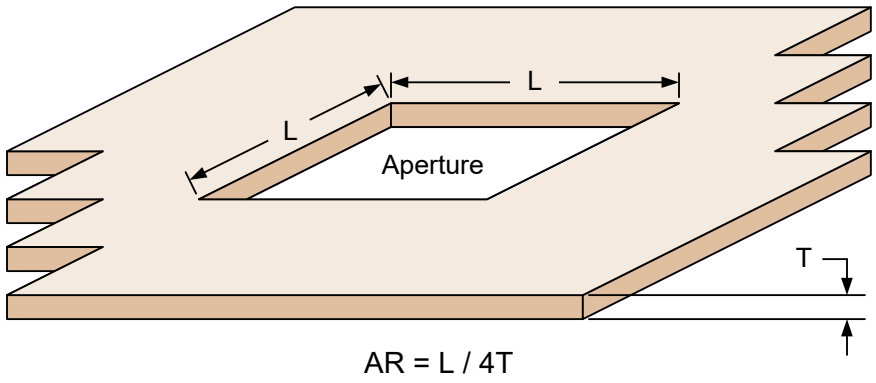


Figure 5-1 Area ratio (AR)

5.2.2 Reflow profile

Reflow profile conditions typically used for lead-free systems are listed in Table 5-1 and are shown in Figure 5-2.

Table 5-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C (minimum). Do not confuse this temperature with the peak temperature reached during MSL testing, as described in Section 5.2.3.

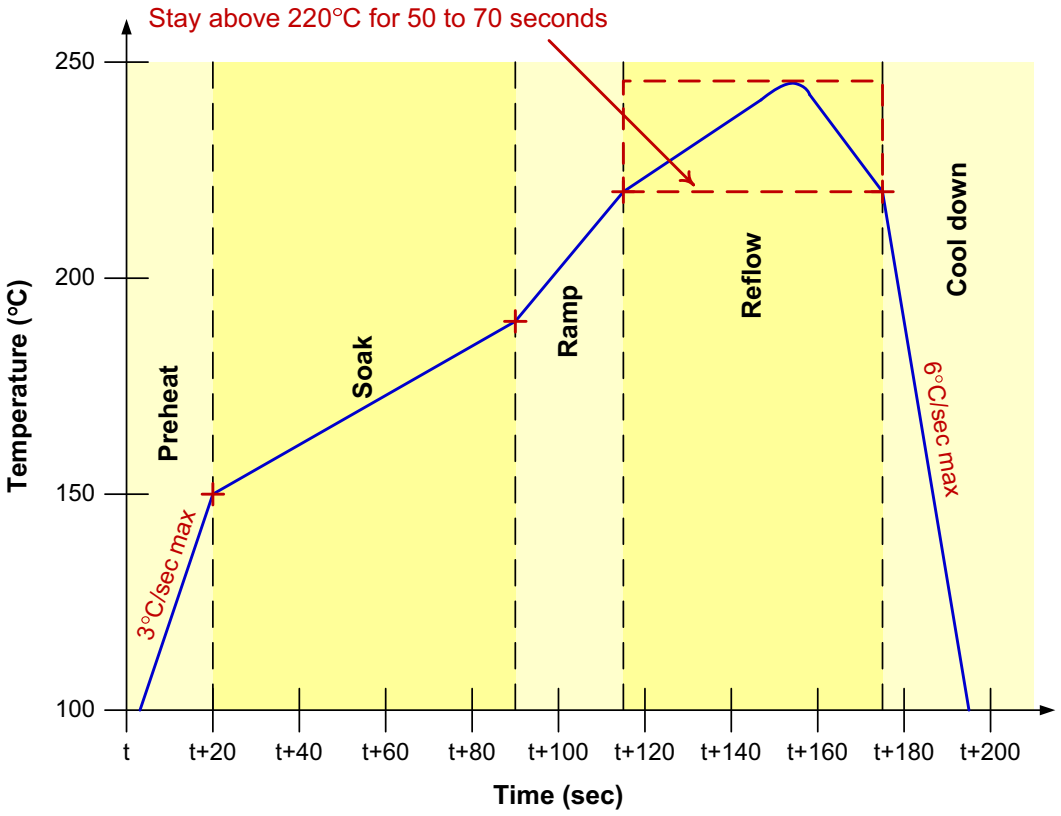


Figure 5-2 Typical SMT reflow profile

5.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three places in this document; and without explanation those temperatures can appear to conflict. The three places are listed here, along with an explanation of the stated value and its meaning in that section's context.

1. Section 4.4 – *Device moisture-sensitivity level*

   APQ8064E devices are classified as MSL3 at 260°C +0/-5°C. The temperature (255°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained in #2 below.

2. Section 5.2.2 – *Reflow profile*

   During a production board's reflow process, the temperature seen by the package must be controlled. Obviously the temperature must be high enough to melt the solder and provide reliable connections, but it must not go so high that the device might be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

3. Section 7.1 – *Reliability qualification summary*

One of the tests conducted for device qualification is the moisture resistance test. QTI follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5°C (255°C to 260°C).

5.2.4 SMT process verification

Verification of the SMT process is recommended prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow-profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

5.3 Board-level reliability

Characterization tests have been conducted to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing - optional (JESD22-B113)

5.4 High-temperature warpage

High temperature warpage is measured using a shadow moire system.

6 Carrier, storage, & handling information

6.1 Carrier

6.1.1 Tape and reel information

All carrier tape systems conform to EIA-481 standards.

A simplified sketch of the APQ8064E 23 × 23 tape carrier is shown in Figure 6-1, along with the proper part orientation, maximum number of devices per reel, and key dimensions. Tape and reel details for the APQ8064E are as follows:

- Reel diameter: 330 mm
- Hub size: 178 mm
- Tape width: 44 mm
- Tape pocket pitch: 32 mm
- Feed: Dual
- Units per reel: 500

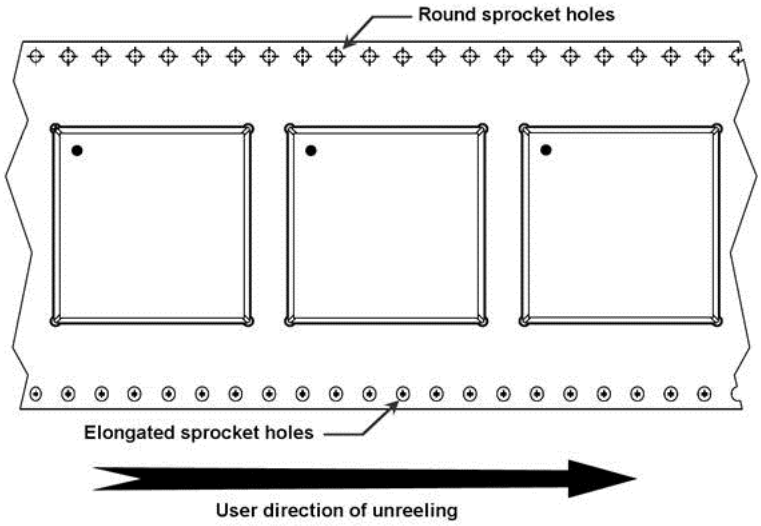


Figure 6-1 Carrier tape drawing with part orientation

6.1.2 Matrix tray information

Table 6-1 Matrix tray approved sources of supply

Tray configuration		Key dimensions (mm)	
Supplier:	ITW Camtex	M	16.95
MPN:	1047-18	M1	17.25
Drawing (rev):	4-1047-18 (A)	M2	25.50
Material:	MPPO	M3	25.50
Units per tray:	5 × 12 (60)		
Standard bundle qty:	300 (5 trays)		
Qualification status:	**Qualified**		

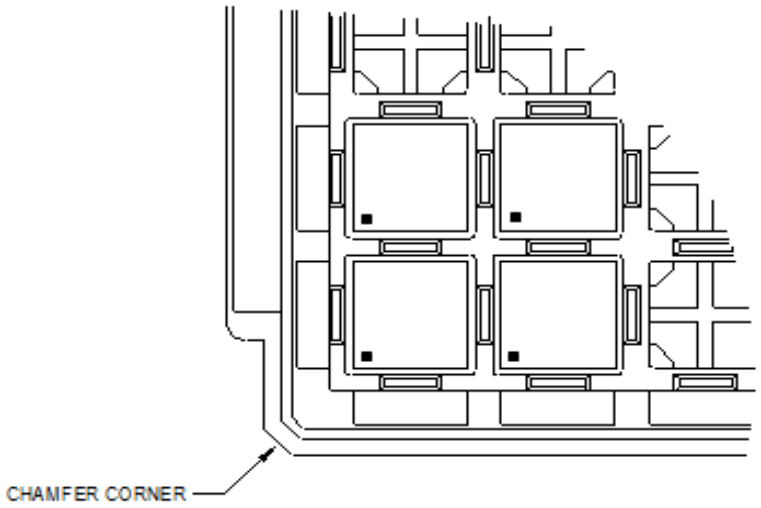


Figure 6-2 Matrix tray part orientation

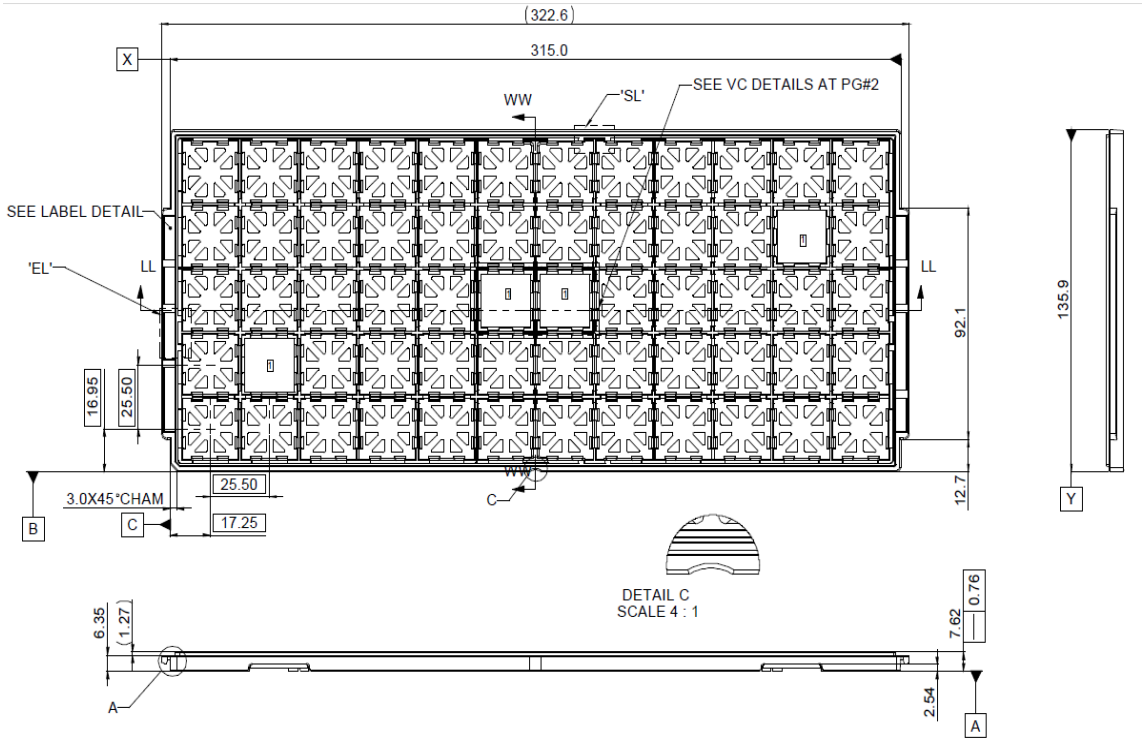


Figure 6-3 Matrix tray drawing

6.2 Storage

6.2.1 Bagged storage conditions

APQ8064E devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags between a temperature and humidity range of 15°C to 40°C, < 90% R.H.

6.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

6.2.3 Storage after assembly into customer's product

APQ8064E devices have been qualified through HTS test at 150°C 500 hrs (or more); refer to Chapter 7. QTI does not conduct storage at -40°C, however QTI has qualified devices through 500 or more temperature cycles between -55°C and +125°C. This does provide reasonable indication that QTI parts are not damaged by exposure to -40°C. In addition, QTI characterizes for operation at -40°C.

However, there are factors other than temperature that affect the assembled product, including humidity, contaminants/corrosive residues from the assembly operations, and assembly items that can outgas chemicals. Therefore, it is customary that the users create and conduct tests for their assemblies that cover the range and duration of the environmental conditions.

Additional information regarding storage can be found in JEDEC JEP 150, J-STD-033, JEP 122.

6.3 Handling

Tape handling was described in Section 6.1.1. Other (IC-specific) handling guidelines are presented in the following sections.

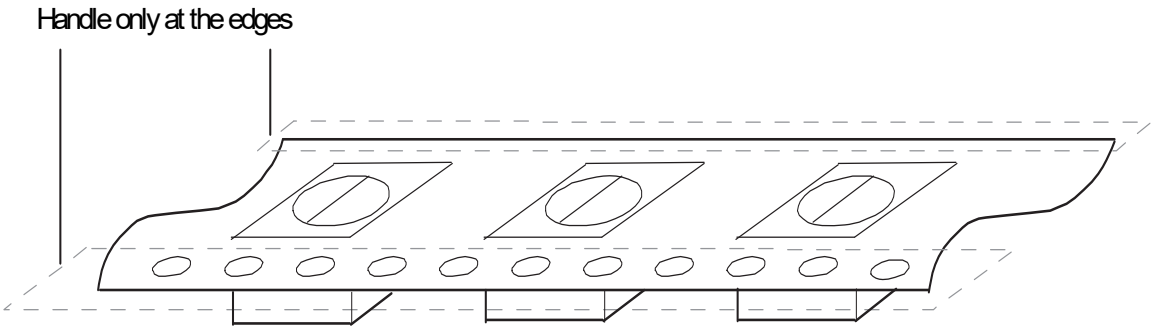


Figure 6-4 Tape handling

6.3.1 Baking

It is **not necessary** to bake the APQ8064E if the conditions specified in Section 6.2.1 and/or Section 6.2.2 have **not been exceeded**.

It is **necessary** to bake the APQ8064E if the humidity indicator card inside the moisture barrier bag indicates a need to do so. The baking conditions are specified on the moisture-sensitive caution label attached to each bag.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Do NOT bake devices in tape and reel carriers at ANY temperature.

6.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage can result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment.*

See Section 7.1 for the ESD ratings.

7 Part reliability

7.1 Reliability qualification summary

Table 7-1 lists the reliability qualification details.

Table 7-1 AEC-Q100 qualification plan and results summary

Stress test	ABV	Test number	Test method	Test conditions/pre- and post-ATE (identify temperature, RH, and bias)	Requirements		Results fails / total S.S	Comments
					S.S per lot	No. of lots		
Test group A: accelerated environment stress tests								
Preconditioning	PC	A1	JEDEC-J-STD-020, JESD22-A113	MSL 3, 3x reflow (pre- and post-ATE at R)	77	3	0F/231	Qualification lot IDs T6B429, T6B765, and T6B766
Preconditioning + bias HAST	BHAST	A2	JEDEC-JESD22-A110	130°C/85% RH for 96 hours (pre- and post-ATE at R and H)	77	3	0F/231	Qualification lot IDs T6B428, T6B429, and T6B764
Preconditioning + unbiased HAST	UHAST	A3	JEDEC-JESD22-A118	130°C/85% RH for 96 hours (pre- and post-ATE at R)	77	3	0F/231	Qualification lot IDs T6B429, T6B765, and T6B766
Preconditioning + temperature cycle	TC	A4	JEDEC-JESD22-A104	Ta = -55°C to +125°C for 500 cycles (pre- and post-ATE at R and H)	77	3	0F/231	Qualification lot IDs T6B429, T6B765, and T6B766. Passes extended stress readpoint to TC 1000 cycles.
Preconditioning + power temperature cycling	PTC	A5	JEDEC JESD22-A105	Ta = -40°C to +105°C for 1000 cycles (pre- and post-ATE at R and H)	45	1	0F/45	Qualification lot ID T6B429
High temperature storage life	HTSL	A6	JEDEC-JESD22-A103	Ta = +150°C for 500 hours (pre- and post-ATE at R and H)	45	1	0F/45	Qualification lot ID T6B429. Passes extended stress readpoint to HTSL 1000 hours.
Test group B: accelerated lifetime simulation tests								
High temperature operating life	HTOL	B1	JEDEC-JESD22-A108	Ta ≥ 85°C for 1000 hours (pre- and post-ATE at R, C, and H)	77	3	0F/231	Qualification lot IDs T6B428, T6B429, and T6B764. The drift analysis performed from T0 to T1000 hours. All shifts within acceptable limits.

Table 7-1 AEC-Q100 qualification plan and results summary

Stress test	ABV	Test number	Test method	Test conditions/pre- and post-ATE (identify temperature, RH, and bias)	Requirements		Results fails / total S.S	Comments
					S.S per lot	No. of lots		
Early life failure rate	ELFR	B2	AEC Q100-008	Ta = 85°C for 48 hours (pre- and post-ATE at R and H)	800	3	0F/2400	Qualification lot IDs T6B765, FT6C446, and FT6C447
NVM endurance, data retention, and operational life	EDR	B3	–	–	–	–	–	No NVM memory on device
Test group C: package assembly integrity tests								
Wire bond shear	WBS	C1	–	–	–	–	–	Not applicable, not a wirebonded package
Wire bond pull strength	WBPS	C2	–	–	–	–	–	Not applicable, not a wirebonded package
Solderability	S	C3	–	–	–	–	–	Not a leadframe package
Physical dimensions	PD	C4	–	Package outline drawing	10	3	0F/30	CPK ≥ 1.67
Solder ball shear	SBS	C5	JESD22-B117	Five balls each from a minimum of 10 devices, ≥ 500 g/ball for pad opening 470 µm	10	3	0F/50	CPK ≥ 1.67
Lead integrity	LI	C6	–	–	–	–	–	Not a leadframe package
Test group D: die fabrication reliability tests								
Electromigration	EM	D1	JP001A	DC lifetime > 11.4 yrs at 110°C, 0.1% cumulative failure	–	–	–	Pass
Time-dependent dielectric breakdown	TDDB	D2	JP001A	DC lifetime > 10 yrs at 125°C 0.1% cumulative failure at 1.1 × Vcc	–	–	–	Pass
Hot carrier injection	HCI	D3	JP001A	DC lifetime > 0.05 yrs at 125°C 0.1% cumulative failure at 1.1 × Vcc; DC lifetime > 0.2 yrs at 25°C 0.1% cumulative failure at 1.1 × Vcc	–	–	–	Pass
Negative bias temperature instability	NBTI	D4	JP001A	DC lifetime > 5 yrs at 125°C 0.1% cumulative failure at 1.1 × Vcc AC to DC factor of 2x	–	–	–	Pass
Stress migration	SM	D5	JP001A	No failure at 200°C, 500-hr bake	–	–	–	Pass

Table 7-1 AEC-Q100 qualification plan and results summary

Stress test	ABV	Test number	Test method	Test conditions/pre- and post-ATE (identify temperature, RH, and bias)	Requirements		Results fails / total S.S	Comments
					S.S per lot	No. of lots		
Test group E: electrical verification tests								
Pre- and post-stress electrical test	TEST	E1	–	–	–	–	–	Per column H
ESD: human body model	HBM	E2	AEC-Q100-002	Pass target ±1 kV with margin (pre- and post-ATE at R and H)	3	1	0F/3	Qualification lot ID T6B429. Passing ESD HBM level +1750 V/-2000 V.
ESD: charged device model	CDM	E3	AEC-Q100-011	Pass target ±250 V with margin (pre- and post-ATE at R and H)	3	1	0F/3	Qualification lot ID T6B429. Passing ESD CDM level +500 V/-450 V, ±750 V corner pins.
Latch-up	LU	E4	AEC-Q100-004	Ta = 85°C, Current injection ±100 mA, over voltage test at 1.5x VDD (pre- and post-ATE at R and H)	6	1	0F/6	Qualification lot ID T6B429
Electrical distribution	ED	E5	–	–	–	–	–	Available for review
Fault grading	FG	E6	–	–	–	–	–	Available for review
Characterization	CHAR	E7	–	–	–	–	–	Available for review
Electromagnetic compatibility	EMC	E9	–	–	–	–	–	Not performed. System level test.
Short circuit characterization	SC	E10	–	–	–	–	–	Not applicable. Not > 12 V or a power device.
Soft error rate	SER	E11	–	–	–	–	–	Available for review
Test group F - defect screening tests								
Process average test	PAT	F1	–	–	–	–	–	Available for review
Statistical bin/yield analysis	SBA	F2	–	–	–	–	–	Available for review
Notes:								

7.2 Qualification sample description

Tested per AEC-Q100 Grade 3

Table 7-2 APQ8064E device characteristics

Device	Specification
Device name	APQ8064E
Package type	784 FCBGA + HS
Package body size	23 mm × 23 mm
Ball count:	784
Ball composition	SAC305
Fab process	28 nm
Fab site	TSMC
Assembly site	ASE-KH
Solder ball pitch	0.8 mm

Exhibit 1

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