LOW-NOISE, VERY LOW DRIFT, PRECISION VOLTAGE REFERENCE

Check for Samples: REF5020-Q1, REF5025-Q1, REF5030-Q1, REF5040-Q1, REF5045-Q1, REF5050-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Low Temperature Drift**
  - **High Grade: 3 ppm/°C (max)**
  - **Standard Grade: 8 ppm/°C (max)**
- **High Accuracy**
  - **High Grade: 0.05% (max)**
  - **Standard Grade: 0.1% (max)**
- **Low Noise: 3 µV_{PP}/V**
- **EXCELLENT LONG-TERM STABILITY:**
  - **5ppm/1000hr (typ) after 1000 hours**
- **High Output Current: ±10 mA**
- **Temperature Range: –40°C to 125°C**

APPLICATIONS

- **16-Bit Data Acquisition Systems**
- **ATE Equipment**
- **Industrial Process Control**
- **Medical Instrumentation**
- **Optical Control Systems**
- **Precision Instrumentation**

DESCRIPTION

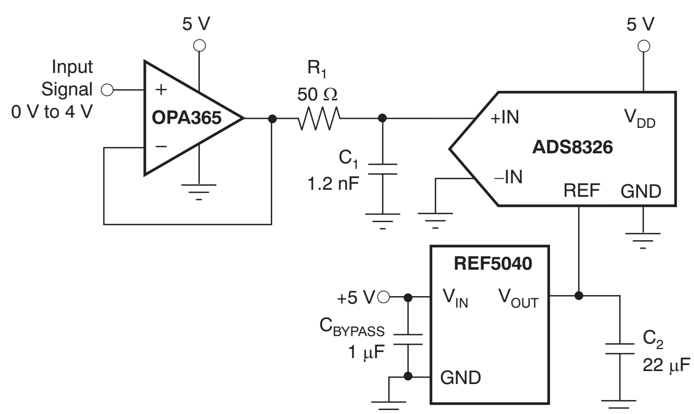
The REF50xx is a family of low-noise, low-drift, very high precision voltage references. These references are capable of both sinking and sourcing, and are very robust with regard to line and load changes.

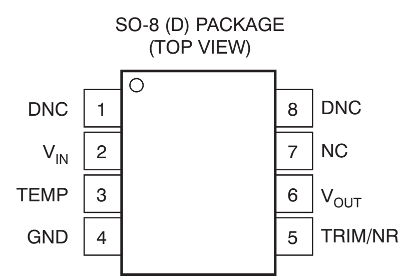
Excellent temperature drift (3 ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features combined with very low noise make the REF50xx family ideal for use in high-precision data acquisition systems.

Each reference voltage is available in both standard- and high-grade versions. They are offered in SO-8 packages and are specified from –40°C to 125°C.

REF50xx Family

MODEL	OUTPUT VOLTAGE
REF5020	2.048 V
REF5025	2.5 V
REF5030	3 V
REF5040	4.096 V
REF5045	4.5 V
REF5050	5 V





DNC = Do not connect
NC = No internal connection

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1) (2)

PRODUCT	OUTPUT VOLTAGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
STANDARD GRADE (8 ppm, 0.1%)				
REF5020A	2.048 V	SO-8	D	RFQ5020
REF5025A	2.5 V	SO-8	D	RFQ5025
REF5030A	3.0 V	SO-8	D	RFQ5030
REF5040A	4.096 V	SO-8	D	RFQ5040
REF5045A	4.5 V	SO-8	D	RFQ5045
REF5050A	5.0 V	SO-8	D	RFQ5050
HIGH GRADE (3 ppm, 0.05%)				
REF5020I	2.048 V	SO-8	D	RFQ5020
REF5025I	2.5 V	SO-8	D	PREVIEW
REF5030I	3.0 V	SO-8	D	PREVIEW
REF5040I	4.096 V	SO-8	D	PREVIEW
REF5045I	4.5 V	SO-8	D	PREVIEW
REF5050I	5.0 V	SO-8	D	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	REF50xx	UNIT
Input voltage	+18	V
Output short-circuit	30	mA
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature (T_J max)	+150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ESD RATINGS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER			VALUE	UNIT
ESD	Human Body Model (HBM)	REF5020AQDRQ1	500	V
		REF5030AQDRQ1	1000	
		REF5040AQDRQ1	500	
		REF5045AQDRQ1	1000	
		REF5050AQDRQ1	500	
	Machine Model (MM)		200	V
	Charged-Device Model		1000	V

ELECTRICAL CHARACTERISTICS: PER DEVICE

Boldface limits apply over the specified temperature range, T_A **= –40°C to 125°C.**
T_A = 25°C, I_{LOAD} = 0, C_L = 1 μF, V_{IN} = (V_{OUT} + 0.2 V) to 18 V (unless otherwise noted).

PARAMETER			CONDITIONS	PER DEVICE MIN	TYP	MAX	UNIT
REF5020 (V_{OUT} = 2.048 V)(1)							
OUTPUT VOLTAGE							
Output voltage		V_{OUT}	2.7 V < V_{IN} < 18 V		2.048		V
Initial accuracy:	High grade			–0.05		0.05	%
	Standard grade			–0.1		0.1	%
NOISE							
Output voltage noise			f = 0.1 Hz to 10 Hz		6		μV_{PP}
REF5025 (V_{OUT} = 2.5 V)							
OUTPUT VOLTAGE							
Output voltage		V_{OUT}			2.5		V
Initial accuracy:	High grade			–0.05		0.05	%
	Standard grade			–0.1		0.1	%
NOISE							
Output Voltage Noise			f = 0.1 Hz to 10 Hz		7.5		μV_{PP}
REF5030 (V_{OUT} = 3 V)							
OUTPUT VOLTAGE							
Output voltage		V_{OUT}			3.0		V
Initial accuracy:	High grade			–0.05		0.05	%
	Standard grade			–0.1		0.1	%
NOISE							
Output voltage noise			f = 0.1 Hz to 10 Hz		9		μV_{PP}
REF5040 (V_{OUT} = 4.096 V)							
OUTPUT VOLTAGE							
Output voltage		V_{OUT}			4.096		V
Initial accuracy:	High grade			–0.05		0.05	%
	Standard grade			–0.1		0.1	%
NOISE							
Output voltage noise			f = 0.1 Hz to 10 Hz		12		μV_{PP}
REF5045 (V_{OUT} = 4.5 V)							
OUTPUT VOLTAGE							
Output voltage		V_{OUT}			4.5		V
Initial accuracy:	High grade			–0.05		0.05	%
	Standard grade			–0.1		0.1	%
NOISE							
Output voltage noise			f = 0.1 Hz to 10 Hz		13.5		μV_{PP}
REF5050 (V_{OUT} = 5 V)							
OUTPUT VOLTAGE							
Output voltage		V_{OUT}			5.0		V
Initial accuracy:	High grade			–0.05		0.05	%
	Standard grade			–0.1		0.1	%
NOISE							
Output voltage noise			f = 0.1 Hz to 10 Hz		15		μV_{PP}

(1) For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

ELECTRICAL CHARACTERISTICS: ALL DEVICES

Boldface limits apply over the specified temperature range, T_A **= –40°C to 125°C.**
T_A = 25°C, I_{LOAD} = 0, C_L = 1 μF, V_{IN} = (V_{OUT} + 0.2 V) to 18 V (unless otherwise noted).

PARAMETER		CONDITIONS	REF50xx MIN	REF50xx TYP	REF50xx MAX	UNIT
OUTPUT VOLTAGE TEMPERATURE DRIFT						
Output voltage temperature drift	**dV_{OUT}/dT**					
High grade				**2.5**	**3**	**ppm/°C**
Standard grade				**3**	**8**	**ppm/°C**
LINE REGULATION						
Line regulation	dV_{OUT}/dV_{IN}					
REF5020[(1)] only		V_{IN} = 2.7 V to 18 V		0.1	1	ppm/V
All other devices		V_{IN} = V_{OUT} + 0.2 V		0.1	1	ppm/V
Over temperature				**0.2**	**1**	**ppm/V**
LOAD REGULATION						
Load regulation	dV_{OUT}/dI_{LOAD}	–10 mA < I_{LOAD} < +10 mA				
REF5020 Only		V_{IN} = 3 V		20	30	ppm/mA
All other devices		V_{IN} = V_{OUT} + 0.75 V		20	30	ppm/mA
Over temperature					**50**	**ppm/mA**
SHORT-CIRCUIT CURRENT						
Short-circuit current	I_{SC}	V_{OUT} = 0 V		25		mA
THERMAL HYSTERESIS [(2)]						
High-Grade	MSOP-8	Cycle 1		10		ppm
Standard-Grade	MSOP-8	Cycle 1		30		ppm
High-Grade	SO-8	Cycle 1		5		ppm
Standard-Grade	SO-8	Cycle 1		10		ppm
High-Grade	MSOP-8	Cycle 2		5		ppm
Standard-Grade	MSOP-8	Cycle 2		10		ppm
High-Grade	SO-8	Cycle 2		3		ppm
Standard-Grade	SO-8	Cycle 2		5		ppm
LONG-TERM STABILITY						
MSOP-8		0 to 1000 hours		50		ppm/1000 hr
MSOP-8		1000 to 2000 hours		5		ppm/1000 hr
SO-8		0 to 1000 hours		90		ppm/1000 hr
SO-8		1000 to 2000 hours		10		ppm/1000 hr
TEMP PIN						
Voltage output		At T_A = 25°C		575		mV
Temperature sensitivity				**2.64**		**mV/°C**
TURN-ON SETTLING TIME						
Turn-on settling time		To 0.1% with C_L = 1 μF		200		μs
POWER SUPPLY						
Supply voltage	V_S	See Note [(1)]	V_{OUT} + 0.2[(1)]		18	V
Quiescent current				0.8	1	mA
Over temperature					**1.2**	**mA**
TEMPERATURE RANGE						
Specified range			–40		125	°C
Operating range			–55		125	°C
Thermal resistance	θ_{JA}					
SO-8				150		°C/W

(1) For V_{OUT} ≤ 2.5 V, the minimal supply voltage is 2.7 V.
(2) The thermal hysteresis procedure is explained in more detail in the *Application Information* section.

TYPICAL CHARACTERISTICS

T_A = 25°C, I_{LOAD} = 0, V_S = V_{OUT} + 0.2 V (unless otherwise noted). For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

TEMPERATURE DRIFT (0°C to 85°C)

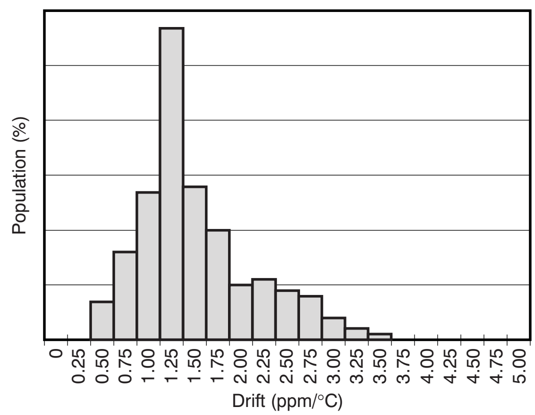


Figure 1.

TEMPERATURE DRIFT (–40°C to 125°C)

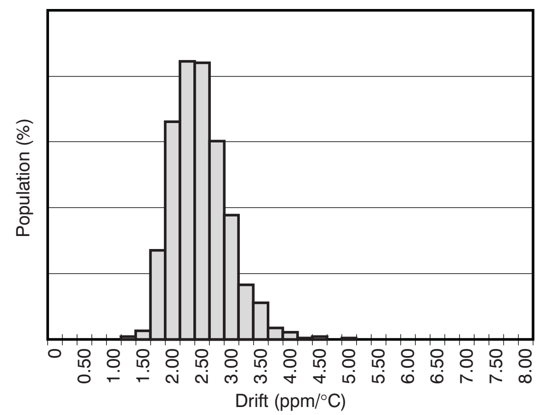


Figure 2.

OUTPUT VOLTAGE INITIAL ACCURACY

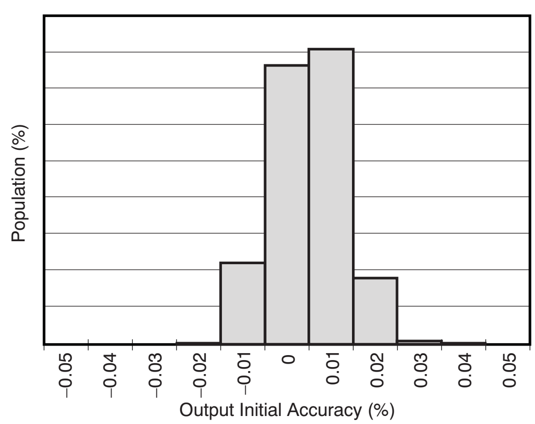


Figure 3.

OUTPUT VOLTAGE ACCURACY vs TEMPERATURE

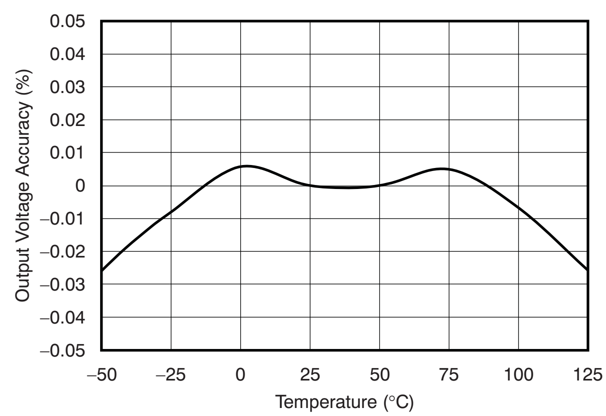


Figure 4.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

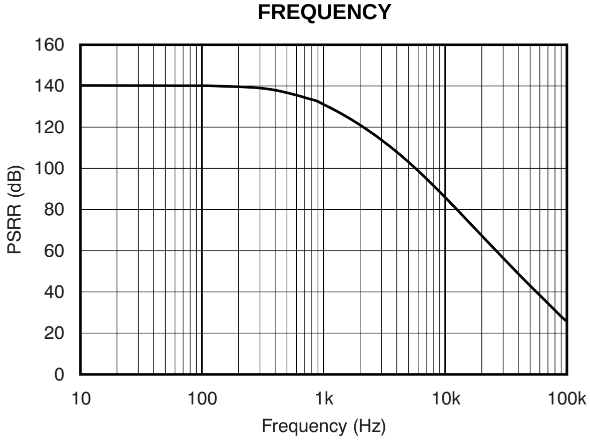


Figure 5.

DROPOUT VOLTAGE vs LOAD CURRENT

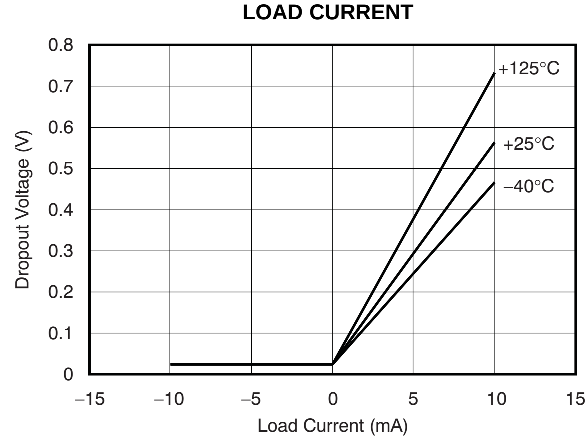


Figure 6.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, I_{LOAD} = 0, V_S = V_{OUT} + 0.2 V (unless otherwise noted). For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

REF5025 OUTPUT VOLTAGE vs LOAD CURRENT

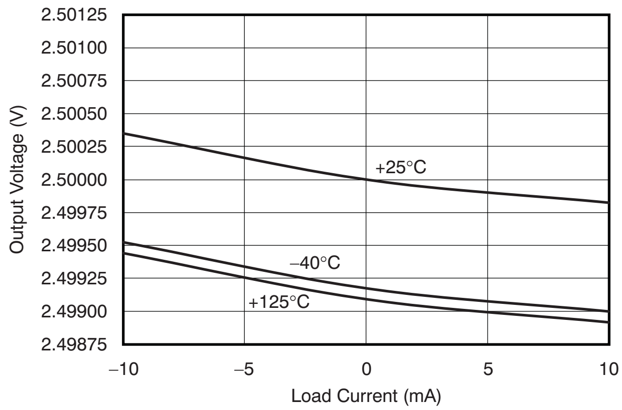


Figure 7.

TEMP PIN OUTPUT VOLTAGE vs TEMPERATURE

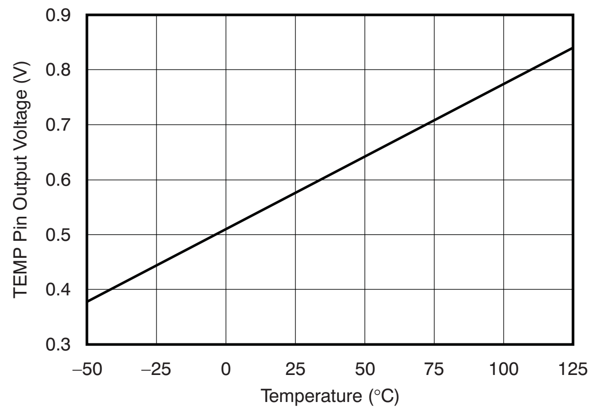


Figure 8.

QUIESCENT CURRENT vs TEMPERATURE

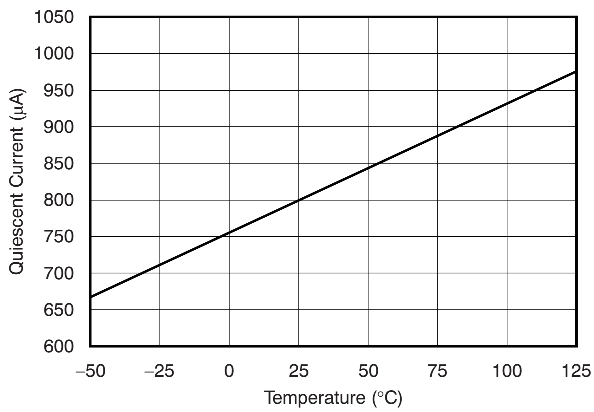


Figure 9.

QUIESCENT CURRENT vs INPUT VOLTAGE

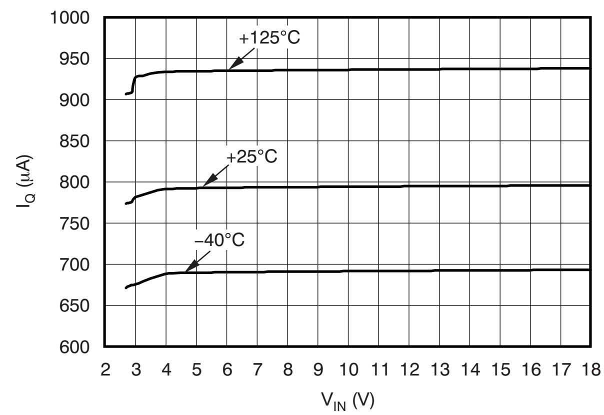


Figure 10.

LINE REGULATION vs TEMPERATURE

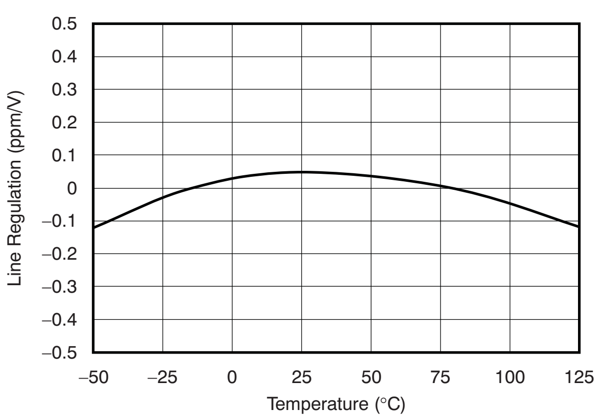


Figure 11.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

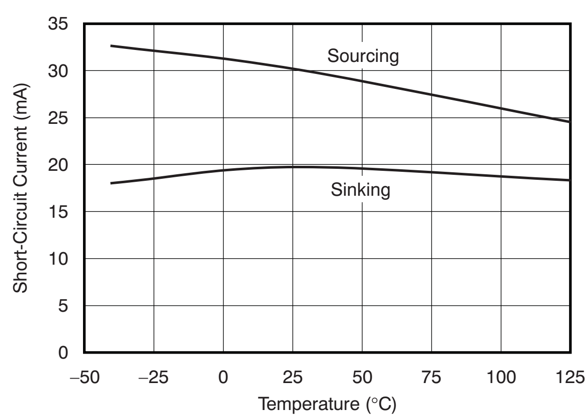


Figure 12.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, I_{LOAD} = 0, V_S = V_{OUT} + 0.2 V (unless otherwise noted). For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

NOISE

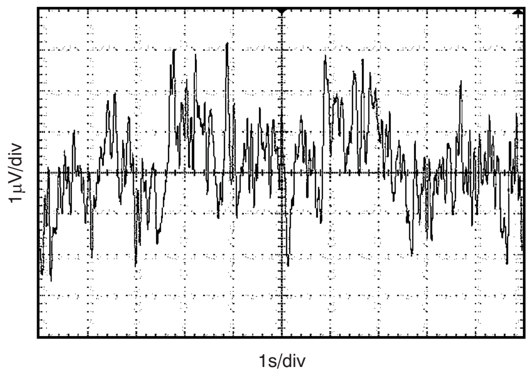


Figure 13.

STARTUP (REF5025, C_L = 1 μF)

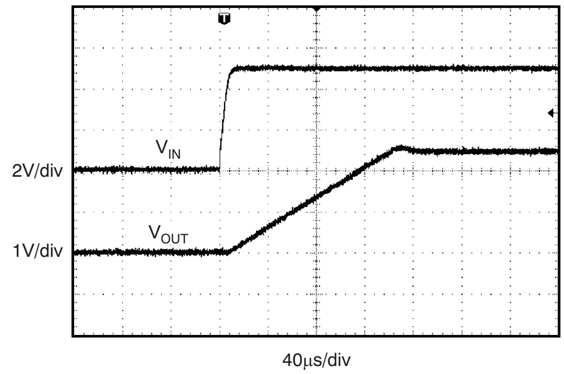


Figure 14.

STARTUP (REF5025, C_L = 10 μF)

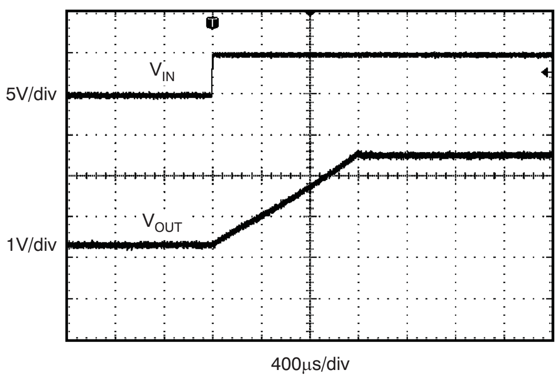


Figure 15.

LOAD TRANSIENT (C_L = 1 μF, I_{OUT} = 1 mA)

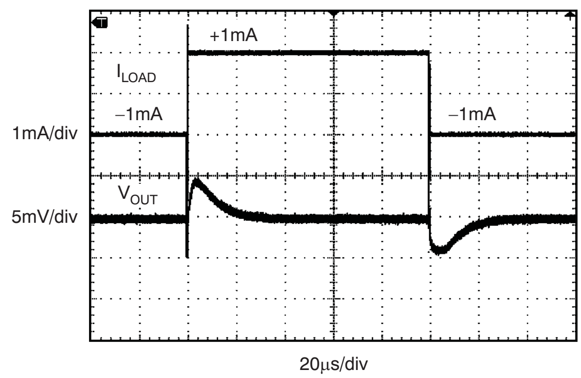


Figure 16.

LOAD TRANSIENT (C_L = 1 μF, I_{OUT} = 10 mA)

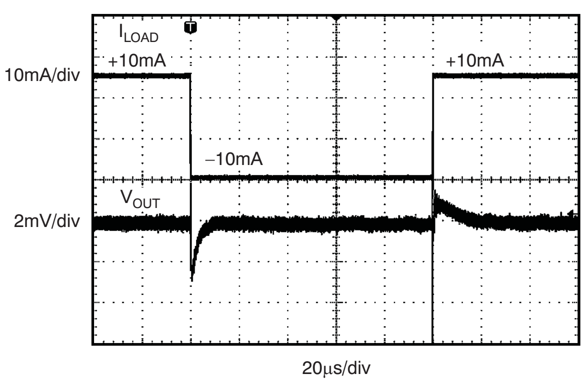


Figure 17.

LOAD TRANSIENT (C_L = 10 μF, I_{OUT} = 1 mA)

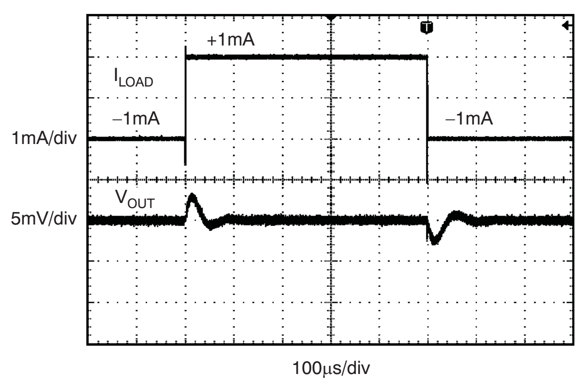


Figure 18.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, I_{LOAD} = 0, V_S = V_{OUT} + 0.2 V (unless otherwise noted). For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

LOAD TRANSIENT
(C_L = 10 μF, I_{OUT} = 10 mA)

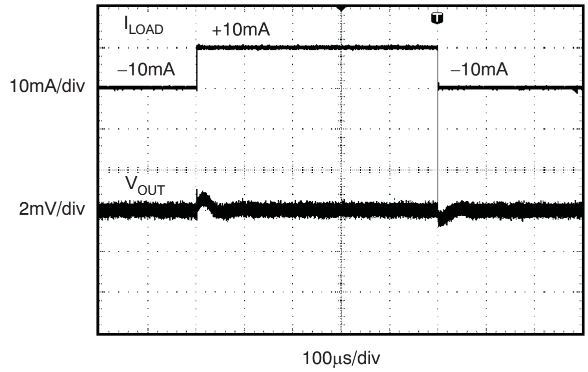


Figure 19.

LINE TRANSIENT
(C_L = 1 μF)

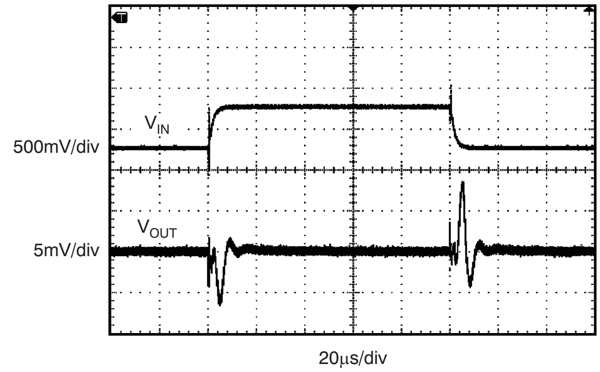


Figure 20.

LINE TRANSIENT
(C_L = 10 μF)

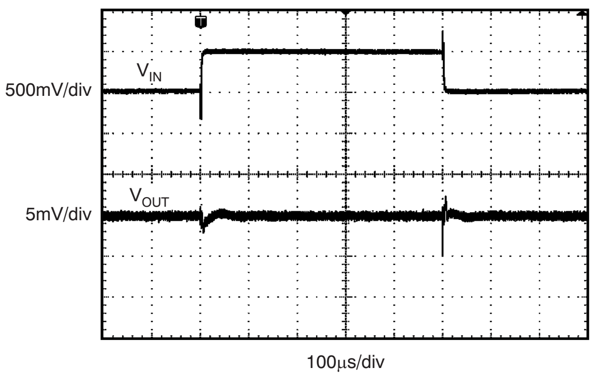


Figure 21.

REF50xx
LONG-TERM STABILITY (FIRST 1000 HOURS)

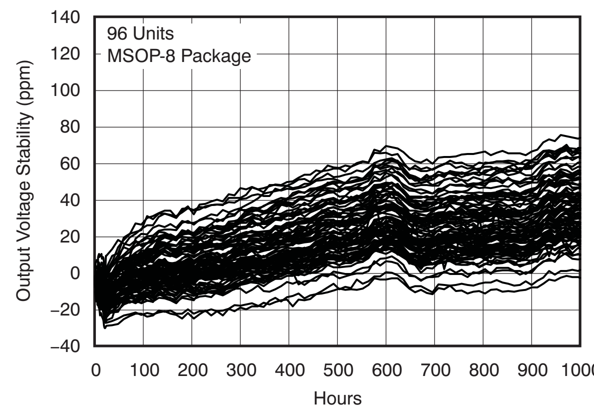


Figure 22.

REF50xx
LONG-TERM STABILITY (SECOND 1000 HOURS)

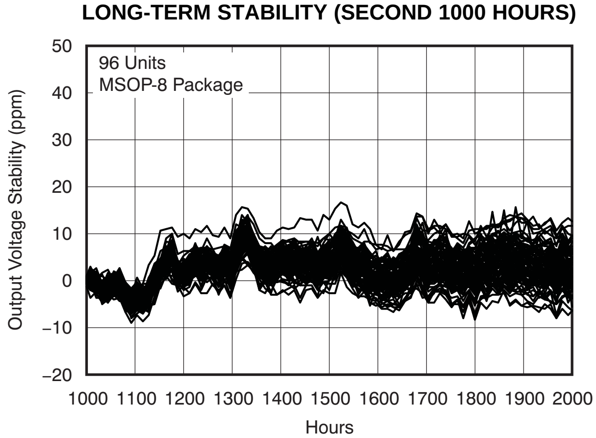


Figure 23.

REF50xx
LONG-TERM STABILITY (2000 HOURS)

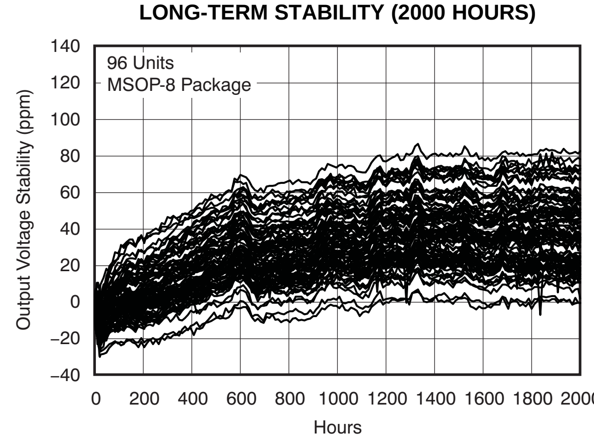


Figure 24.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, I_{LOAD} = 0, V_S = V_{OUT} + 0.2 V (unless otherwise noted). For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

REF50xx
LONG-TERM STABILITY (FIRST 1000 HOURS)

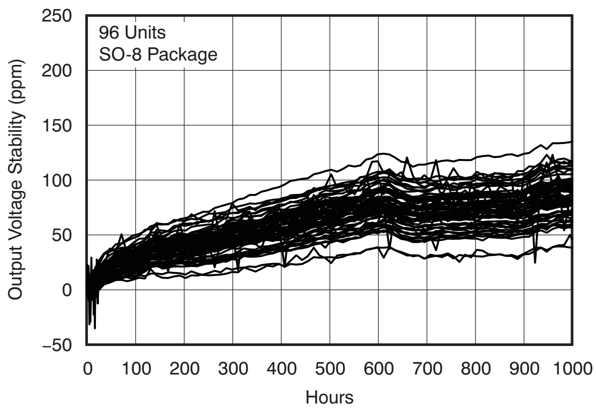


Figure 25.

REF50xx
LONG-TERM STABILITY (SECOND 1000 HOURS)

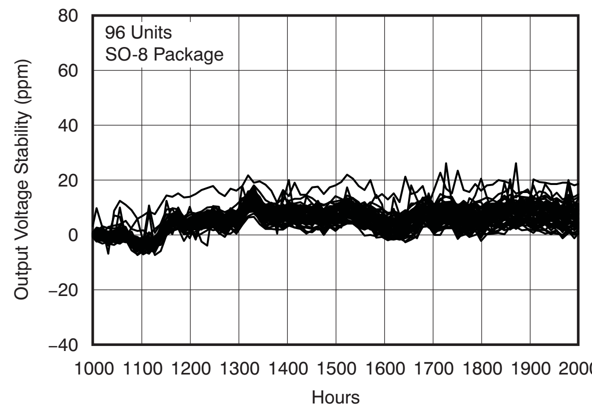


Figure 26.

REF50xx
LONG-TERM STABILITY (2000 HOURS)

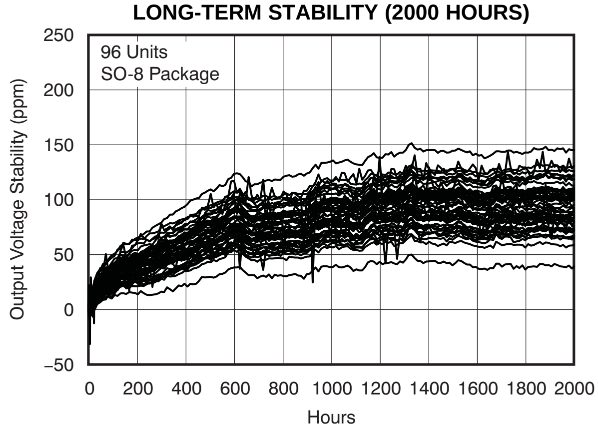


Figure 27.

APPLICATION INFORMATION

The REF50xx is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. Figure 28 shows a simplified block diagram of the REF50xx.

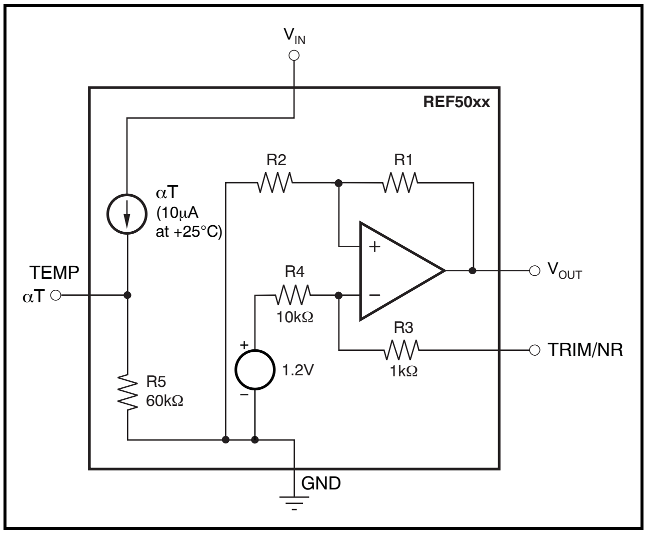


Figure 28. REF50xx Simplified Block Diagram

BASIC CONNECTIONS

Figure 29 shows the typical connections for the REF50xx. A supply bypass capacitor ranging between 1 μF to 10 μF is recommended. A 1-μF to 50-μF, low-ESR output capacitor (C_L) must be connected from V_{OUT} to GND. The ESR value should be less than or equal to 1.5 Ω. The ESR minimizes gain peaking of the internal 1.2-V reference and thus reduces noise at the V_{OUT} pin.

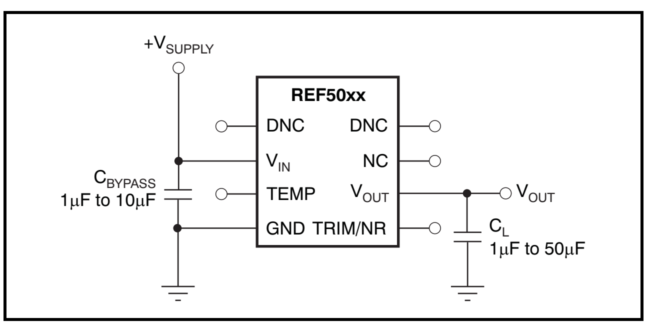


Figure 29. Basic Connections

SUPPLY VOLTAGE

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7 V, these references can be operated with a supply of 200 mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is shown in Figure 6 of the *Typical Characteristics*.

USING THE TRIM/NR PIN

The REF50xx provides a very accurate voltage output. However, V_{OUT} can be adjusted to reduce noise and shift the output voltage from the nominal value by configuring the trim and noise reduction pin (TRIM/NR, pin 5). The TRIM/NR pin provides a ±15-mV adjustment of the device bandgap, which produces a ±15-mV change on the V_{OUT} pin. Figure 30 shows a typical circuit using the TRIM/NR pin to adjust V_{OUT}. When using this technique, the temperature coefficients of the resistors can degrade the temperature drift at the output.

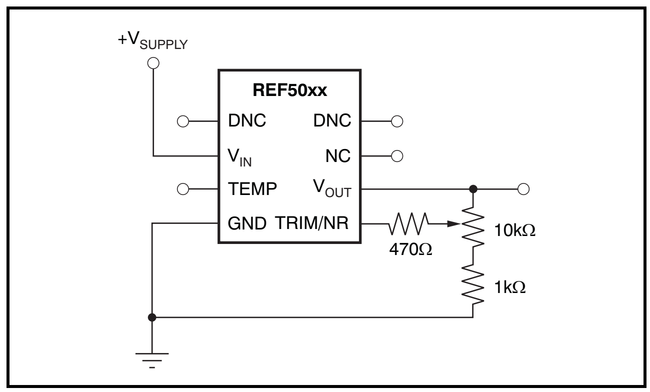


Figure 30. V_{OUT} Adjustment Using TRIM/NR Pin

The REF50xx allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (as Figure 31 illustrates) in combination with the internal 1-kΩ resistor creates a low-pass filter that lowers the overall noise measured on the V_{OUT} pin. A capacitance of 1 μF is suggested for a low-pass filter with a corner frequency of 14.5 Hz. Higher capacitance results in a lower cutoff frequency.

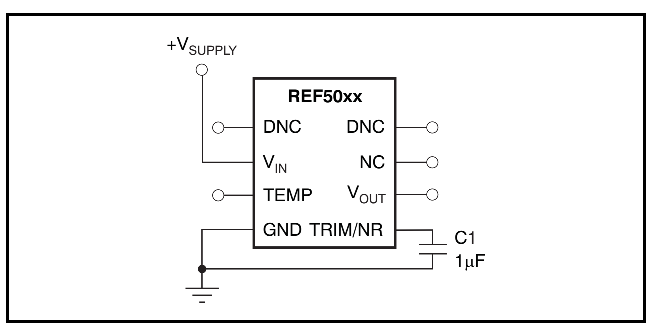


Figure 31. Noise Reduction Using TRIM/NR Pin

TEMPERATURE DRIFT

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temp Range}}\right) \times 10^6(\text{ppm}) \quad (1)$$

The REF50xx features a maximum drift coefficient of 3 ppm/°C for the high-grade version, and 8 ppm/°C for the standard-grade.

THERMAL HYSTERESIS

Thermal hysteresis for the REF50xx is defined as the change in output voltage after operating the device at +25°C, cycling the device through the specified temperature range, and returning to +25°C. It can be expressed as Equation 2:

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}}\right) \bullet 10^6(\text{ppm}) \quad (2)$$

Where:

V_{HYST} = thermal hysteresis (in units of ppm).

V_{NOM} = the specified output voltage.

V_{PRE} = output voltage measured at +25°C pretemperature cycling.

V_{POST} = output voltage measured after the device has been cycled from +25°C through the specified temperature range of –40°C to +125°C and returned to +25°C.

TEMPERATURE MONITORING

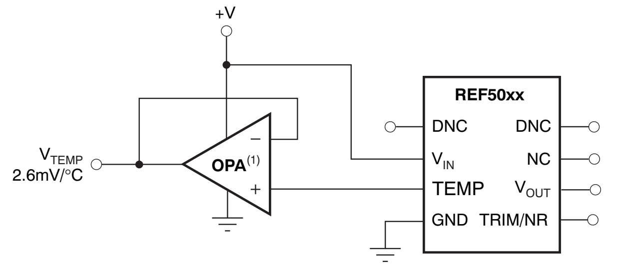
The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60-kΩ source impedance. As seen in Figure 8, the output voltage follows the nominal relationship:

$V_{TEMP\ PIN}$ = 509 mV + 2.64 × T(°C)

This pin indicates general chip temperature, accurate to approximately ±15°C. Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79-mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see Figure 28). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on V_{OUT} accuracy.

To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in Figure 32.



NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

Figure 32. Buffering the TEMP Pin Output

POWER DISSIPATION

The REF50xx family is specified to deliver current loads of ±10 mA over the specified input voltage range. The temperature of the device increases according to the equation:

$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Where:

T_J = Junction temperature (°C)

T_A = Ambient temperature (°C)

P_D = Power dissipated (W)

θ_{JA} = Junction-to-ambient thermal resistance (°C/W)

The REF50xx junction temperature must not exceed the absolute maximum rating of 150°C.

NOISE PERFORMANCE

Typical 0.1Hz to 10Hz voltage noise for each member of the REF50xx family is specified in the *Electrical Characteristics: Per Device* table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications such as data converters, refer to the series of *Analog Applications Journal* articles entitled, *How a Voltage Reference Affects ADC Performance*. This three-part series is available for download from the TI website under three literature numbers: SLYT331, SLYT339, and SLYT355 for Part I, Part II, and Part III, respectively.

APPLICATION CIRCUITS

NEGATIVE REFERENCE VOLTAGE

For applications requiring a negative and positive reference voltage, the REF50xx and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 33 shows the REF5025 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of R_1 and R_2.

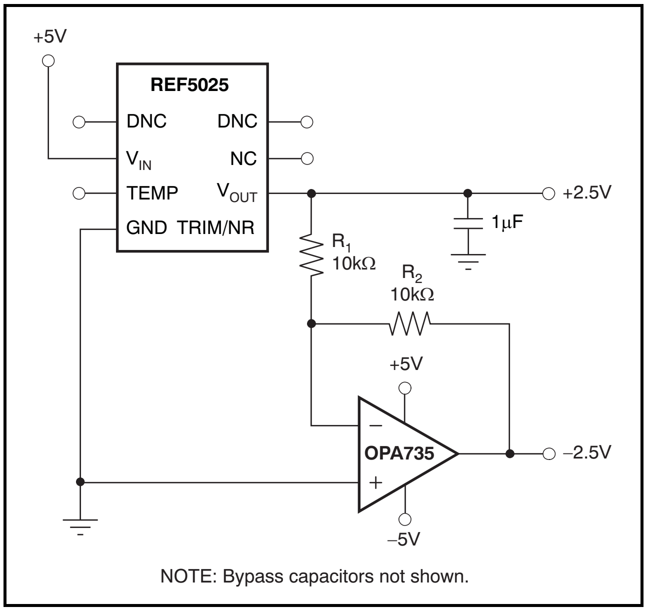


Figure 33. The REF5025 and OPA735 Create Positive and Negative Reference Voltages

DATA ACQUISITION

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 34 shows the REF5040 in a basic data acquisition system.

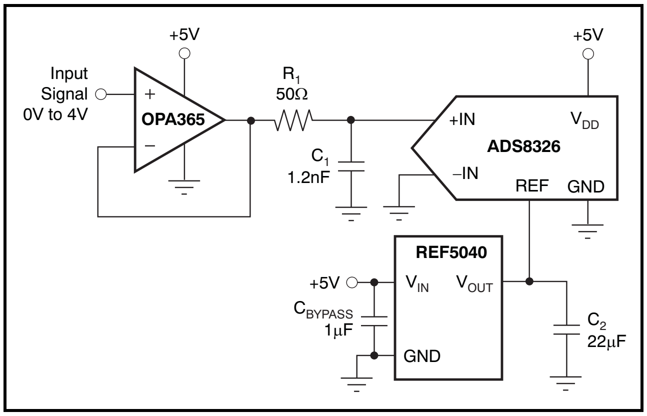


Figure 34. Basic Data Acquisition System

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2011) to Revision F **Page**

- Added REF5045A top-side marking 2
- Added REF5045AQDRQ1 HBM ESD rating of 1000 V 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
REF5020AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
REF5025AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
REF5030AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
REF5040AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
REF5045AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
REF5050AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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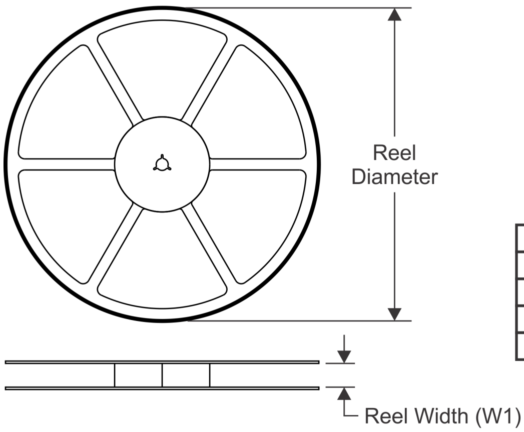
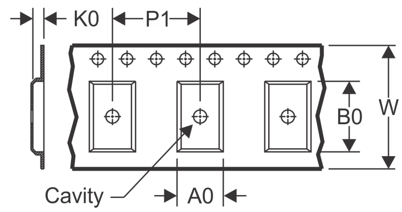
TAPE AND REEL INFORMATION

REEL DIMENSIONS

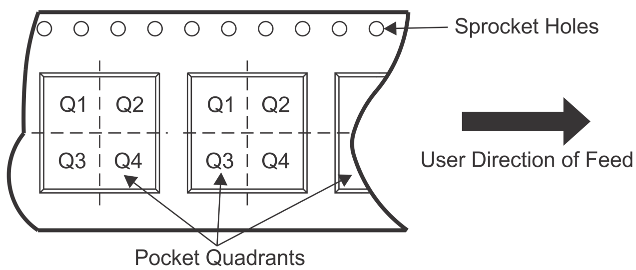


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

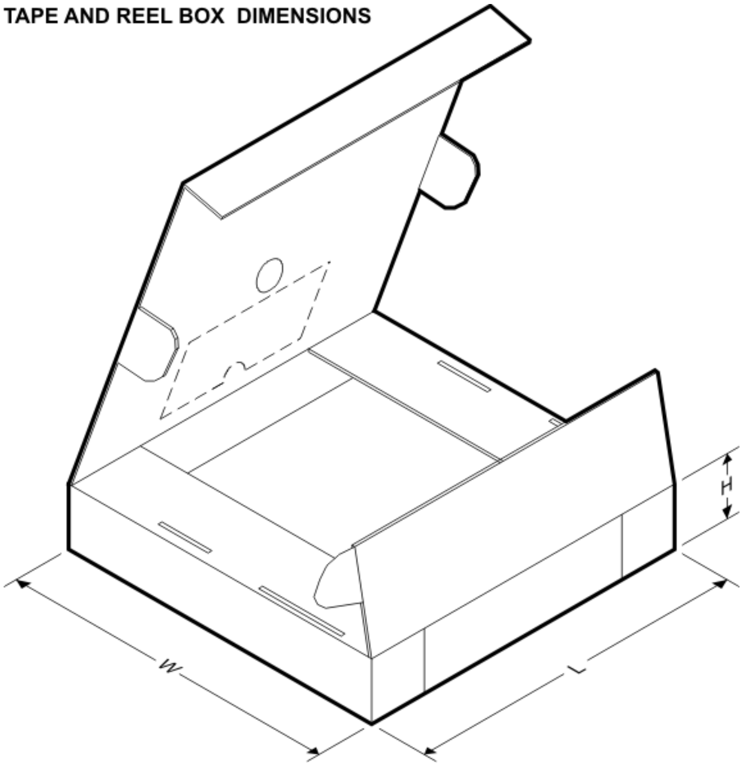
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5025AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

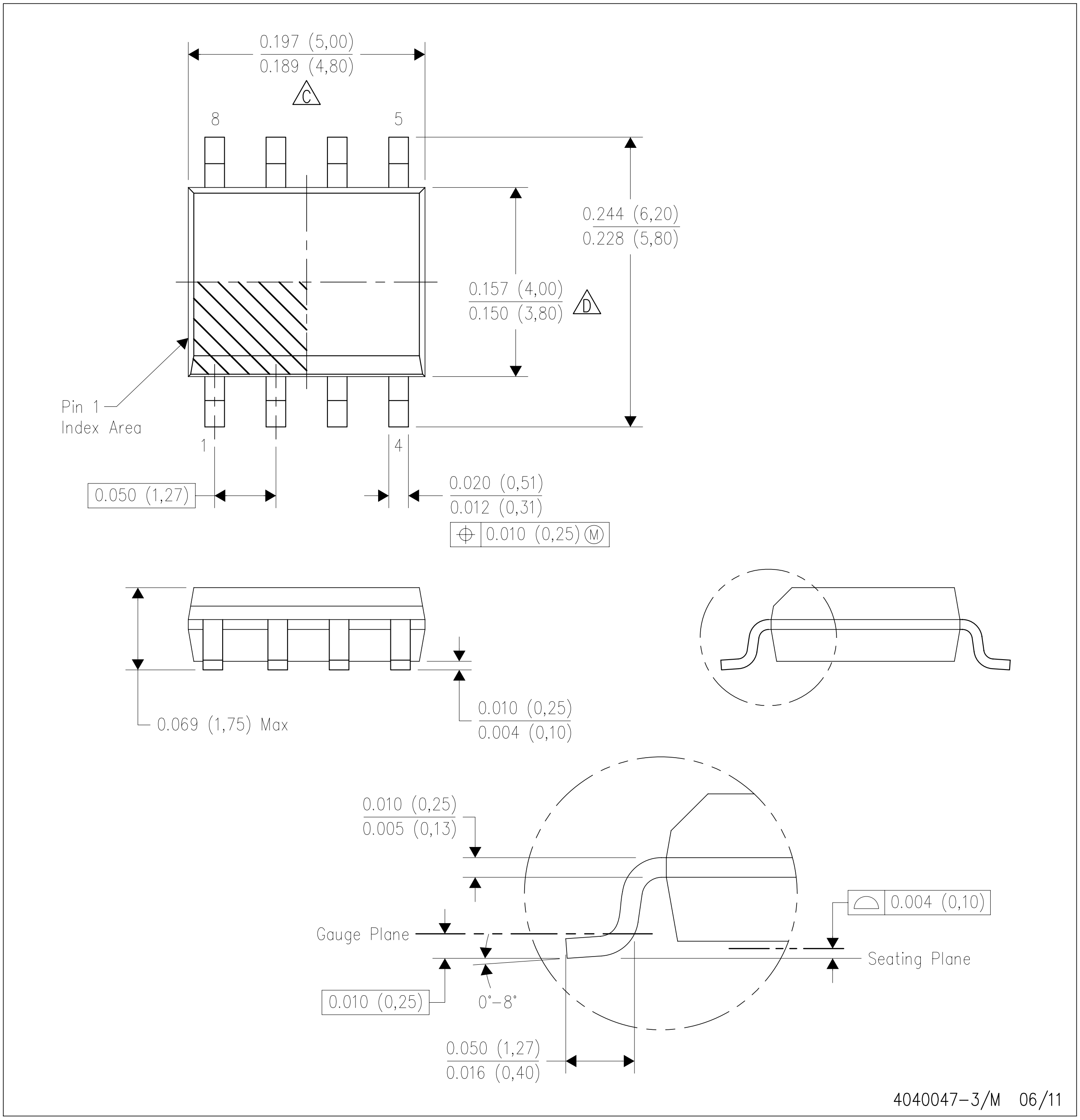
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

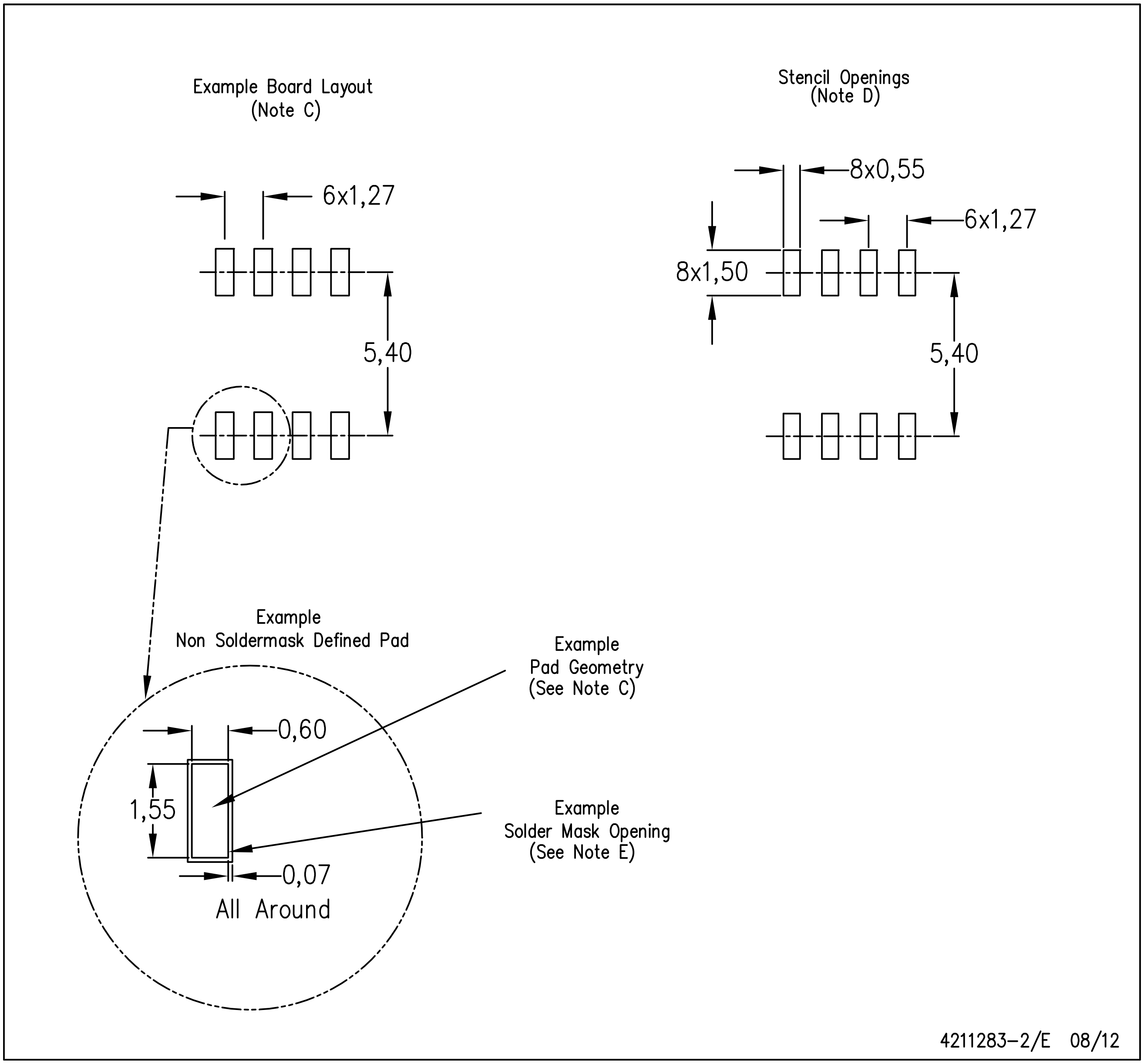
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5025AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
REF5030AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
REF5040AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
REF5045AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
REF5050AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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