HIGH-SPEED ARITHMETIC LOGIC

S54181
N74181

S54181–N,F,Q • N74181–N,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54181 and 74181 are high-speed arithmetic logic units (ALU)/ function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the 54181/74181 for fast, simultaneous carry generation with a group carry propagate (P) and carry generate (G) for the 4 bits in the package. When used in conjunction with the 54182 or 74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the 54181/74181 is 24 nanoseconds for 4 bits. When expanding to 16-bit addition with the 54182/74182, only 13 nanoseconds, further delay is added so that the total addition time is 35 nanoseconds, or 2.2 nanoseconds per bit. One 54182/74182 is needed for every 16 bits (four 54181/74181 circuits).

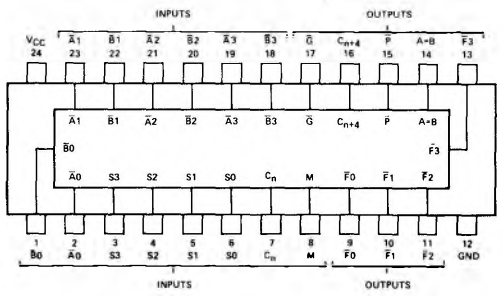
These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR and OR functions.

The 54181/74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

The 54181 is characterized for operation over the full military temperature range of -55°C to 125°C; the 74181 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

N,F,Q PACKAGE



TRUTH TABLES

TABLE OF ARITHMETIC OPERATIONS

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOW LEVELS ACTIVE	HIGH LEVELS ACTIVE
L	L	L	L	F = A minus 1	F = A
L	L	L	H	F = AB minus 1	F = A+B
L	L	H	L	F = A$\overline{B}$ minus 1	F = A+$\overline{B}$
L	L	H	H	F = minus 1 (2's complement)	F = minus 1 (2's complement)
L	H	L	L	F = A plus (A+$\overline{B}$)	F = A plus A$\overline{B}$
L	H	L	H	F = AB plus (A+$\overline{B}$)	F = (A+B) plus A$\overline{B}$
L	H	H	L	F=A minus B minus 1	F=A minus B minus 1
L	H	H	H	F = A+$\overline{B}$	F = A$\overline{B}$ minus 1
H	L	L	L	F = A plus (A+B)	F = A plus AB
H	L	L	H	F = A plus B	F = A plus B
H	L	H	L	F=A$\overline{B}$ plus (A+B)	F=(A+$\overline{B}$) plus AB
H	L	H	H	F = A+B	F = AB minus 1
H	H	L	L	F = A plus A[†]	F = A plus A[†]
H	H	L	H	F = AB plus A	F=(A+B) plus A
H	H	H	L	F = A$\overline{B}$ plus A	F=(A+$\overline{B}$) plus A
H	H	H	H	F = A	F = A minus 1

TABLE OF LOGIC FUNCTIONS

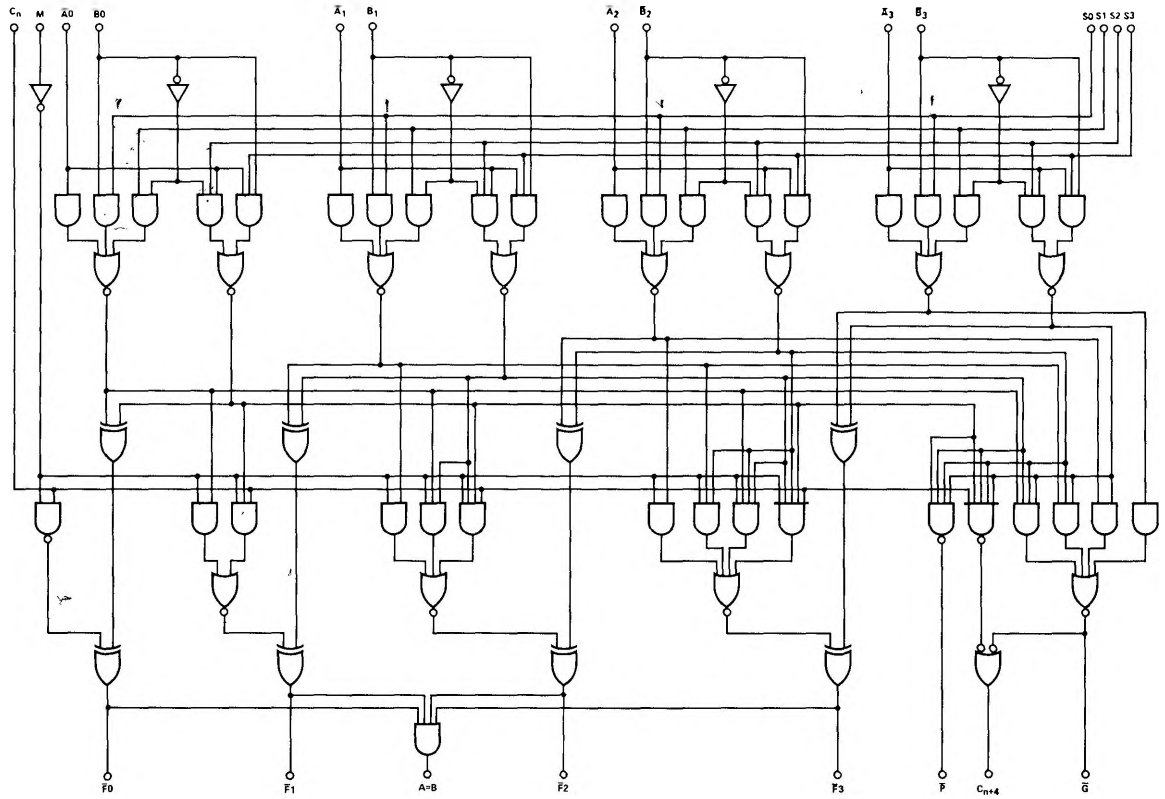
FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	NEGATIVE LOGIC	POSITIVE LOGIC
L	L	L	L	F = $\overline{A}$	F = $\overline{A}$
L	L	L	H	F = $\overline{AB}$	F = $\overline{A+B}$
L	L	H	L	F = $\overline{A}$+B	F = $\overline{A}$B
L	L	H	H	F=Logical 1	F=Logical 0
L	H	L	L	F = $\overline{A+B}$	F = $\overline{AB}$
L	H	L	H	F = $\overline{B}$	F = $\overline{B}$
L	H	H	L	F=$\overline{A + B}$	F=A + B
L	H	H	H	F = A+$\overline{B}$	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$B	F = $\overline{A}$+B
H	L	L	H	F=A + B	F=$\overline{A + B}$
H	L	H	L	F = B	F = B
H	L	H	H	F = A+B	F = AB
H	H	L	L	F= Logical 0	F=Logical 1
H	H	L	H	F = AB	F = A+$\overline{B}$
H	H	H	L	F = AB	F = A+B
H	H	H	H	F = A	F = A

Notes (See Page 158)

NOTES:
With mode control (M) and C_n low
†Each bit is shifted to the next more significant position.

With mode control (M) high: C_n irrelevant
For positive logic: logical 1 = high voltage
logical 0 = low voltage
For negative logic: logical 1 = low voltage
logical 0 = high voltage

LOGIC DIAGRAM



RECOMMENDED OPERATING CHARACTERISTICS

	S54181			N74181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature Range, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (mode input)						40	μA
I_{IH}	High-level input current (any $\overline{A}$ or $\overline{B}$ input)	V_{CC} = MAX,	V_I = 2.4V				120	μA
I_{IH}	High-level input current (any S input)						160	μA
I_{IH}	High-level input current (carry input)						200	μA
I_{IH}	High-level input current (any input)	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (mode input)						-1.6	mA
I_{IL}	Low-level input current (any $\overline{A}$ or $\overline{B}$ input)	V_{CC} = MAX,	V_I = 0.4V				-4.8	mA
I_{IL}	Low-level input current (any S input)						-6.4	mA
I_{IL}	Low-level input current (carry input)						-8	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		S54181	-20		-55	mA
				N74181	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX		S54181		88	127	mA
				N74181		88	140	
I_{CC}	Supply current	V_{CC} = MAX		S54181		94	135	mA
				N74181		94	150	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (C_L = 15pF, R_L = 400Ω)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			12	18	ns
t_{PHL}					13	19	
t_{PLH}	C_n	Any $\overline{F}$	M = 0V		13	19	ns
t_{PHL}			(SUM or $\overline{DIFF}$ mode)		12	18	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0V, S0 = S3 = 4.5V,		13	19	ns
t_{PHL}			S1 = S2 = 0V ($\overline{SUM}$ mode)		13	19	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0V, S0 = S3 = 0V,		17	25	ns
t_{PHL}			S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0V, S0 = S3 = 4.5V,		13	19	ns
t_{PHL}			S1 = S2 = 0V ($\overline{SUM}$ mode)		17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0V, S0 = S3 = 0V,		17	25	ns
t_{PHL}			S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0V, S0 = S3 = 4.5V,		28	42	ns
t_{PHL}			S1 = S2 = 0V ($\overline{SUM}$ mode)		21	32	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0V, S0 = S3 = 0V,		32	48	ns
t_{PHL}			S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		23	34	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 4.5V (logic model)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{A}$ = $\overline{B}$	M = 0V, S0 = S3 = 0V,		35	50	ns
t_{PHL}			S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		32	48	

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

TYPICAL APPLICATION DATA

Typical addition times for various configurations are given in the table below. Subtraction times are in the same range as summation times.

TYPICAL ADDITION TIMES

NO. OF BITS	TOTAL ADDITION TIME (ns)	ADD TIME PER BIT (ns)	PACKAGE COUNT	
			S54181/ N74181	S54182 N74182
4	24	6.0	1	
8	36	4.5	2	
12	48	4.0	3	
12	36	3.0	3	1
16	60	3.8	4	
16	36	2.2	4	1
32	120	3.8	8	
32	96	3.0	8	1
32	72	2.2	8	2
32	60	1.9	8	3
48	165	3.4	12	
48	148	3.1	12	1
48	132	2.7	12	2
48	108	2.2	12	3
48	60	1.25	12	4
64	220	3.5	16	
64	192	3.0	16	2
64	172	2.7	16	3
64	144	2.2	16	4
64	60	0.94	16	5