PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1660B (HIGH Z)
SP1661B (LOW Z)
DUAL 4-INPUT OR/NOR GATE

SP1660B provides simultaneous OR-NOR output functions with the capability of driving 50Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (0°C to +75°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

- Gate Switching Speed 1ns Typ.
- MECL/PECL II and MECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

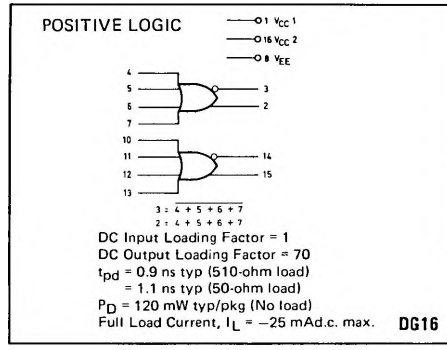

Fig. 1 Logic diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Base input voltage	0V to V_{EE}
O/P source current	< 40mA
Storage temperature	55°C to +150°C
Junction operating temp.	< +125°C

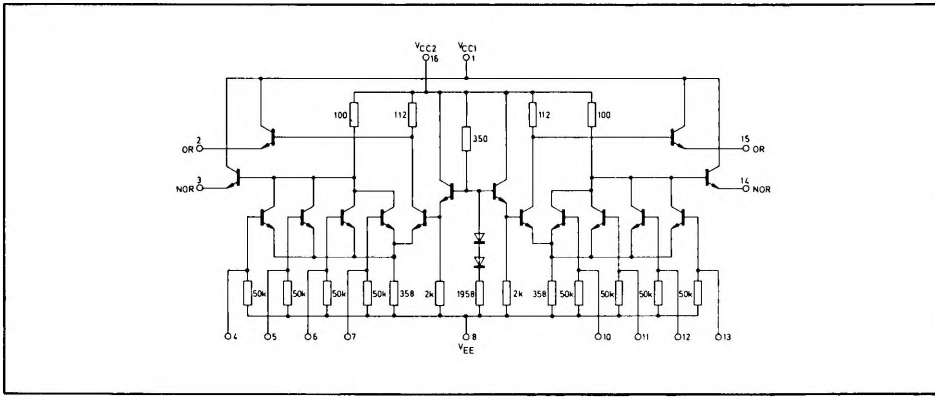

Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC 14A2CB or equivalent) or a transverse air flow greater than 500 linear ft/min should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50Ω resistor to −2.0 Vd.c.

@ Test Temperature	TEST VOLTAGE VALUES (V) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1660B Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	OV
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 0 Output Voltage	V_{OL}	3	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 1 Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 0 Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 1 Threshold Voltage	V_{OHA}	3	−1.020	–	−0.980	–	−0.920	–	V	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	−1.615	–	−1.600	–	−1.575	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	*6	–		
			–		–		–			–	–	7	–		
OR Logic 1 Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	V	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	V	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			−3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	1.1	1.7	1.1	1.7	1.2	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	1.1	1.7	1.1	1.7	1.2	1.9			2	–	–		
	t_{4+2+}	2	1.0	1.5	1.0	1.5	1.1	1.7			2	–	–		
	t_{4-3+}	3	1.0	1.5	1.0	1.5	1.1	1.7			3	–	–		
Rise Time	t_{3+}	3	1.5	2.1	1.5	2.1	1.6	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	1.5	2.1	1.5	2.1	1.6	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test.

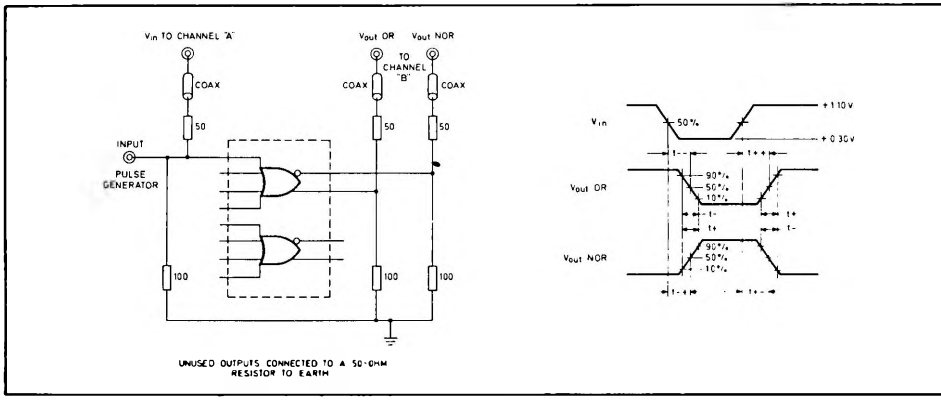

Fig. 3 Switching time test circuit and wave forms at +25°C