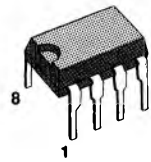
SGS-THOMSON MICROELECTRONICS

ST24C04

4K BIT (512 X 8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

- 2 PAGES OF 256 X 8 BITS
- 2 WIRE SERIAL INTERFACE, COMPATIBLE WITH THE INTER-INTEGRATED CIRCUIT (I^2C) BUS.
- SINGLE POWER SUPPLY (READ AND WRITE)
- WORD AND MULTIBYTE WRITE CAPABILITY (UP TO 4 BYTES)
- PART OF MEMORY PROTECTION CAPABILITY
- PAGE WRITE CAPABILITY
- SELF-TIMED PROGRAMMING CYCLE
- AUTOMATIC WORD ADDRESS INCREMENTING.
- SEQUENTIAL REGISTER READ
- LOW POWER CMOS
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY
- OVER 1 MILLION ERASE/WRITE CYCLES
- OVER 10 YEARS DATA RETENTION



PDIP8

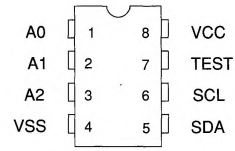
PSO14

(Ordering information at the end of the datasheet)

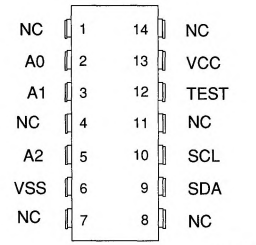
PIN NAMES

A0-A1-A2	Address Inputs
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
TEST	Test Input
V_{CC}	Power Supply

PIN CONNECTION



VR00B224



VR000233

DESCRIPTION

The ST24C04 is a 4096 bits read/write non volatile memory organized in 512 words of 8 bits and is manufactured in SGS-THOMSON highly reliable CMOS EEPROM technology.

It is an external memory accessed via a simple serial interface. This serial interface based on a two wire bus, allows bi-directional communication between devices.

The 4K bits memory capacity is divided in two pages of 256 words of 8 bits. All memory operations are synchronized on an external strobe: SCL bus. The Read and Write operations are initiated by a Start instruction sent on the SDA bus by the master device.

The Start instruction includes a Start condition followed by an 8 bit word : the seven first bits address the right EEPROM slave device and the last bit defines the kind of operation to follow : Read or Write. A Start instruction is ended by an acknowledge of the slave device. The specific address of a given ST24C04 is hardwired through the 2 address pins A1 and A2.

The ST24C04 features 3 kind of operations:

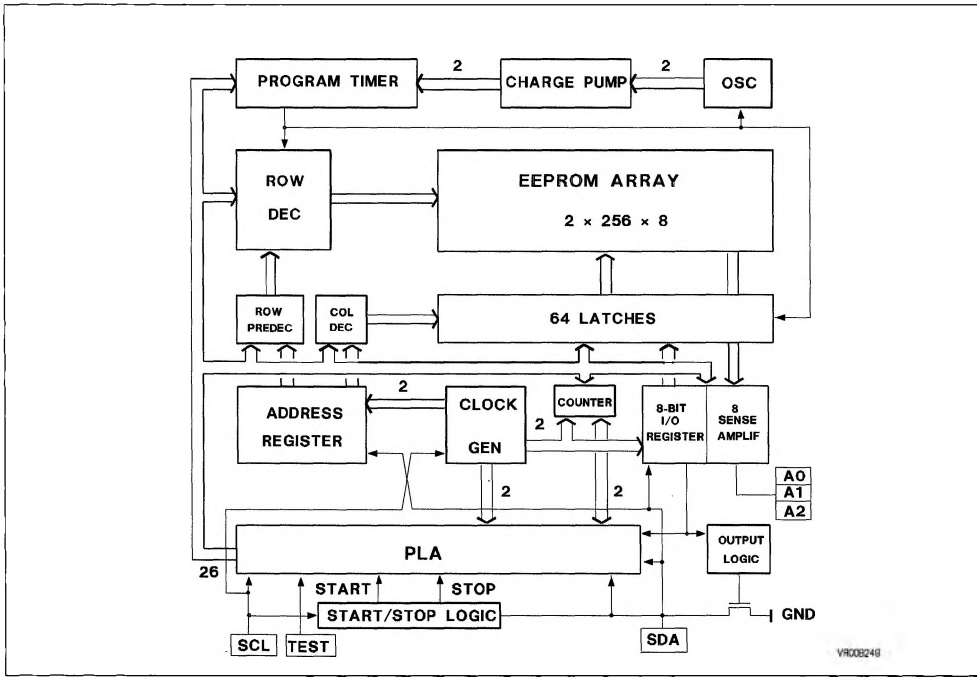
- Byte Write: 8 bits are written at the address previously defined in the byte write operation mode.
- Multibyte programming which allows to write consecutively up to 4 words in any location of the memory array in a single programming cycle.
- Page Write mode which allows to write from 2 to 8 bytes in a single programming cycle.

In Read Mode 3 read operations are available for the user:

- The Current Address read performs a read operation at the previously pointed address incremented by one.
- The Random Read performs a read operation at the address defined in the randon read instruction
- The Sequential Read performs either a Current Address read or a Random Read, but reads consecutive words provided the master device acknowledges each string of 8 bits read from the memory without generating a STOP condition.

The design of the ST24C04 and its processing with a highly reliable technology yields to typical endurance better than 1 million cycles and Data Retention greater than 10 years.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	- 65 to 150	°C
Input or Output Voltage with respect to ground	- 0.3 to 6.5	V
Lead Temperature (soldering, 10 seconds)	+ 300	°C
ESD Rating	2000	V

OPERATING CONDITIONS

Ambient Operating Temperature		
ST24C04-1	0 to 0.70	°C
ST24C04-6	- 40 to +85	°C
ST24C04-3	- 40 to +125	°C
POWER SUPPLY	4.5 to 5.5	V

D.C. OPERATING CHARACTERISTICS ta=-40°C to +125°C according to selected temperature range VCC=5V ±10%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{CC}	Power Supply Current			2	mA	f_{SCL} = 100kHZ
I_{SB}	Standby Current		100		µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND or V_{CC}
I_{LO}	Ouput Leakage Current			10	µA	V_{OUT} = GND or V_{CC}
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 .7xV_{cc}		.3xV_{cc} V_{cc}+1.0	V V	
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 V_{cc} - 0.5		+ 0.5 V_{cc} + 1.0	V V	A0, A1, A2 inputs A0, A1, A2 inputs
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

A.C. CHARACTERISTICS t_a=-40°C to 125°C according to selected temperature range
V_{CC}=5V ±10%, unless otherwise specified

SYMBOL		MIN.	TYP.	MAX.	UNITS
f_{SCL}	SCL Clock Frequency	0		100	kHZ
T_I	Noise Suppression Time Constant on SCL, SDA Inputs			100	ns
t_{AA}	SCL Low to SDA Data Valid	300			ns
t_{BUF}	Time the bus must be be free before a new transmission.	4.7			µs
$t_{HD:STA}$	START Condition Hold Time	4.0			µs
t_{LOW}	Clock Low Period	4.7			µs
t_{HIGH}	Clock High Period	4.0			µs
$t_{SU:STA}$	Start Condition Setup Time (For a repeated START condition)	4.7			µs
$t_{HD:DAT}$	DATA IN Hold Time	0			ns
$t_{SU:DAT}$	DATA IN Setup Time	250			ns
t_R	SDA & SCL Rise Time			1	µs
t_F	SDA & SCL Fall Time			300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4.7			µs
t_{DH}	DATA OUT Hold Time	300			ns
t_{WR}	Programming Time (note 1)			10.	ms
Endurance	W/E Cycles	1 million Cycles minimum			

Note 1: in multibyte programming mode and only in this mode,if the accessed words are located in two consecutive rows the maximun programming time will be extended to two times tWR.

FIGURE 1 : BUS TIMING

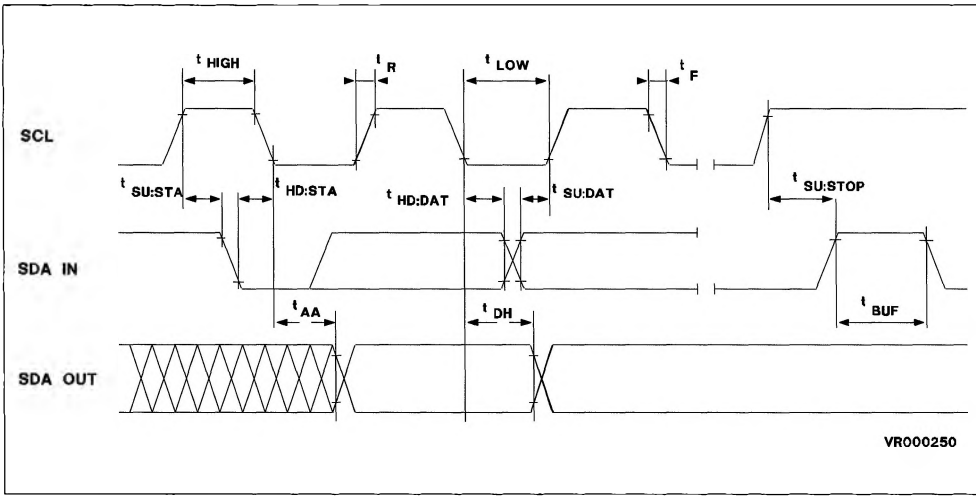
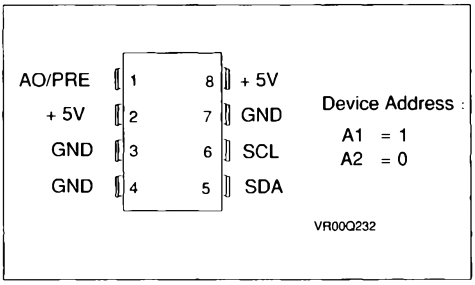


FIGURE 2 : TYPICAL INTERFACE



PIN DESCRIPTION

SERIAL CLOCK (SCL)
The SCL input is used to clock all data into or out of the device.

SERIAL DATA (SDA)
SDA is a bidirectional pin used to transfer data into or out of the device.It is an open drain output that may be wired with any open drain or open collector outputs to formed the system SDA bus.

ADDRESS (A0/PRE)
For proper device operation this pin must be tied to V_{SS} or V_{CC}

- When set to VSS all the memory array can be accessed in read or write mode.
- When set to VCC this pin is considered as a protection key, therefore allowing the upper portion of the memory to be protected in write mode. (See "PROTECT MODE" section in the following pages of the Data sheet).

ADDRESS (A1,A2)
These two addresses inputs are used to set the fifth and sixth bits of the seven bits slave address.These inputs can be used static or driven. When used statically they must be tied to V_{CC} or V_{SS}. When used driven CMOS levels have to applied to the device.

TEST PIN (TEST)
For proper device operation this input must be tied to V_{SS} or V_{CC} According to the voltage on TEST pin up to four or eight bytes may be written in the ST24C04 in a single write operation (see "Write Operation" section.)

DEVICE OPERATION

The ST24C04 supports the I^2C (bidirectional bus oriented) protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and the device being controlled is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations. Therefore, the ST24C04 will be considered as a slave receiver or transmitter in all applications.

DATA TRANSITION
Data transition on the SDA line must only occur when the clock SCL is Low. SDA transitions while SCL is HIGH will be interpreted as START or STOP conditions. See Fig 1.

START CONDITION
A START condition is defined by a HIGH to LOW transition of THE SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The ST24C04 continuously monitors the SDA and SCL lines for a START and will not respond to any command if this condition has not been met.

STOP CONDITION
A STOP condition is defined by a LOW to HIGH transition of the SDA line while the SCL is at a stable HIGH level. This condition terminates communication between devices and forces the ST24C04 in the standby power mode.

ACKNOWLEDGE
Acknowledge is used to indicate successfull data transfer. The transmitter (master or slave) will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line LOW to indicate it received the 8 bits of data.

DATA TRANSFER
During Data Transfer the ST24C04 samples the SDA line on the leading edge of SCL clock.Therefore,for proper device operation SDA line must be stable during the SCL LOW to HIGH transition.

Note In the I^2C protocol ,the SDA bus must be connected to the positive power supply through a pull-up resistor.

DEVICE ADDRESSING

To start communication between two devices, the bus master must initiate a start instruction sequence; following a START condition the master sends onto the SDA bus an eight bit word correspondind to the address of the device it is addressing.

- The most significant 4 bits of the slave address , therefore the first bits sent onto the bus are the device type identifier. The ST24C04 memory device type is fixed as "1010".
- The next 2 significant bits are used to address a particular device of the previously defined type connected to the bus. The state of the hardwired A1 and A2 pins defines the device address. Up to four ST24C04 can be connected on the same bus.
- The next bit of the slave address field is the most significant bit of the word address ; it is used as the page select bit.
- The last bit of the start instruction defines the type of operation to be performed:

- When set to "1" a read operation is selected
- When set to "0" a write operation is selected

Chip selection is accomplished by setting the two bits of the chip address field to the corresponding levels of A1 and A2 inputs. After a START condition is detected all ST24C04 connected to the bus will compare the slave address being transmitted with their own hardwired address (A1 and A2). After comparison , the selected ST24C04 will acknowledge on the SDA line and will perform the read or write operation according to the state of the R/W bit.

WRITE OPERATION

The standard operation mode is byte write or multibyte programming. If pin 7 is forced to Vss the ST24C04 switches to page mode.

BYTE WRITE
In this mode, following a START condition the master sends a slave address word with the R/W bit set to "0". The ST24C04 will acknowledge this first transmission and waits for a second word : the word address field.This 8 bit address field provides access to any of the 256 words of the selected page. Upon receipt of the word address the ST24C04 slave device will respond with an acknowledge. At this time, all following words transmitted to the ST24C04 will be considered as Data. In Byte Write mode the master sends one word which is acknowledged by the ST24C04. Then the master terminates the transfer by generating a STOP condition. This STOP condition initiates the internal self-timed programming cycle.

While the internal programming cycle is in progress the ST24C04 will not respond to any request from the bus master.

FIGURE 3 : SLAVE ADDRESS ALLOCATION

	Device type				Device Address		Page	
START	1	0	1	0	A2	A1	A0	R/W
	Slave Address							

MULTIBYTE PROGRAMMING
The ST24C04 is able to write consecutively up to 4 bytes in the multibyte programming mode. As in the Byte Write programming mode,the multibyte programming can be started at any specified address and whithout any restriction of any kind. This multibyte mode is started and performed in the same way as the Byte Write mode; but instead of terminating the write sequence after the first data word is transfered,the master does not generate a STOP condition and up to 3 additional words can be transmitted to the ST24C04. After receipt of each word,the ST24C04 will respond with an acknowledge. After the bytes to be written (4 bytes maximun) have been transfered, the master generates a STOP condition which starts the internal self-timed programming cycle.

PAGE WRITE (only available if pin 7 is grounded)
The ST24C04 is able to write up to 8 bytes in a Page Write operation. This mode allows to write 2 to 8 bytes in a single write cycle provided they are all topologically located in the same physical row.(five most significant address bits identical.)

This mode is started and performed in the same way as the byte write operation, but instead of terminating the write sequence after the first data word is transfered, the master doesn't generate a STOP condition and can transmit up to seven additional words. After receipt of each word the ST24C04 will respond with an acknowledge.

After receipt of each data word the internal address counter is automatically incremented by one. Only the three low order address bits are incremented, the high order five bits remain constant.

Therefore, a special attention has to be paid when using this feature in order to avoid any scrambling or over writing. If more than 8 words are transmitted the address counter will "roll-over" and the previously written data will be overwritten. As in byte write operation the master terminates the transfer by generating a stop condition that triggers the internal programming cycle.

All inputs are disabled until completion of the internal write cycle.

READ OPERATIONS

Read operations are initiated in the same manner as the write operation with the exception that the R/W bit following the slave address in the start instruction is set to a logical "1". Three read operation modes are available:

- current address read
- random read
- sequential read

CURRENT ADDRESS READ

The ST24C04 has an internal address counter that points the address of the last word accessed incremented by one. Therefore if the last access (either read or write) was to address n, the next current read operation will access data from address n+1. To initiate this read mode the master generates a start instruction (START condition followed by the eight bit slave address word) with the R/W bit set to one. The ST24C04 will respond with an acknowledge and transmit the 8 bits of data. To terminate the transfer the master MUST not acknowledge the transfer and DOES generate a STOP condition.

RANDOM READ

The random read mode allows the master to access any memory location. In order to load into the device the word address the master must first performed a "dummy" write sequence.(START, slave address ,R/W bit set to "0",followed by the word address to be read). After the word address has been acknowledged,the master immediately reissues a START instruction whith the R/W bit set to "1". The ST24C04 will acknowledge the transfer and output the 8 bits of the addressed word. As in current address read to terminate the transfer the master MUST not acknowledge the transfer and DOES generate a STOP condition.

SEQUENTIAL READ

This mode can be initiated with either a current address read or random read. The first word read out of the memory is transmitted in the same way as in both previous modes,however the master must now acknowledge the transfer indicating it requires more data. The ST24C04 will output a string of eight bits for each acknowledge it received. As in the other read modes to terminate the transfer the master MUST not acknowledge the last transfer and DOES generate a STOP condition.

The data output is sequential;data from address n followed by data from address n+1. The internal address counter is automaticaly incremented allowing the entire content of the 512 words page to be serially read in a single read operation.If more than 512 words are read the counter will "roll-over" and the ST24C04 will continue to output data for each acknowledge received.

SDA BUS IN READ MODE

In all read modes the ST24C04 is waiting for an acknowledge (SDA line low) on the 9th clock pulse of a data transfer.If an acknowledge is not detected,the ST24C04 terminates the data transfer and switches to a "receiver" state.

PROTECT MODE

This mode is activated only if pin AO/PRE is set to V_{CC}. In this mode the upper page of the memory (A_0=1) can be protected against spurrious or parasitic writes.

The depth of the protected zone is defined by the user when programming the last byte of the memory (address FF hex in the upper page (A_0=1))

This byte called PROTECT REGISTER defines the address of the first memory location to be protected.

To use properly the ST24C04 in this specific mode, the user must write first into the memory the pattern he wants to protect, then lock the access of this protected zone by writing into the PROTECT REGISTER (address FF Hex) the address of the first location to be protected.

As the Protect Register is included into the protected zone the only way to change the protected zone depth or content is to set pin 1 (AO/PRE) to ground and disable the protect mode.

Protect Register definitions :

The 5 most significant bits : first address to be protected. The first address to be protected is defined every 8 bytes thus a maximum of 256 bytes can be protected with a minimum of 8 bytes.

The 6th bit is the protection mode flag.

- When set to 1 : protection mode is disabled

- When set to 0 : protection mode is enabled

The 2 last bits are don't- care

A	A	A	A	A	F	X	X
<----		Adress		---->	Flag		

Example : Configuration register : 001010XX addresses ranging from 28 hex to FF hex are protected.

Remark :

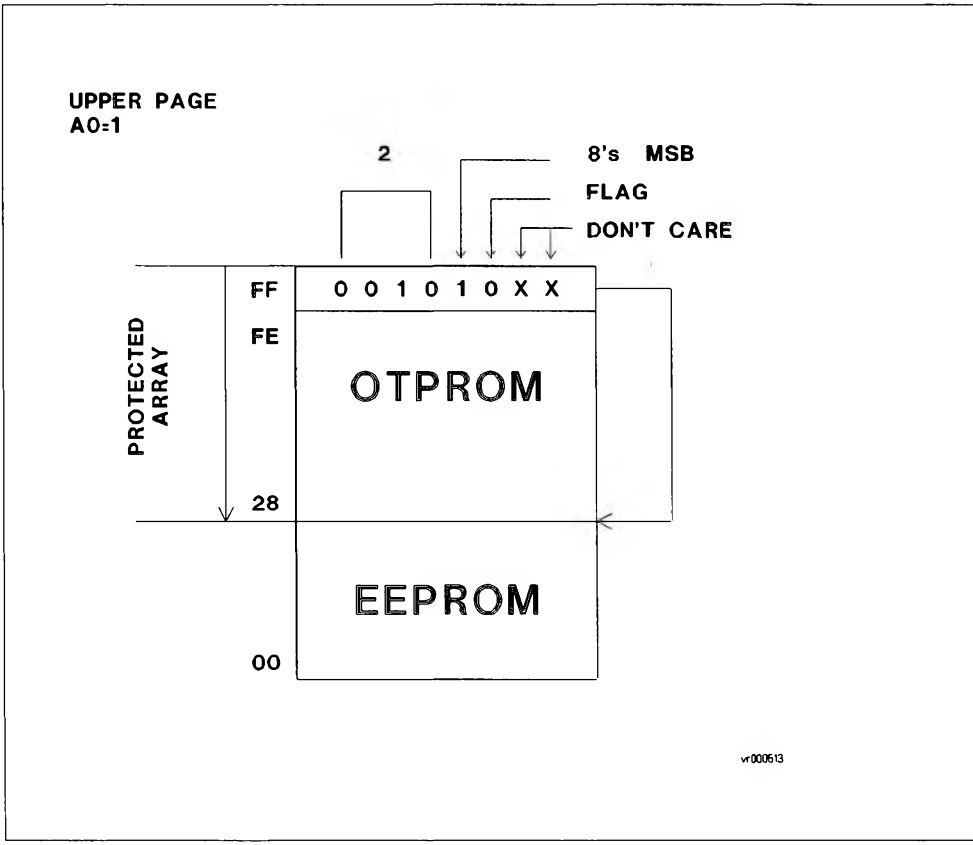
A special attention has to be paid when using this mode with TEST pin set to "1" (multibyte mode).

In this mode the ST24C04 doesn't roll over on the last 3 least significant bits of the address word, therefore is able to enter the protected portion as described previously.

In this case the first protected address is defined by the content of the PROTECT REGISTER plus 3 bytes .

Ex : if Protected Register content is 001010XX
Addresses 2B hex to FF are protected.
Addresses 28, 29, 2A hex are not protected.

FIGURE 3 BIS : MEMORY PROTECTION



TIMMING DIAGRAMS

FIGURE 4 : BYTE WRITE

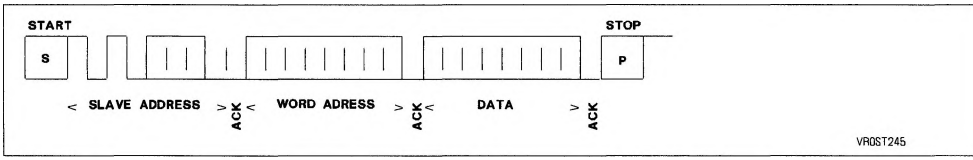


FIGURE 5 : PAGE WRITE

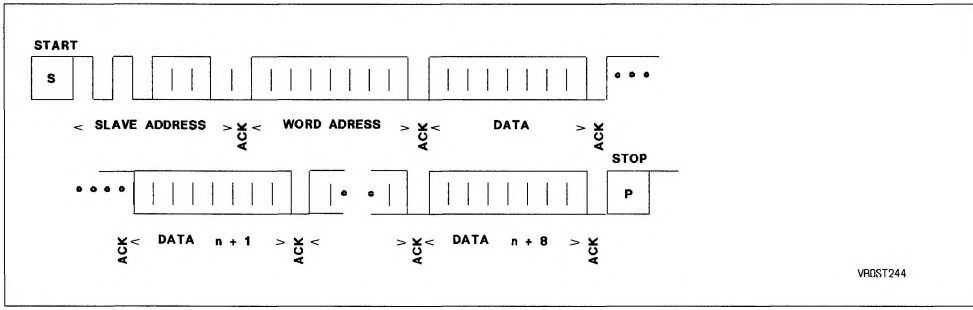


FIGURE 6 : CURRENT ADDRESS READ

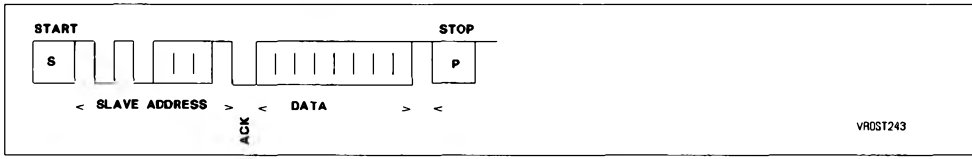


FIGURE 7 : RANDOM ADDRESS READ

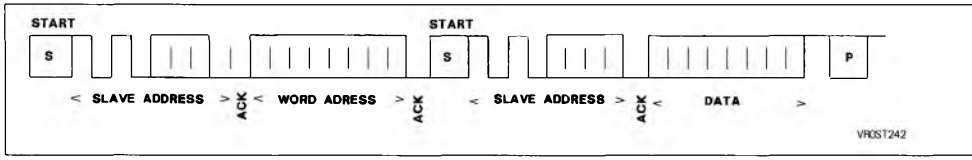
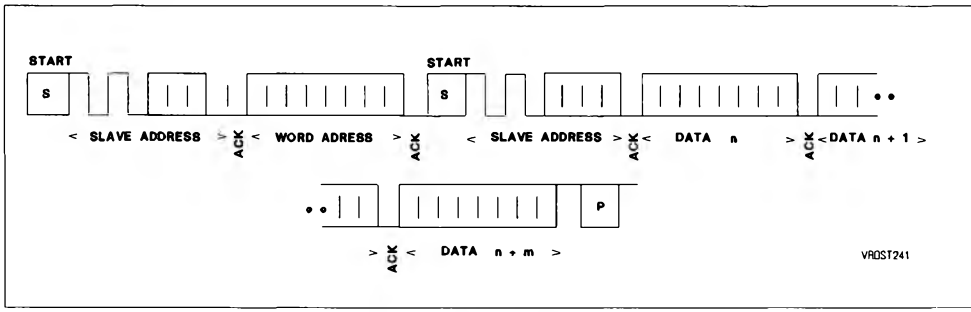


FIGURE 8 : SEQUENTIAL READ

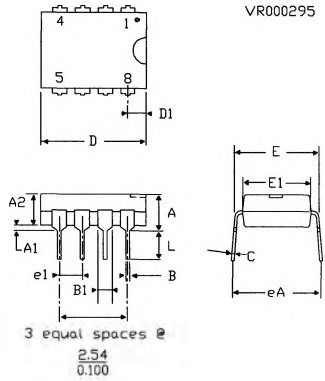


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST24C04B1	Dual-in-line	0°C to 70°C	4.5V to 5.5V
ST24C04ML1	SO 14		
ST24C04B6	Dual-in-line	-40°C to 85°C	
ST24C04ML6	SO 14		
ST24C04B3	Dual-in-line	-40°C to 125°C	
ST24C04ML3	SO 14		

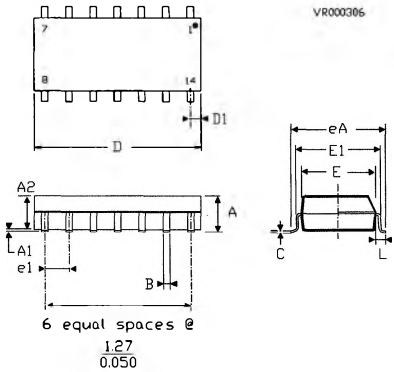
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO14 PACKAGE (ML)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10		0.20	.004		.008
A2			1.60			0.063
B	0.35		0.46	.014		.018
C	0.19		0.25	.007		.010
D	8.55		8.75	.337		.344
D1			0.68			.027
E	3.80		4.00	.150		.157
E1	4.60		5.30	.181		.209
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.50		1.27	.020		.050