Features

- **No External Components Except PIN Diode**
- **Supply-voltage Range: 2.7 V to 5.5 V**
- **Automatic Sensitivity Adaptation (AGC)**
- **Automatic Strong Signal Adaptation (ATC)**
- **Automatic Supply Voltage Adaptation**
- **Enhanced Immunity against Ambient Light Disturbances**
- **Available for Carrier Frequencies between 30 kHz to 76 kHz; adjusted by Zener-Diode Fusing ± 2.5%**
- **TTL and CMOS Compatible**

Applications

- **Audio Video Applications**
- **Home Appliances**
- **Remote Control Equipment**

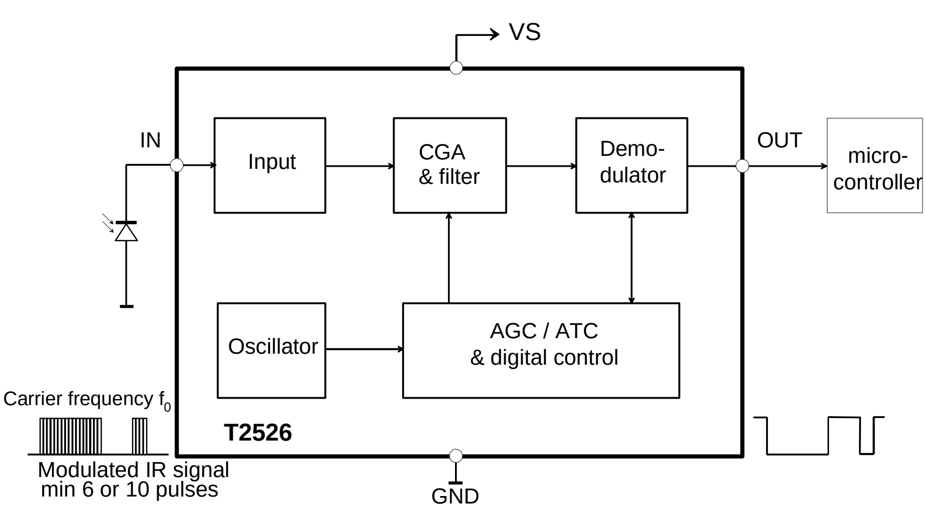
Low-voltage IR Receiver ASSP

T2526

Description

The IC T2526 is a complete IR receiver for data communication developed and optimized for use in carrier-frequency-modulated transmission applications. Its function can be described using the block diagram of Figure 1. The input stage meets two main functions. First it provides a suitable bias voltage for the PIN diode. Secondly the pulsed photo-current signals are transformed into a voltage by a special circuit which is optimized for low noise applications. After amplification by a **c**ontrolled **g**ain **a**mplifier (CGA) the signals have to pass a tuned integrated narrow bandpass filter with a center frequency f_0 which is equivalent to the choosen carrier frequency of the input signal The demodulator is used first to convert the input burst signal to a digital envelope output pulse and to evaluate the signal information quality, i.e., unwanted pulses will be suppressed at the output pin. All this is done by means of an integrated dynamic feedback circuit which varies the gain as a function of the present enviromental conditions (ambient light, modulated lamps etc.). Other special features are used to adapt to the current application to secure best transmission quality. The T2526 operates in a supply-voltage range from 2.7 V to 5.5 V. By default, the T2526 is optimized for best performance within 2.7 V to 3.3 V.

Figure 1. Block Diagram



Rev. 4597A–AUTO–01/03

Pin Configuration

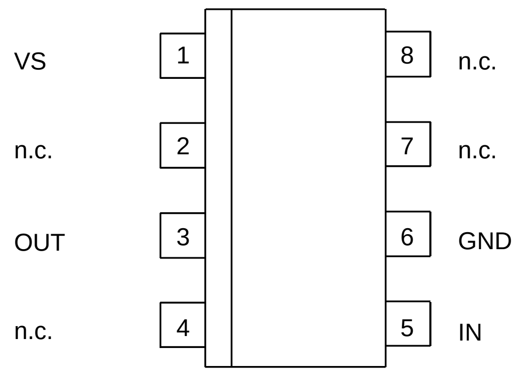


Figure 2. Pinning SO8 and TSSOP8

Pin Description

Pin	Symbol	Function
1	VS	Supply voltage
2	n.c.	Not connected
3	OUT	Data output
4	n.c.	Not connected
5	IN	Input PIN-diode
6	GND	Ground
7	n.c.	Not connected
8	n.c.	Not connected

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V_S	-0.3 to 6	V
Supply current	I_S	3	mA
Input voltage	V_{IN}	-0.3 to V_S	V
Input DC current at V_S = 5 V	I_{IN}	0.75	mA
Output voltage	V_O	-0.3 to V_S	V
Output current	I_O	10	mA
Operating temperature	T_{amb}	-25 to +85	°C
Storage temperature	T_{stg}	-40 to +125	°C
Power dissipation at T_{amb} = 25°C	P_{tot}	30	mW

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient SO8	R_{thJA}	130	k/W
Junction ambient TSSOP8	R_{thJA}	tbd	K/W

Electrical Characteristics, 3-V Operation

T_{amb} = -25°C to 85°C, V_S = 2.7 V to 3.3 V unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Supply**								
1.1	Supply-voltage range		1	V_S	2.7	3.0	3.3	V	C
1.2	Supply current	I_{IN} =0	1	I_S	0.7	0.9	1.2	mA	B
2	**Output**								
2.1	Internal pull-up resistor [1)]	T_{amb} = 25°C; see Figure 12	1, 3	R_{PU}		30/40		kΩ	A
2.2	Output voltage low	R_2 = 2.4 kΩ; see Figure 12	3, 6	V_{OL}			250	mV	B
2.3	Output voltage high		3, 1	V_{OH}	V_S-0.25		Vs	V	B
2.4	Output current clamping	R_2 = 0; see Figure 12	3, 6	I_{OCL}		8		mA	B
3	**Input**								
3.1	Input DC current	V_{IN} = 0; see Figure 12	5	I_{IN_DCMAX}	-150			µA	C
3.2	Input DC current; see Figure 5	V_{IN} = 0; Vs = 3 V, T_{amb} = 25°C	5	I_{IN_DCMAX}		-350		µA	B
3.3	Min. detection threshold current; see Figure 3	Test signal: see Figure 11 V_S = 3 V, T_{amb}= 25°C, I_{IN_DC}=1µA; square pp, burst N=16, f = f_0; t_{PER} = 10 ms, Figure 10; BER = 50[2)]	3	I_{Eemin}		-700		pA	B
3.4	Min. detection threshold current with AC current disturbance IIN_AC100 = 3 µA at 100 Hz		3	I_{Eemin}		-1500		pA	C
3.5	Max. detection threshold current with V_{IN} > 0V	Test signal: see Figure 11 V_S = 3 V, T_{amb} = 25°C, I_{IN_DC} = 1 µA; square pp, burst N = 16, f = f_0; t_{PER} = 10 ms, Figure 10; BER = 5%[2)]	3	I_{Eemax}	-200			µA	D

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Depending on version, see “Ordering Information”
2. BER = bit error rate; e.g., BER = 5% means that with P = 20 at the input pin 19...21 pulses can appear at the Pin OUT
3. After transformation of input current into voltage

Electrical Characteristics, 3-V Operation (Continued)

T_{amb} = -25°C to 85°C, V_S = 2.7 V to 3.3 V unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4	**Controlled Amplifier and Filter**								
4.1	Max. value of variable gain (CGA)			G_{VARMAX}		51		dB	D
4.2	Min. value of variable gain (CGA)			G_{VARMIN}		-5		dB	D
4.3	Total internal amplification[3)]			G_{MAX}		71		dB	D
4.4	Center frequency fusing accuracy of bandpass	V_S = 3 V, T_{amb} = 25°C		f_{03V_FUSE}	-2.5	f_0	+2.5	%	A
4.5	Overall accuracy center frequency of bandpass			f_{03V}	-5.5	f_0	+3.5	%	C
4.6	Overall accuracy center frequency of bandpass	T_{amb} = 0 to 70°C		f_{03V}	-4.5	f_0	+3.0	%	C
4.7	BPF bandwidth	-3dB; f_0 = 38 kHz; see Figure 9		B		3.8		kHz	C

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Depending on version, see “Ordering Information”
2. BER = bit error rate; e.g., BER = 5% means that with P = 20 at the input pin 19...21 pulses can appear at the Pin OUT
3. After transformation of input current into voltage

Electrical Characteristics, 5-V Operation

T_{amb} = -25°C to 85°C, V_S = 4.5 V to 5.5 V unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	**Supply**								
5.1	Supply-voltage range		1	V_S	4.5	5.0	5.5	V	C
5.2	Supply current	I_{IN} =0	1	I_S	0.9	1.2	1.5	mA	B
6	**Output**								
6.1	Internal pull-up resistor[1)]	T_{amb} = 25°C; see Figure 12	1,3	R_{PU}		30/40		kΩ	A
6.2	Output voltage low	R_2 = 2.4 kΩ; see Figure 12	3,6	V_{OL}			250	mV	B
6.3	Output voltage high		3,1	V_{OH}	V_S-0.25		Vs	V	B
6.4	Output current clamping	R_2 = 0; see Figure 12	3,6	I_{OCL}		8		mA	B

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Depending on version, see “Ordering Information”
2. BER = bit error rate; e.g., BER = 5% means that with P = 20 at the input pin 19...21 pulses can appear at the Pin OUT
3. After transformation of input current into voltage

Electrical Characteristics, 5-V Operation (Continued)

T_{amb} = -25°C to 85°C, V_S = 4.5 V to 5.5 V unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	**Input**								
7.1	Input DC current	V_{IN} = 0; see Figure 12	5	I_{IN_DCMAX}	-400			µA	C
7.2	Input DC-current; see Figure 6	V_{IN} = 0; Vs = 5 V, T_{amb} = 25°C	5	I_{IN_DCMAX}		-700		µA	B
7.3	Min. detection threshold current; see Figure 4	Test signal: see Figure 11 V_S = 5 V, T_{amb} = 25°C, I_{IN_DC} = 1µA; square pp, burst N = 16, f = f_0; t_{PER} = 10 ms, Figure 10; BER = 50[2)]	3	I_{Eemin}		-890		pA	B
7.4	Min. detection threshold current with AC current disturbance IIN_AC100 = 3 µA at 100 Hz		3	I_{Eemin}		-2500		pA	C
7.5	Max. detection threshold current with V_{IN} > 0V	Test signal: see Figure 11 V_S = 5 V, T_{amb} = 25°C, I_{IN_DC} = 1µA; square pp, burst N = 16, f = f_0; t_{PER} = 10 ms, Figure 10; BER = 5%[2)]	3	I_{Eemax}	-500			µA	D
8	**Controlled Amplifier and Filter**								
8.1	Max. value of variable gain (CGA)			G_{VARMAX}		51		dB	D
8.2	Min. value of variable gain (CGA)			G_{VARMIN}		-5		dB	D
8.3	Total internal amplification[3)]			G_{MAX}		71		dB	D
8.4	Resulting center frequency fusing accuracy	f_0 fused at V_S = 3 V V_S = 5 V, T_{amb} = 25°C		f_{05V}		$f_{03V\text{-}FUSE}$ +0.5		%	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Depending on version, see "Ordering Information"
2. BER = bit error rate; e.g., BER = 5% means that with P = 20 at the input pin 19...21 pulses can appear at the Pin OUT
3. After transformation of input current into voltage

ESD

All pins ⇒ 2000V HBM; 200V MM, MIL-STD-883C, Method 3015.7

Reliability

Electrical qualification (1000h) in molded SO8 plastic package

Typical Electrical Curves at T_{amb} = 25°C

Figure 3. I_{Eemin} versus I_{IN_DC} , V_S = 3 V

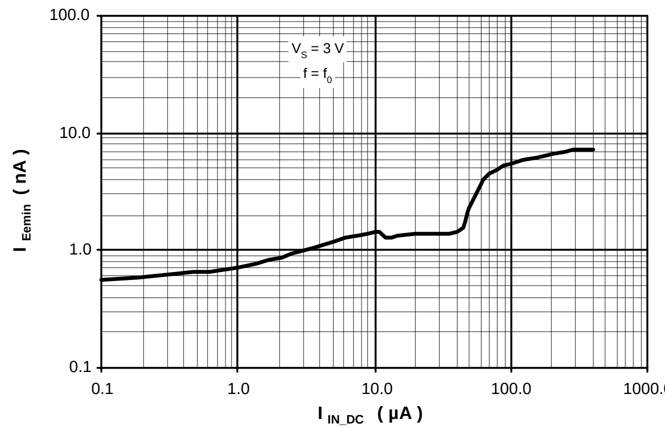


Figure 4. I_{Eemin} versus I_{IN_DC} , V_S = 5 V

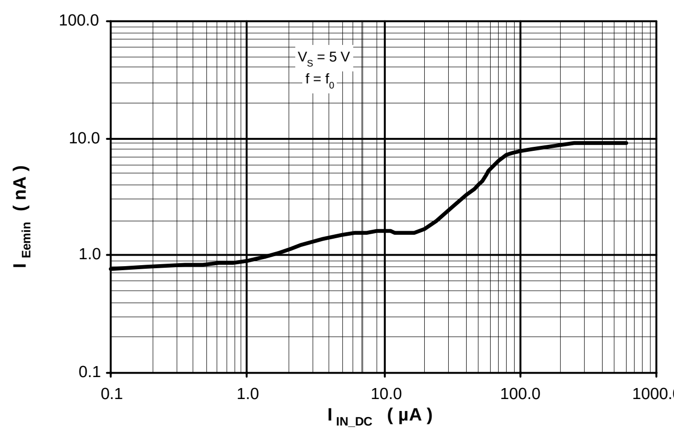


Figure 5. V_{IN} versus I_{IN_DC}, V_S = 3 V

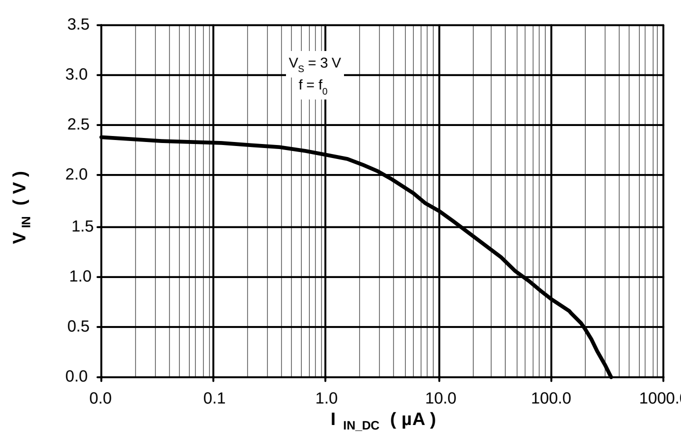


Figure 6. V_{IN} versus I_{IN_DC}, V_S = 5 V

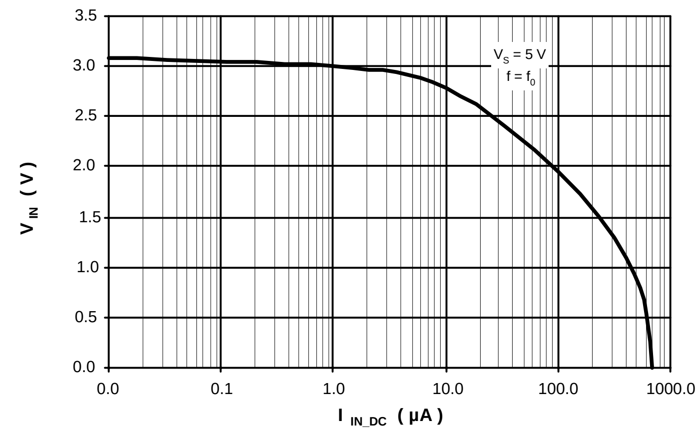


Figure 7. Data Transmission Rate, V_S = 3 V

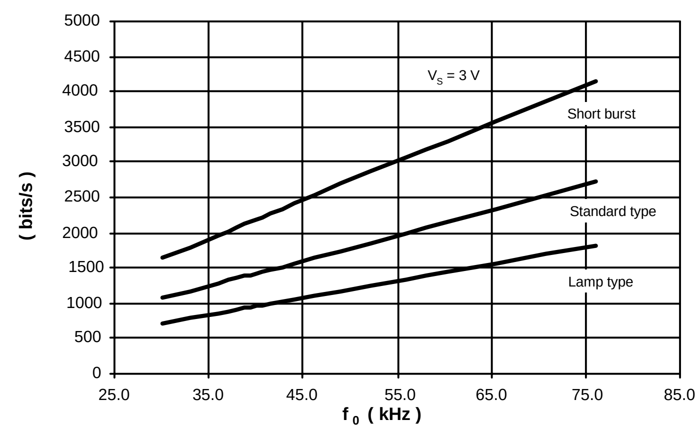


Figure 8. Data Transmission Rate, V_S = 5 V

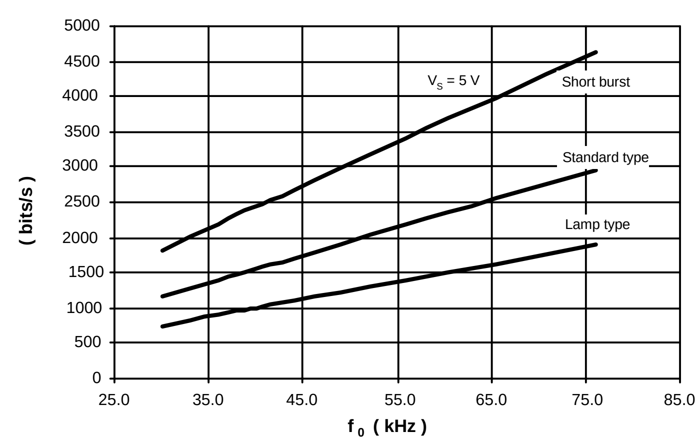
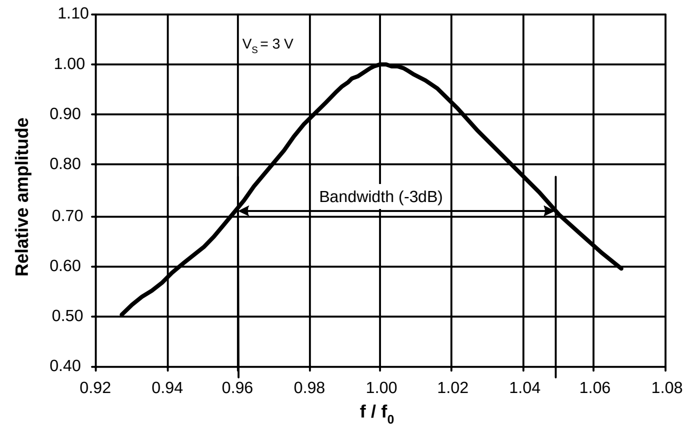


Figure 9. Typical Bandpass Curve



$Q = f/f_0/B$; B => -3 dB values.

Example: $Q = 1/(1.047 - 0.954) = 11$

Figure 10. Illustration of Used Terms

Example: f = 30 kHz, burst with 16 pulses, 16 periods

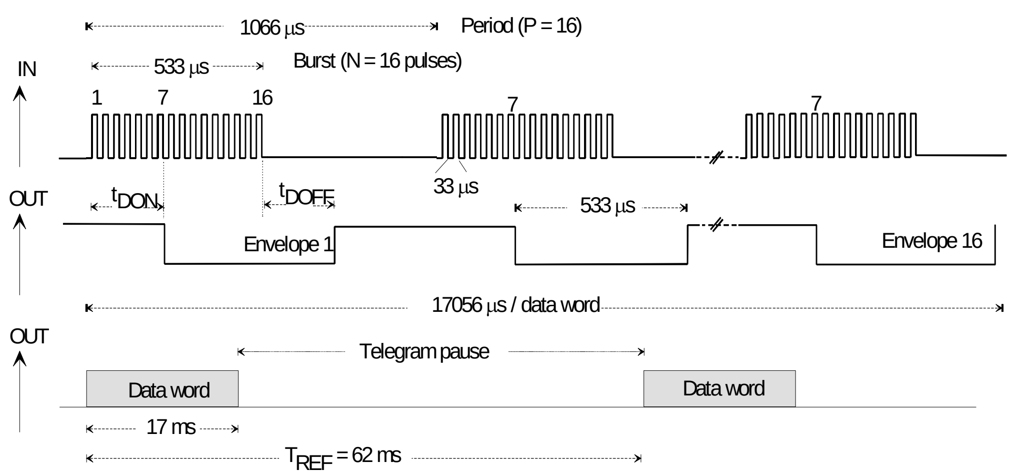


Figure 11. Test Circuit

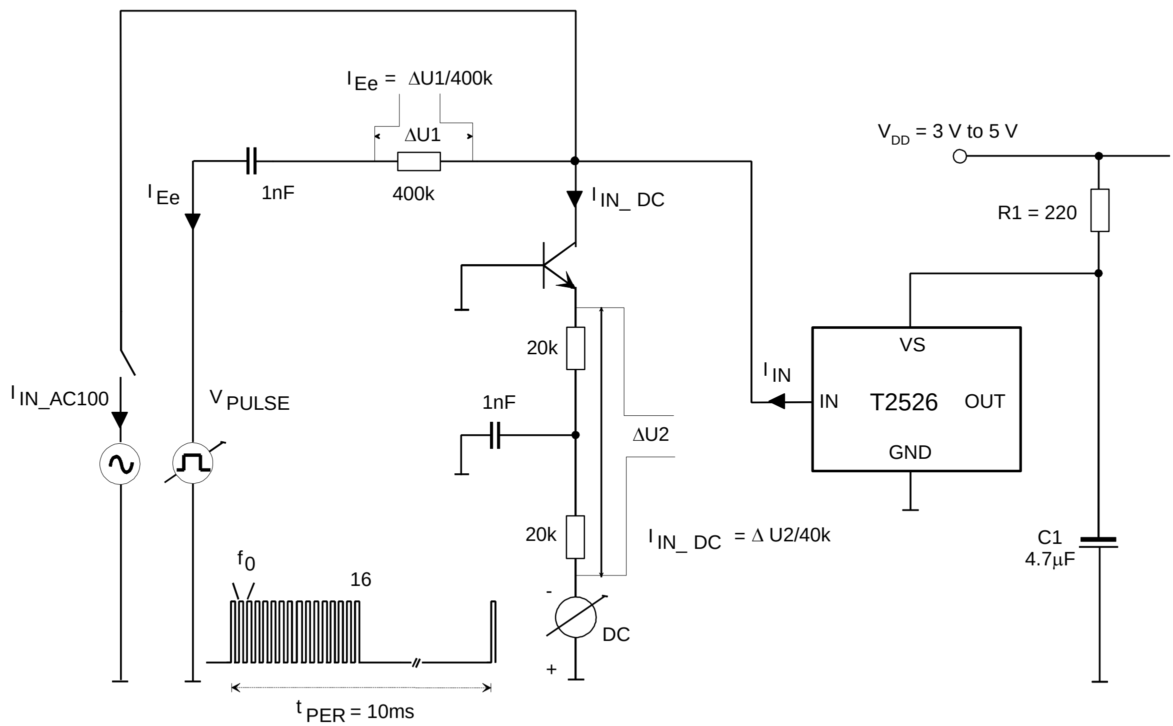
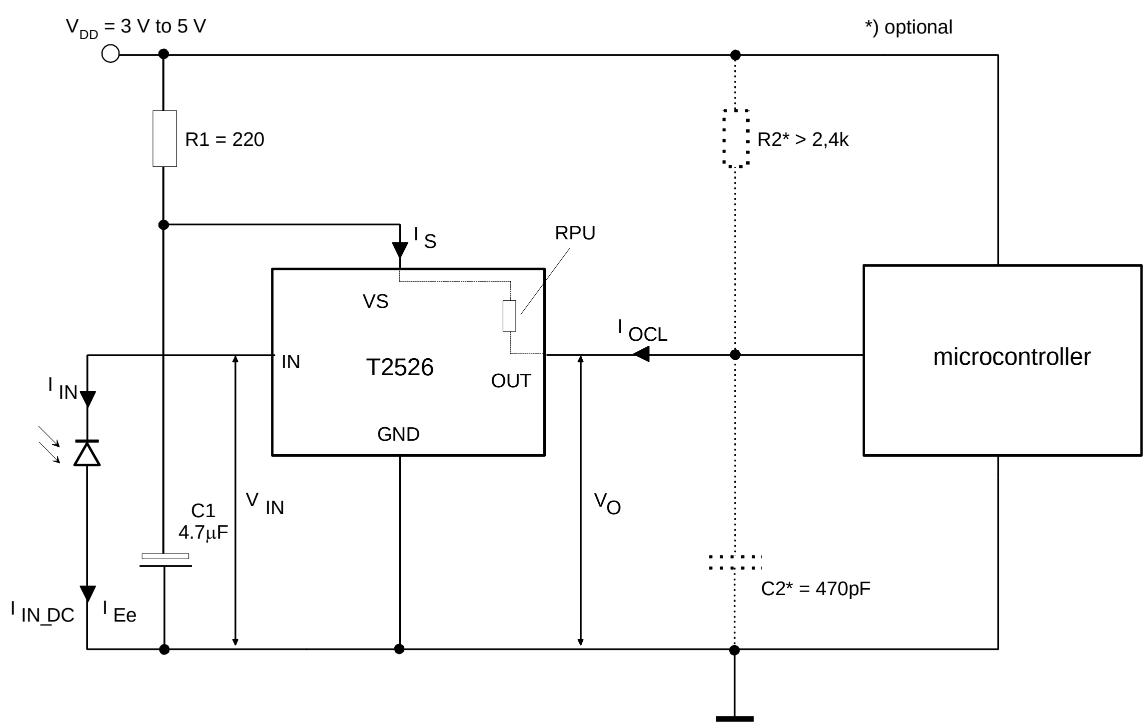
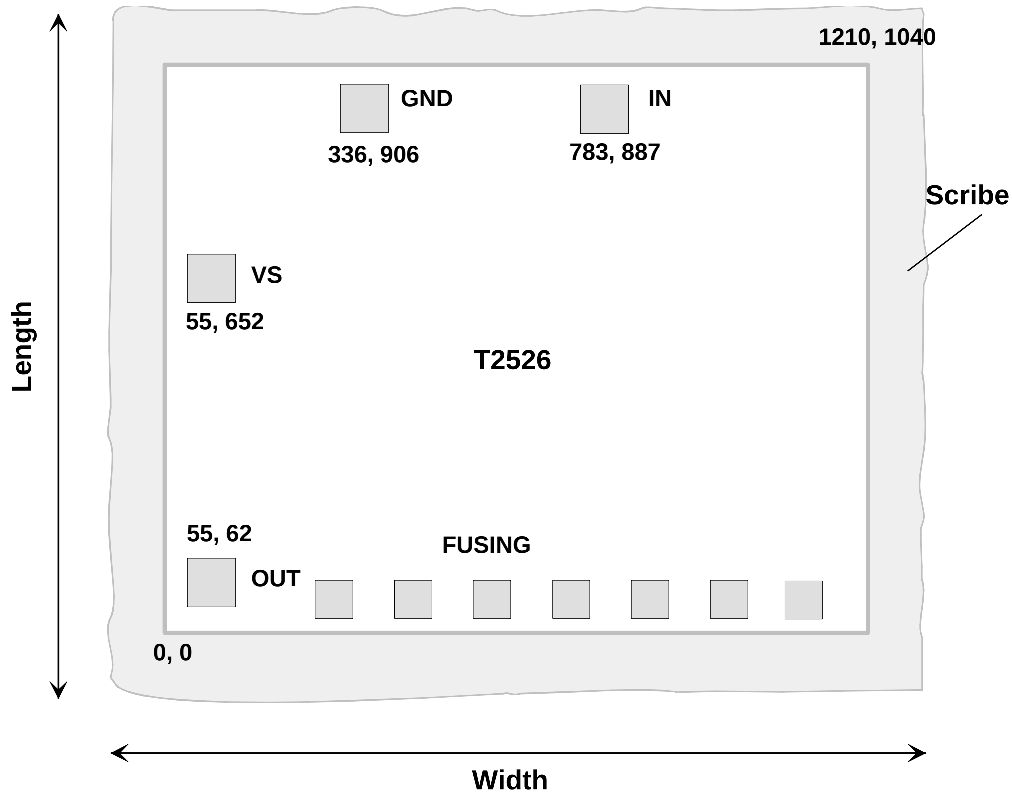


Figure 12. Application Circuit



Chip Dimensions

Figure 13. Chip Size in µm



Note: Pad coordinates are given for lower left corner of the pad in µm from the origin 0,0

Dimensions	Length inclusive scribe	1.16 mm
	Width inclusive scribe	1.37 mm
	Thickness	290 µ ± 5%
	Pads	90 µ x 90 µ
	Fusing pads	70 µ x 70 µ
Pad metallurgy	AlSiTi	
Finish	Si_3N_4 thickness 1.05 µm	

Ordering Information

Delivery: unsawn wafers (DDW) in box, SO8 (150 mil) and TSSOP8 (3 mm body).

Extended Type Number	PL[2)]	R_{PU}[3)]	D[4)]	Type
T2526N0xx[1)]-yyy[5)]	2	30	2179	**Standard type:** ≥ 10 pulses, enhanced sensibility, high data rate
T2526N1xx[1)]-DDW	1	30	2179	
T2526N2xx[1)]-yyy[5]	2	40	1404	**Lamp type:** ≥ 10 pulses, enhanced suppression of disturbances, secure data transmission
T2526N3xx[1)]-DDW	1	40	1404	
T2526N6xx[1)]-yyy[5]	2	30	3415	**Short burst type:** ≥ 6 pulses, enhanced data rate
T2526N7xx[1)]-DDW	1	30	3415	

Notes:
1. xx means the used carrier frequency value f_0 30, 33, 36, 38, 40, 44 or 56 kHz.(76 kHz type on request)
2. Two pad layout versions (see Figure 14 and Figure 15) available for different assembly demand
3. Integrated pull-up resistor at PIN OUT (see electrical characteristics)
4. Typical data transmission rate up to bit/s with f_0 = 56 kHz, V_S = 5 V (see Figure 10)
5. yyy means kind of packaging:
   ....DDW -> unsawn wafers in box
   ....6AQ -> (only on request, TSSOP8 taped and reeled)

Pad Layout

Figure 14. Pad Layout 1 (DDW only)

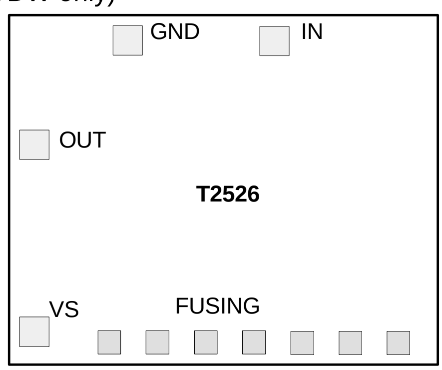
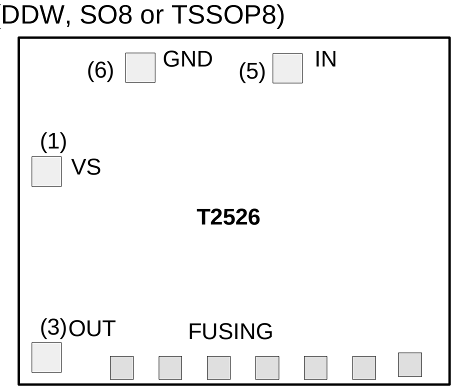


Figure 15. Pad Layout 2 (DDW, SO8 or TSSOP8)



Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

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Colorado Springs, CO 80906
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FAX 1(719) 540-1759

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FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
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FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

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Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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