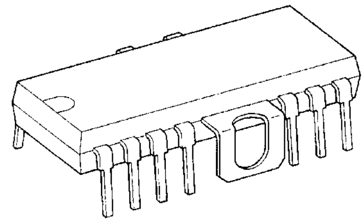
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA7289P,TA7289F

PWM STEPPING MOTOR DRIVER

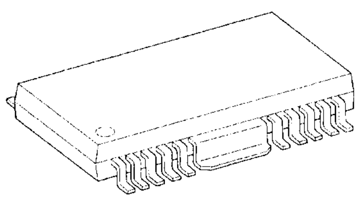
The TA7289P, TA7289F are PWM solenoid driver designed especially for use high efficiency stepping motor control.
It consist of 1.5A peak current drive capable output full bridge driver, oscillation circuit for PWM switching, 4bit D−A for output current control and TTL compatible input circuit.

TA7289P



HDIP14-P-500-2.54A

TA7289F



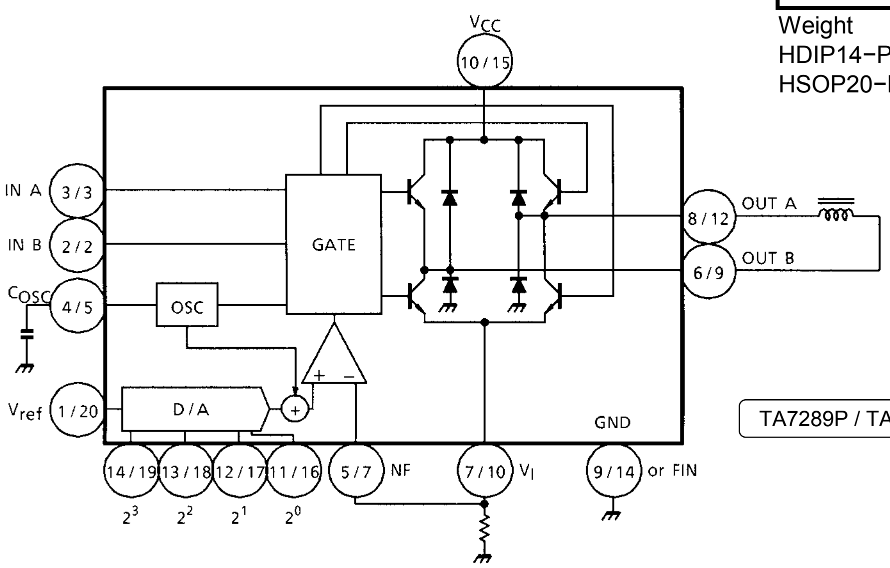
HSOP20-P-450-1.00

Weight
HDIP14−P−500−2.54A : 3.00g (Typ.)
HSOP20−P−450−1.00 : 0.79g (Typ.)

FEATURES

- Wide Range of Operating Voltage
  : $V_{CC\ (opr.)}$ Min. = 6~27 V
- High Current Capability: I_O Max = 1.5 A (PEAK)
- LS−TTL Compatible Control Inputs (IN A, IN B)
- Few External Components Required.
- Build−in 4bit DAC.

BLOCK DIAGRAM



TA7289P / TA7289F

Note: Pin (1), (4), (6), (8), (11) of TA7289F are all NC (Non−connection)

PIN FUNCTION

PIN No. P	PIN No. F	PIN SYMBOL	FUNCTIONAL DESCRIPTION	
1	20	V_{ref}	NF voltage supply input terminal	
2	2	IN B	Signal input terminal	Function
3	3	IN A	Signal input terminal	
4	5	C_{OSC}	Internal oscillation frequency input terminal	
5	7	NF	Output current detection terminal	
6	9	OUT B	Output B terminal	
7	10	V_I	Comparator input terminal	
8	12	OUT A	Output A terminal	
9	14	GND	GND terminal	
10	15	V_{CC}	Power voltage supply terminal	
11	16	2^0	D / A input terminal	
12	17	2^1	D / A input terminal	
13	18	2^2	D / A input terminal	
14	19	2^3	D / A input terminal	
FIN	FIN	GND	GND terminal	

Note: Pin (1), (4), (6), (8), (11) of TA7289F are all NC (Non−connection)

FUNCTION

IN A	IN B	OUT A	OUT B	MODE
L	L	OFF	OFF	STOP
H	L	H	L	CW / CCW
L	H	L	H	CCW / CW
H	H	OFF	OFF	STOP

INPUT CIRCUIT (IN A, IN B)

Input circuit is shown in Fig.1 IN A and IN B are TTL compatible “Low Active” type and have a hysteresis of 0.8 V Typ at $T_j = 25°C$.

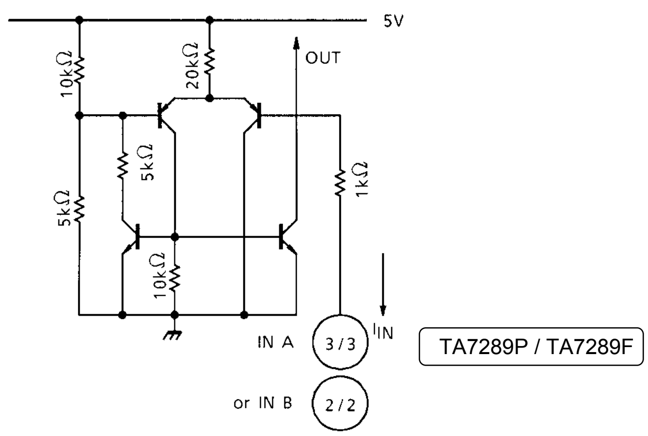


Fig. 1

D / A AND Vref CIRCUIT

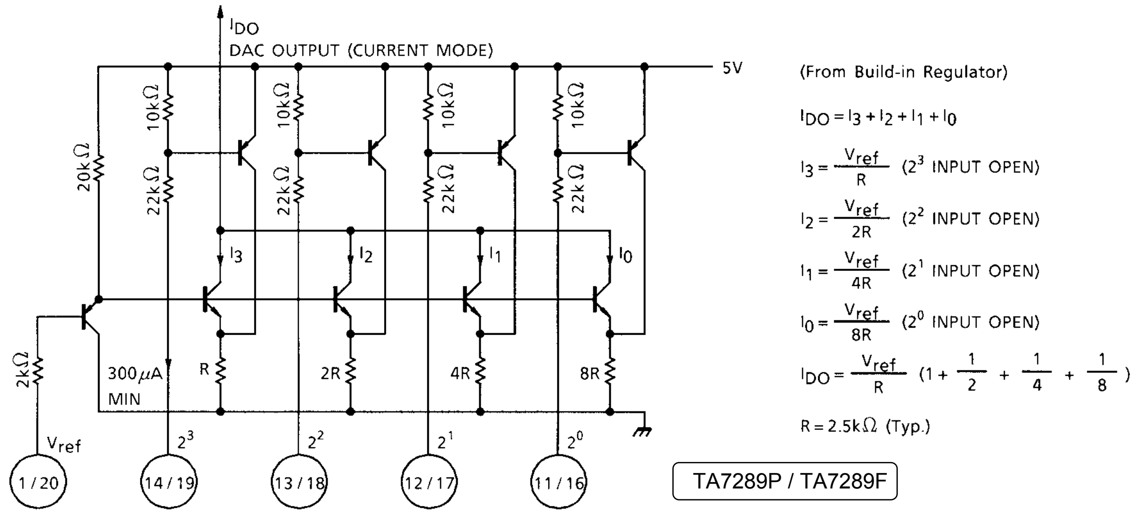


Fig. 2

I_{DO} of current mode DAC output is proportional to multipled voltage of V_{ref} (PIN (1) (or (20))) and DAC inputs. DAC inputs are all "low active" type and required input current of 300 μA MIN for each input terminal.

OSC AND COMPARATOR

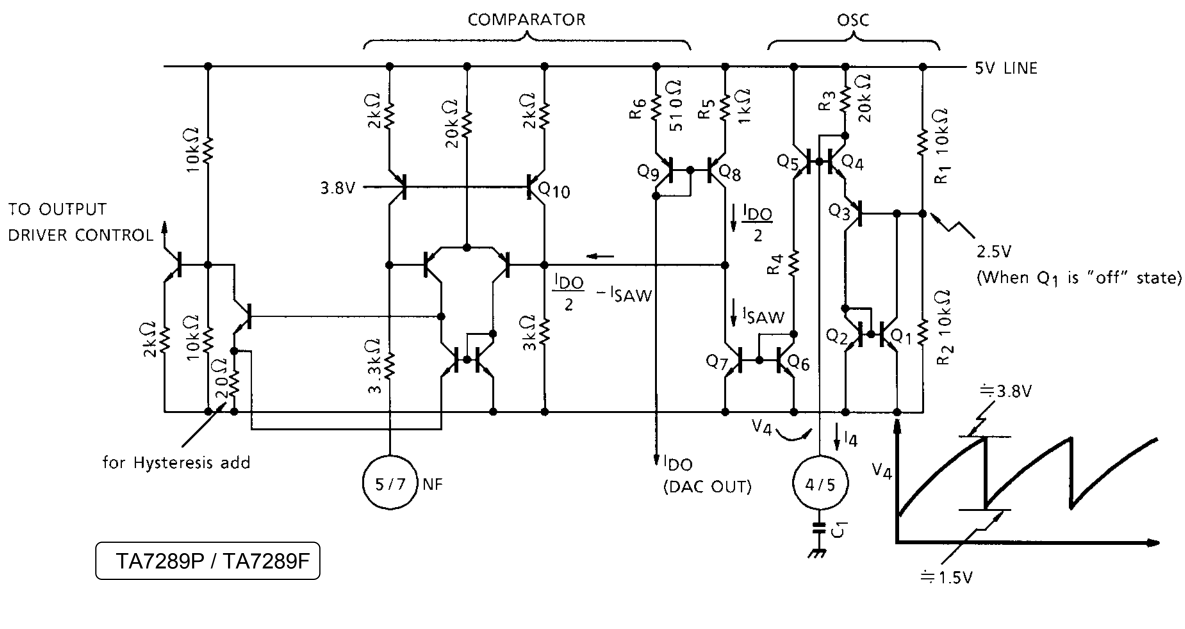


Fig. 3

Sawtooth OSC circuit consists of Q_1 through Q_4 and R_1 through R_3.
R_1 and R_2 are voltage divider of 5 V build−in regulator.
Q_1 is turned "off" when V_4 is less than the voltage of 2.5 V + V_{BE} Q_4 + V_{BE} Q_3 approximately equal to 3.8 V. V_4 is increased by C_1 charging of I_4. Q_1 and Q_2 are turned "ON" when V_4 becomes V_4 − H level.
Lower level of V_4 (V_4 − L) is equal to V_{BE} Q_4 + V_{BE} Q_3 + V_{SAT} Q_1 approximately equal to 1.5 V.
V_4 is calculated by following equation.

$$V_4 = 5 \cdot (1 - e - \frac{1}{C_1 \cdot R_3} \cdot t) \quad \text{.......... (1)}$$

Assuming that V_4 = 1.5 V (t = t_1) and=3.8 V (t = t_2).
C_1 is external capacitance connected to Pin (4) (or (5)) and R_3 is on−chip 20 kΩ resistor.
Therefore, OSC frequency is calculated as follows.

$$t_1 = -C_1 \cdot R_3 \cdot 1n\ (1 - \frac{1.5}{5}) \quad \text{.......... (2)}$$

$$t_2 = -C_1 \cdot R_3 \cdot 1n\ (1 - \frac{3.8}{5}) \quad \text{.......... (3)}$$

$$f_{OSC} = \frac{1}{t_1 - t_2} = \frac{1}{C_1 \cdot (R_3 \cdot 1n\ (1 - \frac{1.5}{5}) - R_3 \cdot 1n\ (1 - \frac{3.8}{5}))}$$

$$= \frac{1}{21.4\ C_1} \text{(kHz) (Unit of } C_1 \text{ is } \mu\text{F)}$$

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	30	V
		V_{ref}	30	
Reference Voltage		V_{IN}	7	
		V_I	2	
Output Current	TA7289P	$I_{O\ (MAX.)}$	1.5	A
	TA7289F		0.8	
	TA7289P	$I_{O\ (AVE.)}$	0.7	
	TA7289F		0.3	
Power Dissipation	TA7289P	PD (Note)	2.3	W
	TA7289F		1.0	
Operating Temperature		T_{opr}	−30~85	°C
Storage Temperature		T_{stg}	−55~150	°C

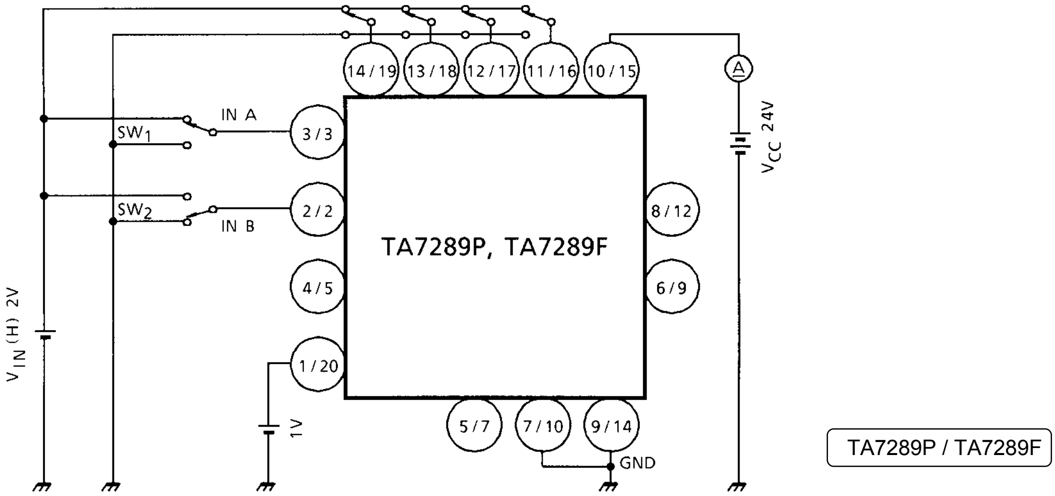
Note: NO HEAT SINK

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC} = 24 V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Quiescent Current	I_{CC1}	1	CW / CCW	Output : Open	12	20	30	mA
	I_{CC2}		STOP		12	20	30	
	I_{CC3}		CW / CCW mode, 2^0~2^3: H		12	20	30	
	I_{CC4}		CW / CCW mode, 2^0~2^3: L		13	23	32	
Output Voltage	$V_{IN\ (H)}$	2	IN A IN B, Source type.		2.0	—	7.0	V
	$V_{IN\ (L)}$				−0.4	—	0.8	
Input Hysteresis Width	ΔV_{IN}	2	—		—	0.8	—	V
Input Current	I_{IN1}	2	IN A, IN B V_{IN} = 0 V Source type		—	25	35	μA
	I_{IN2}		2^0, 2^1, 2^2, 2^3 V_{IN} = 0 V Source type		90	160	200	
Output Saturation Voltage	$V_{SAT\ U-1}$	3	I_{OUT} = 0.2 A		—	1.1	1.5	V
	$V_{SAT\ L-1}$				—	0.8	1.1	
	$V_{SAT\ U-2}$		I_{OUT} = 0.7 A		—	1.2	1.7	
	$V_{SAT\ L-2}$				—	0.9	1.3	
	$V_{SAT\ U-3}$		I_{OUT} = 1.5 A		—	1.8	2.6	
	$V_{SAT\ L-3}$				—	1.2	1.9	
Control Supply Voltage	V_{ref}	—	—		GND	—	2.0	V
Control Supply Current	I_{ref}	2	V_{ref} = 0~2.0 V		—	25	35	μA
Diode Forward Voltage	V_{FU}	4	I_F = 1.5 A		—	2.6	3.3	V
	V_{FL}				—	0.8	1.1	
Output Leakage Current	I_{L-U}	5	V_L = 30 V		—	—	50	μA
	I_{L-L}		V_L = 30 V		—	—	50	
NF Terminal Current	I_{NF}	6	Source type V_{NF} = 0~2.0 V T_j = 0~125°C		180	300	490	μA
Internal Supply Output Voltage	V_{CC2}	6	—		—	5	—	V
Resistor for Oscillation (R3)	R_{OSC}	6	T_j = 0~125°C		13	20	32	kΩ

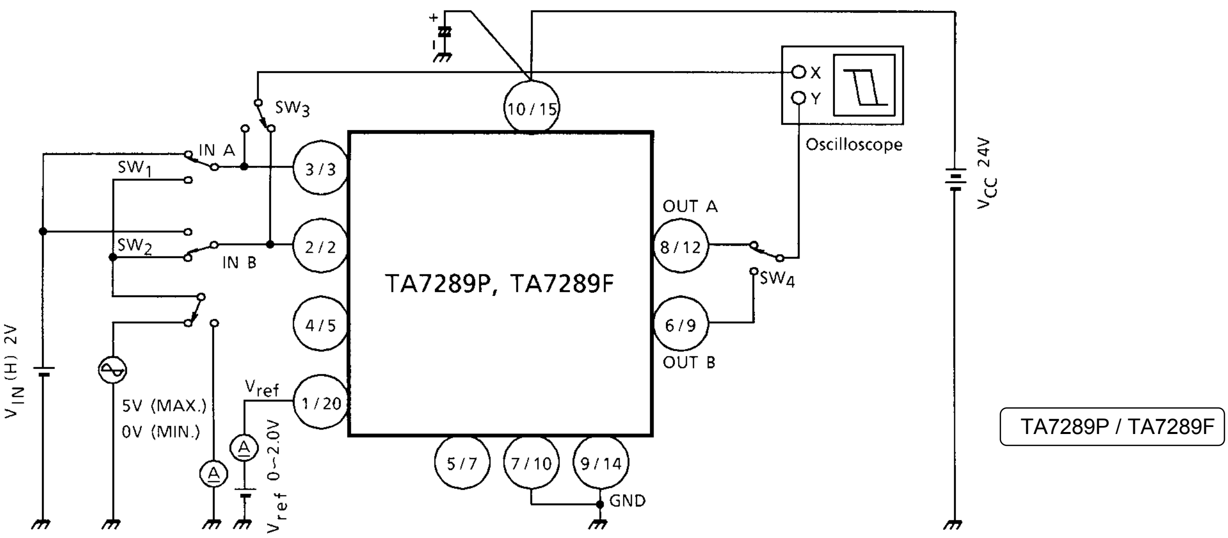
TEST CIRCUIT 1

$I_{CC1,\,2,\,3,\,4}$



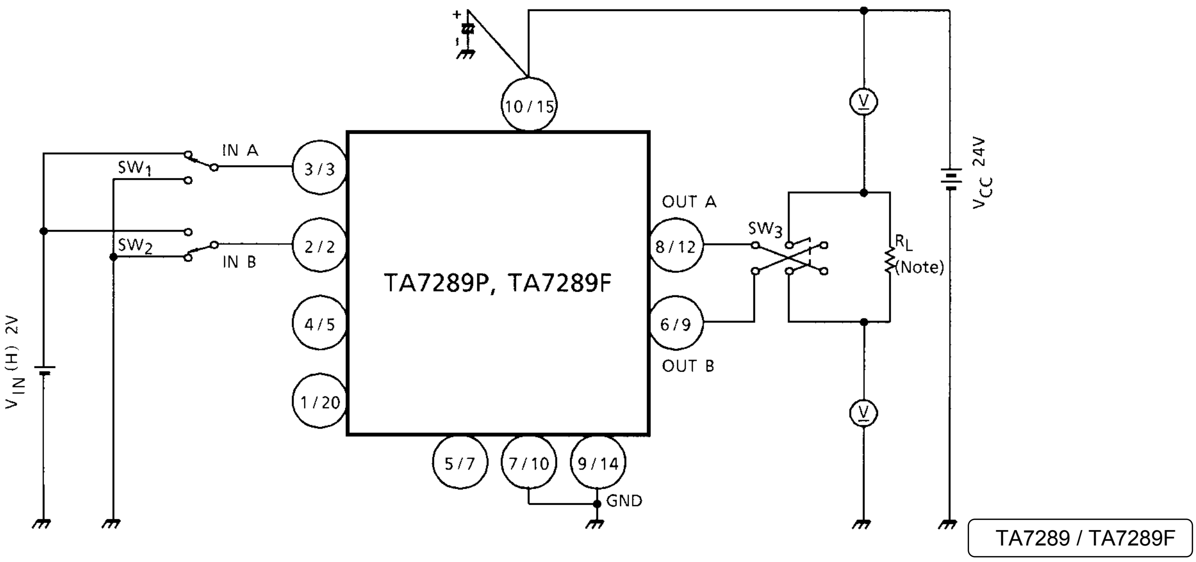
TEST CIRCUIT 2

$V_{IN\,(H),\,(L)}$, $I_{IN1,\,2}$, ΔV_{IN}, I_{ref}



TEST CIRCUIT 3

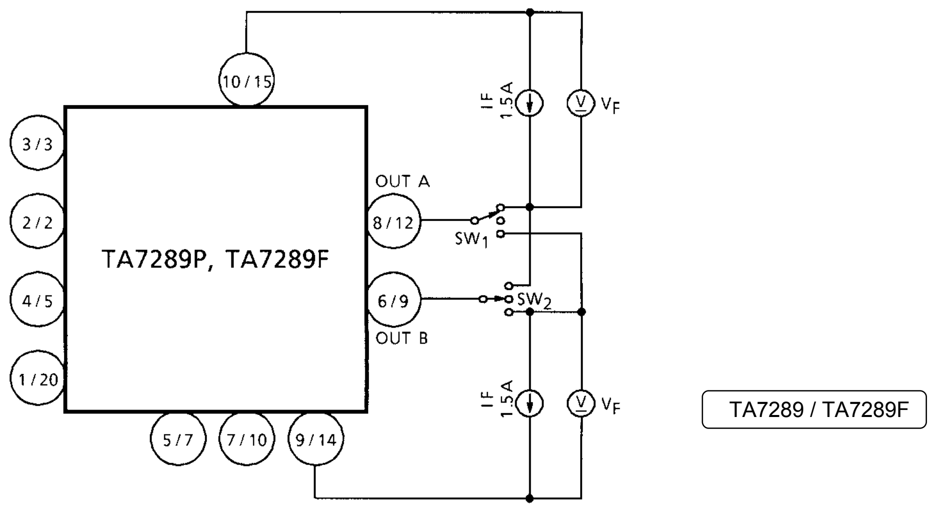
V_{SAT} U1, L1, U2, L2, U3, L3



Note: Calibrate I_{OUT} to 0.2A / 0.7A / 1.5A by R_L

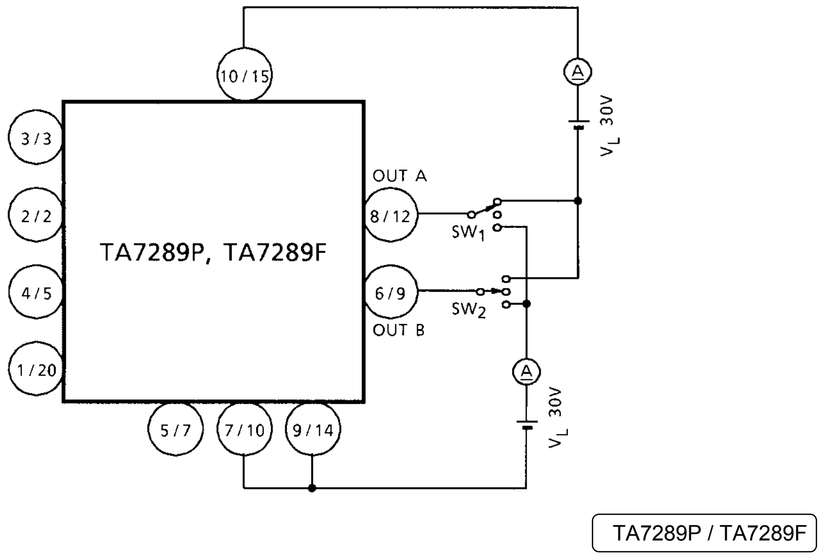
TEST CIRCUIT 4

V_{FU}, V_{FL}



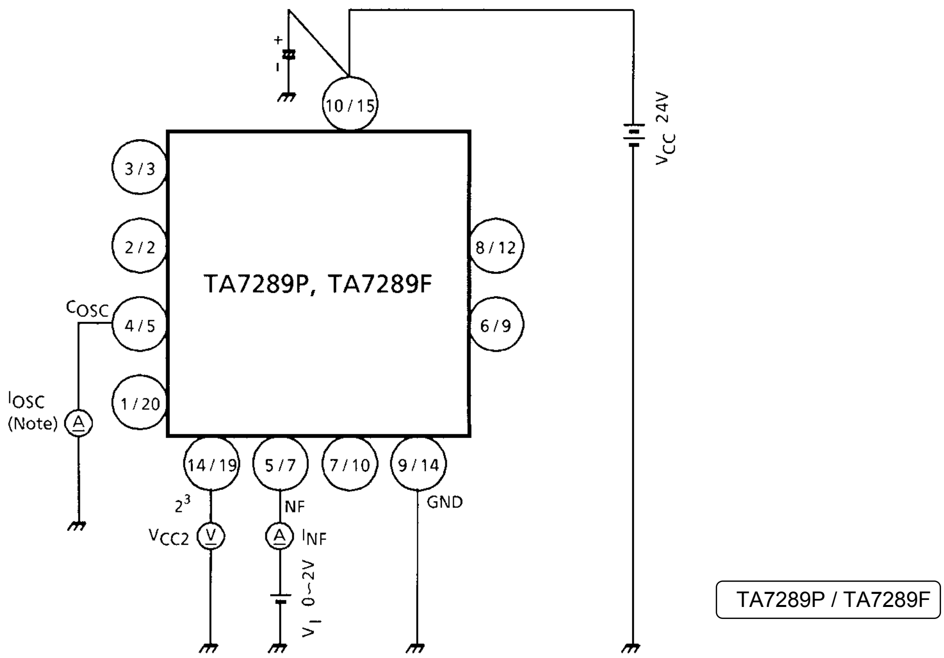
TEST CIRCUIT 5

I_{L-U}, I_{L-L}



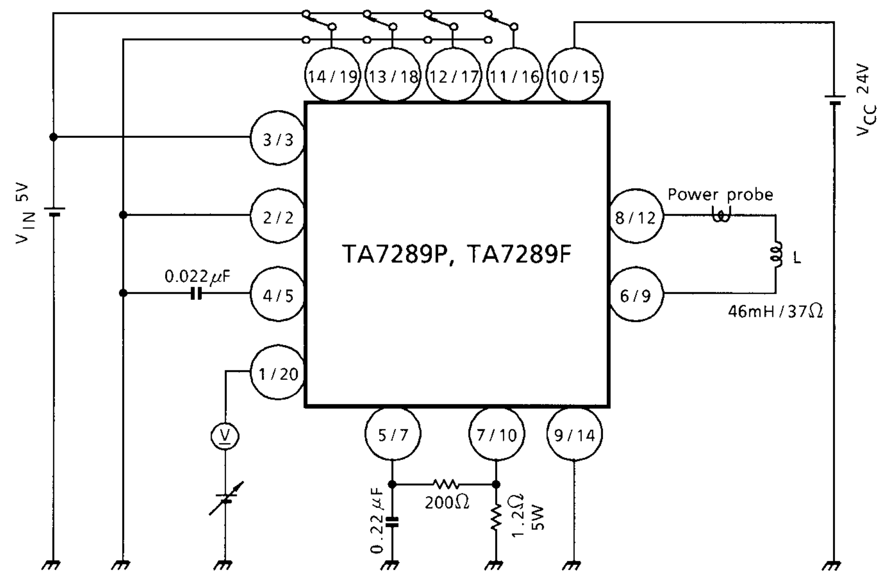
TEST CIRCUIT 6

I_{NF}, V_{CC2}, R_{OSC}



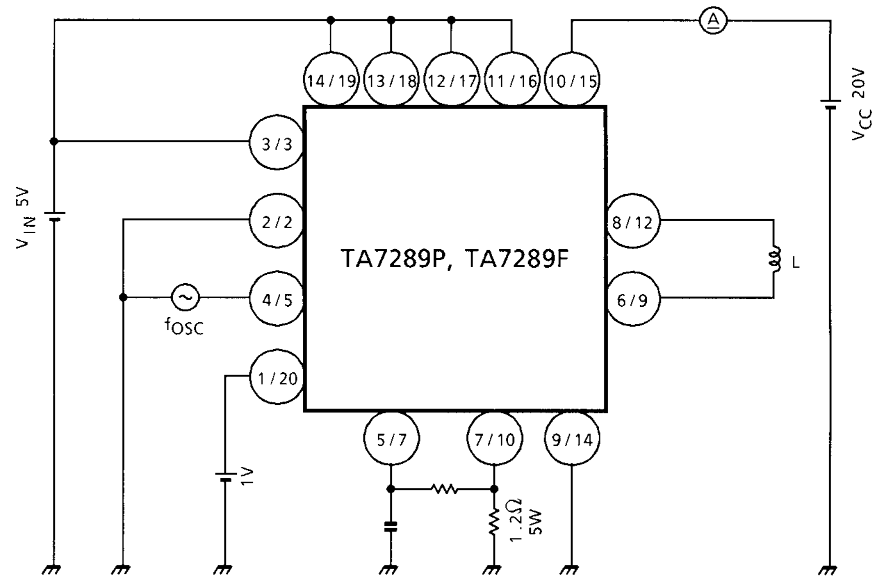
Note: $R_{OSC} = \frac{V_{CC2}\,(V)}{I_{OSC}\,(A)}\ (\Omega)$

TEST CIRCUIT 7
I_{OUT} – V_{ref} CHARACTERISTIC, I_{OUT} – D / A CHARACTERISTIC

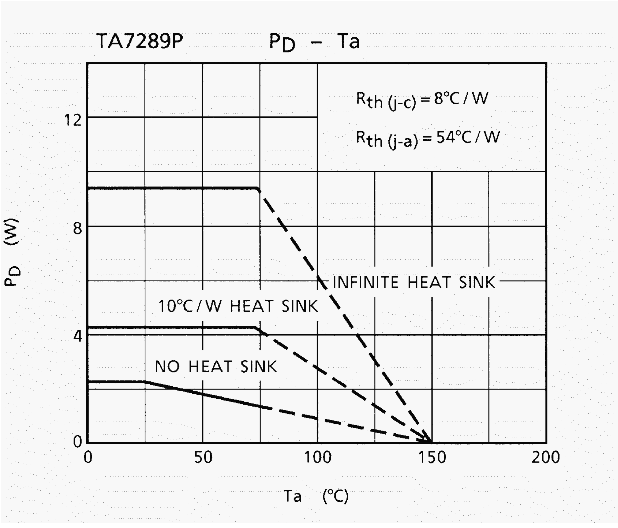


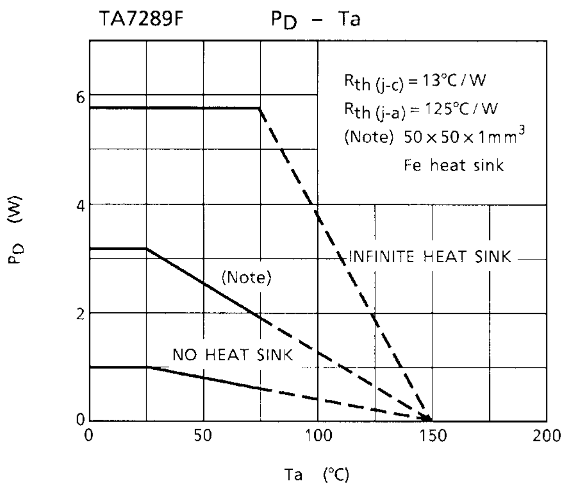
TA7289P / TA7289F

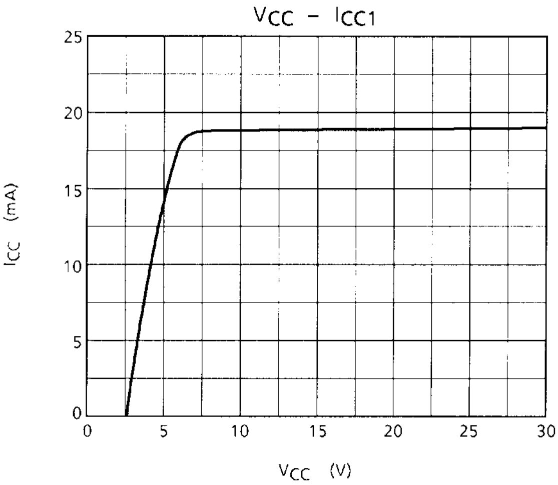
TEST CIRCUIT 8
I_{CC} – FREQUENCY CHARACTERISTIC

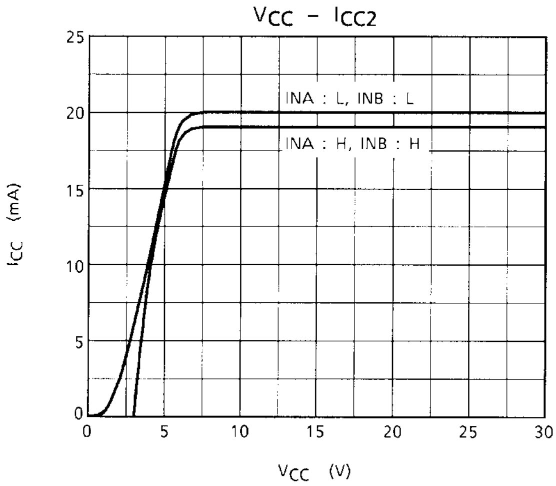


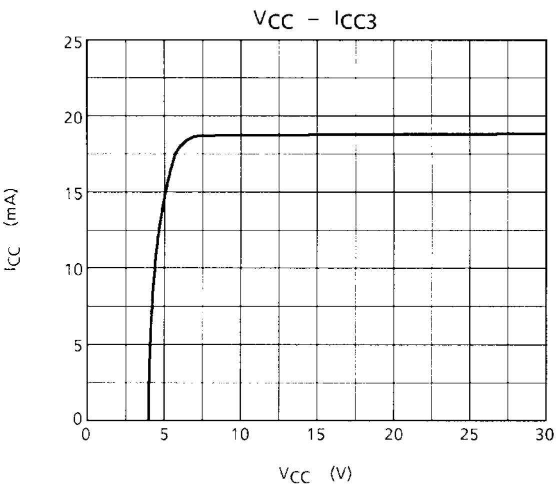
TA7289P / TA7289F

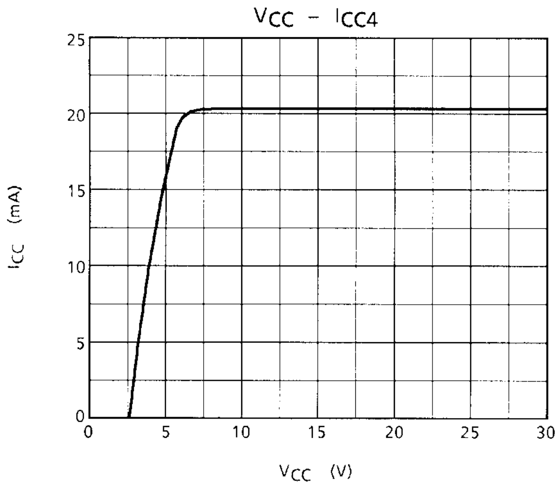

TA7289P
PD – Ta
Rth (j-c) = 8°C / W
Rth (j-a) = 54°C / W
INFINITE HEAT SINK
10°C / W HEAT SINK
NO HEAT SINK
PD (W)
Ta (°C)

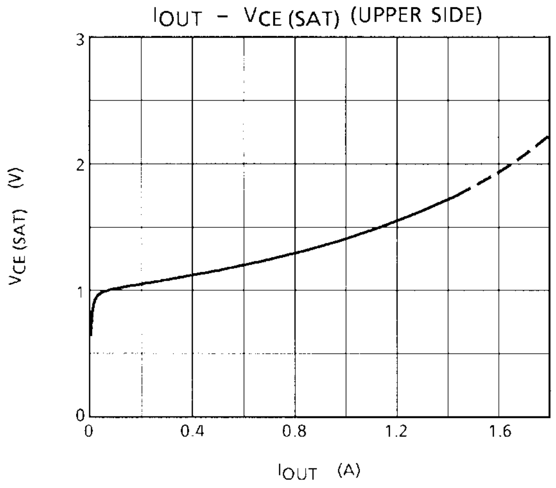

TA7289F
PD – Ta
Rth (j-c) = 13°C / W
Rth (j-a) = 125°C / W
(Note) 50 × 50 × 1mm3
Fe heat sink
INFINITE HEAT SINK
(Note)
NO HEAT SINK
PD (W)
Ta (°C)

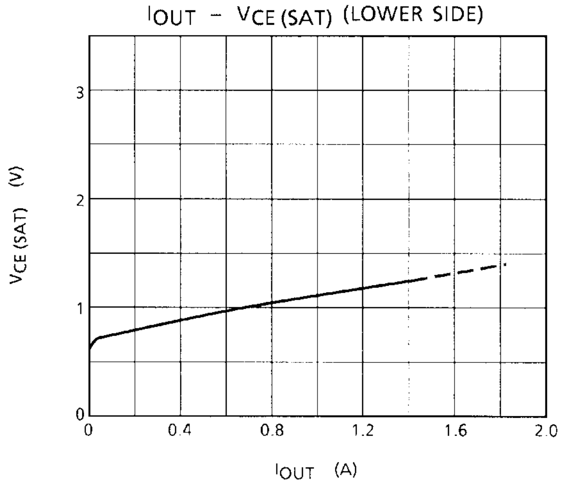

VCC – ICC1
ICC (mA)
VCC (V)

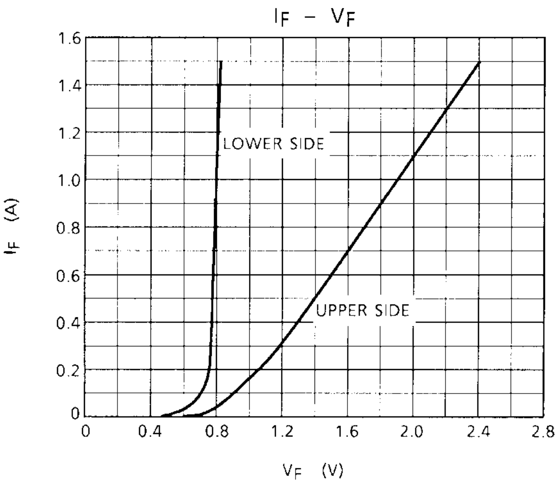

VCC – ICC2
INA : L, INB : L
INA : H, INB : H
ICC (mA)
VCC (V)

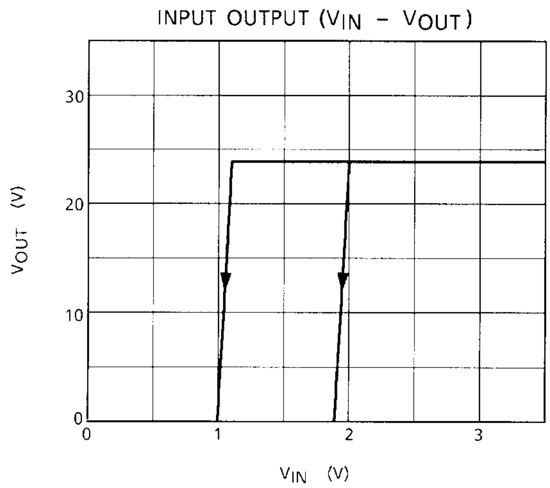

VCC – ICC3
ICC (mA)
VCC (V)

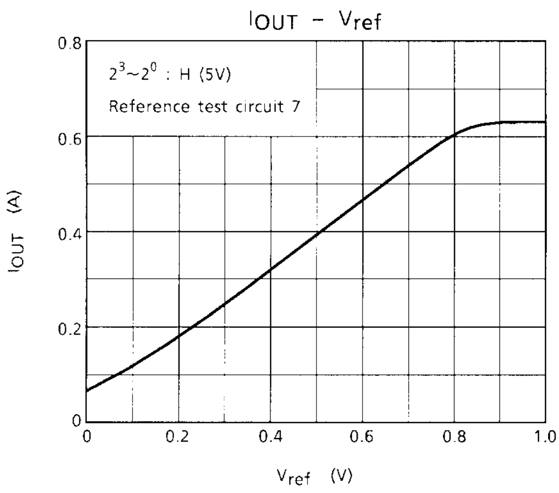

VCC – ICC4
ICC (mA)
VCC (V)

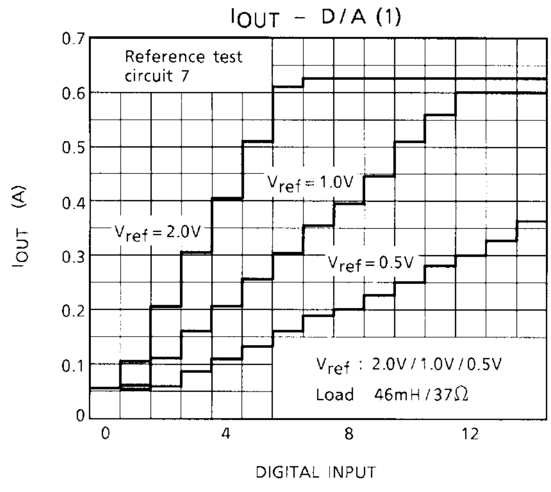

IOUT – VCE (SAT) (UPPER SIDE)
VCE (SAT) (V)
IOUT (A)

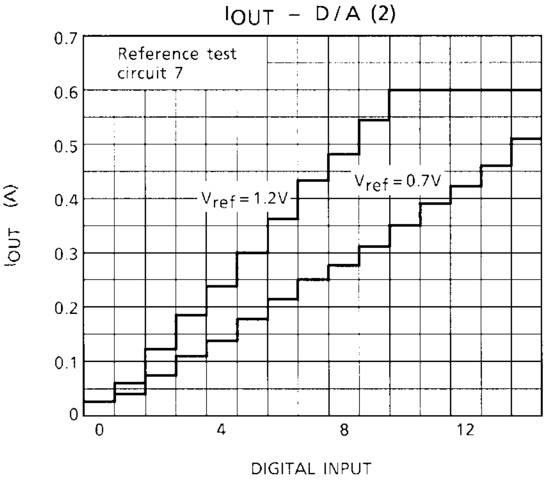

IOUT – VCE (SAT) (LOWER SIDE)
VCE (SAT) (V)
IOUT (A)

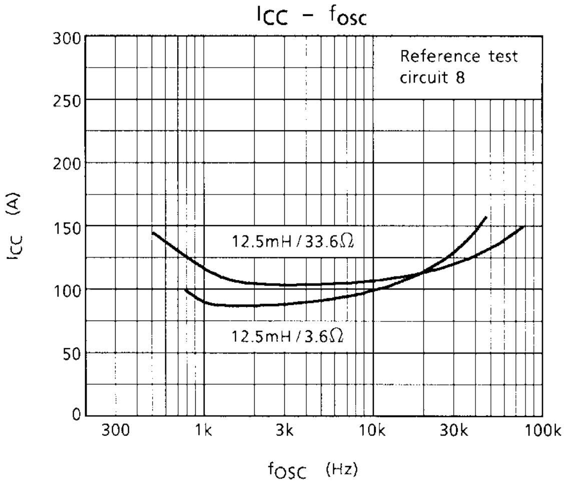

IF – VF
LOWER SIDE
UPPER SIDE
IF (A)
VF (V)


INPUT OUTPUT (VIN – VOUT)
VOUT (V)
VIN (V)

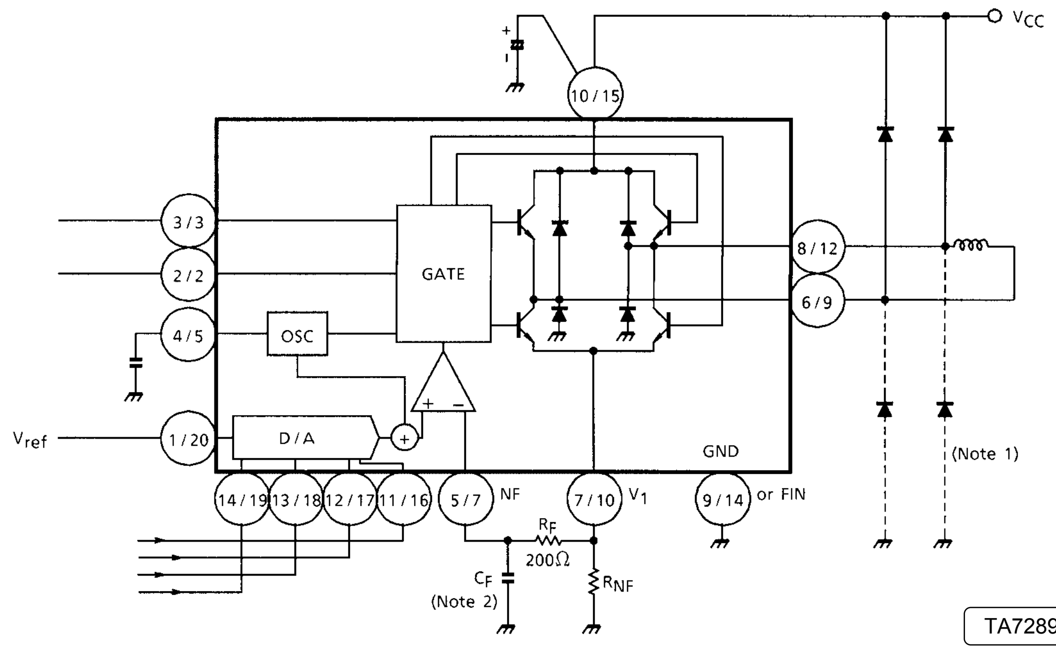

IOUT – Vref
2^3~2^0 : H (5V)
Reference test circuit 7
IOUT (A)
Vref (V)


IOUT – D/A (1)
Reference test circuit 7
Vref = 1.0V
Vref = 2.0V
Vref = 0.5V
Vref : 2.0V / 1.0V / 0.5V
Load 46mH / 37Ω
IOUT (A)
DIGITAL INPUT





APPLICATION CIRCUIT 1



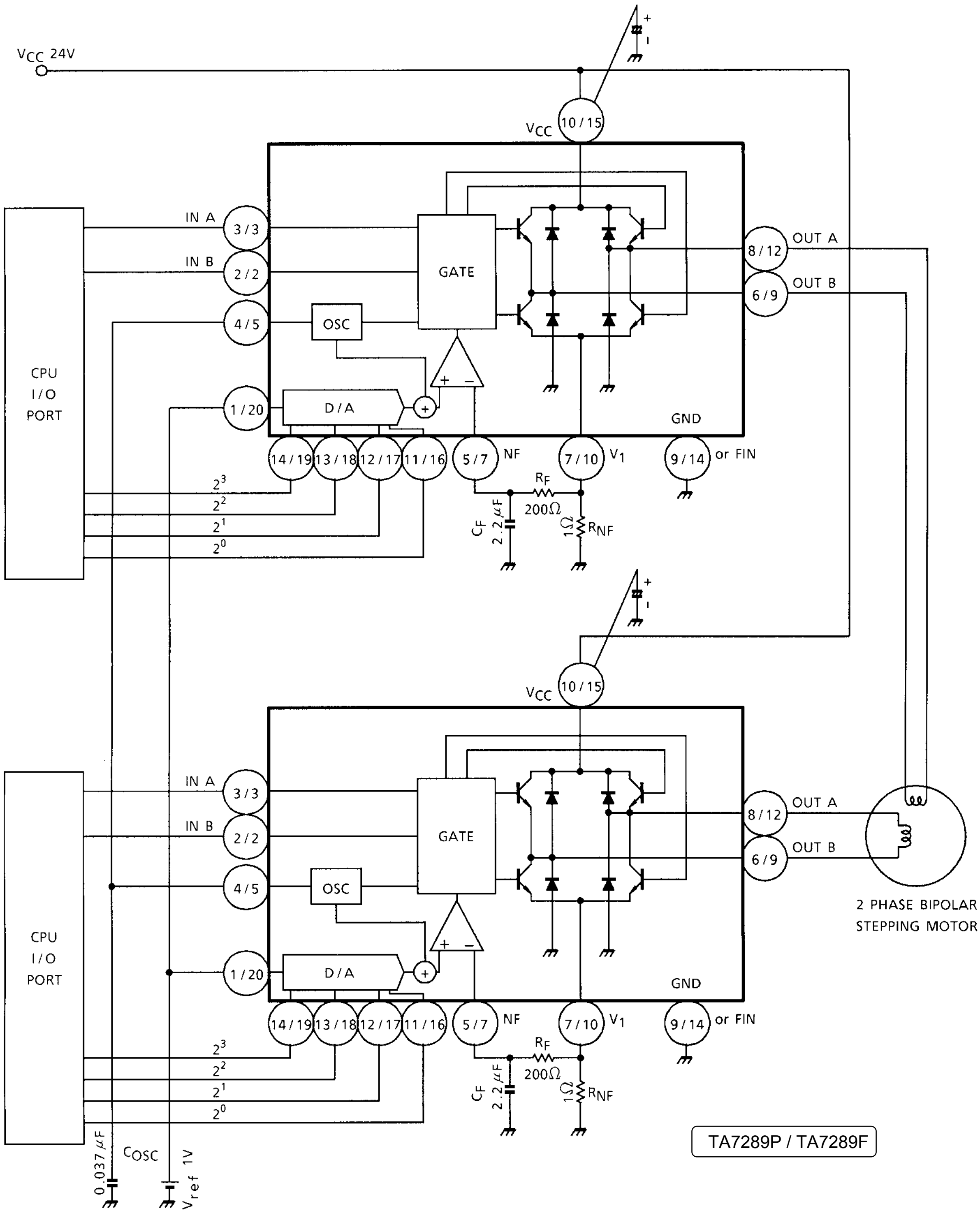
TA7289P / TA7289F

Note 1: Connect if required.

Note 2: Recommended R_F value is approximately 200 Ω.
And C_F value is concerned with the OSC frequency.
We recommend to select optimum value of C_F under the experimental consideration of noise cutting and time delay characteristics.

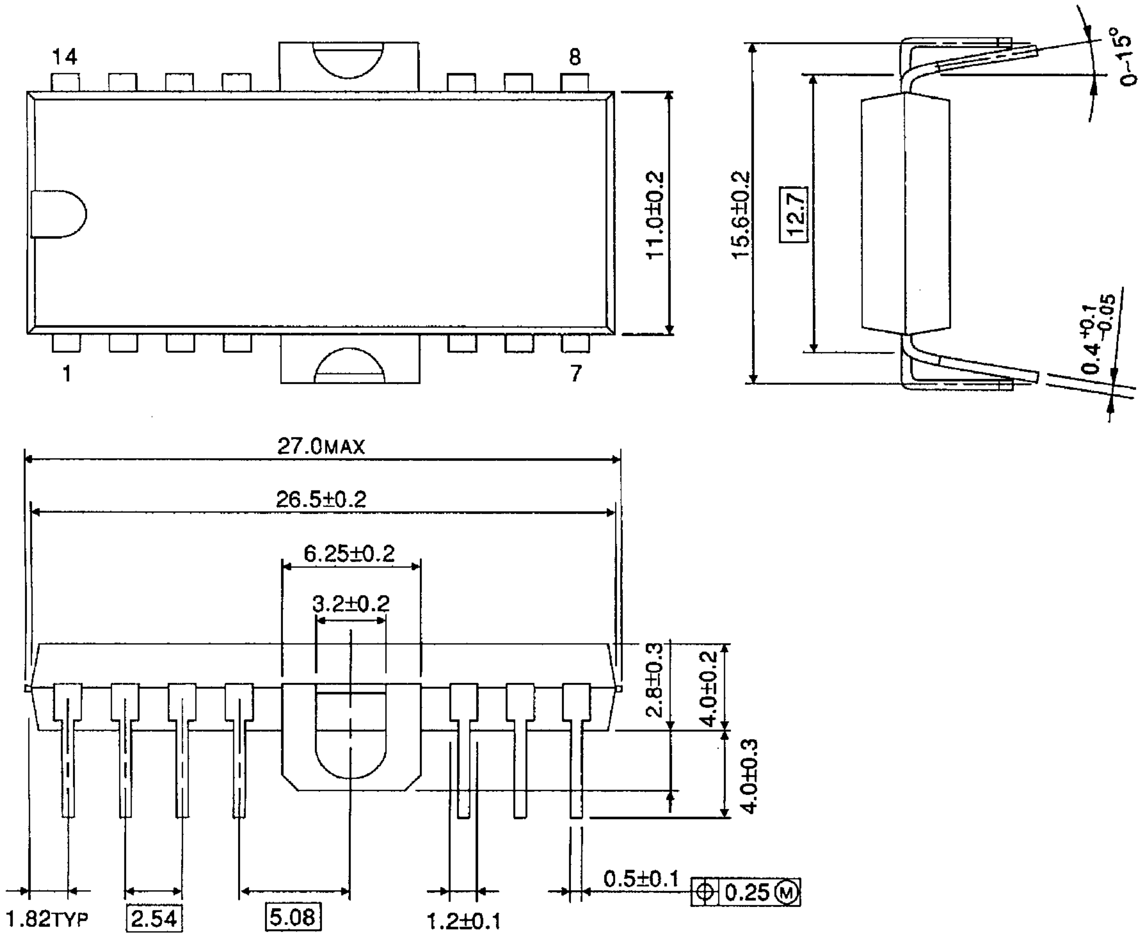
Note 3: Utmost care is necessary in the design of the output line, V_{CC} and GND line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

APPLICATION CIRCUIT 2 (PWM chopper stepping motor driver)



PACKAGE DIMENSIONS

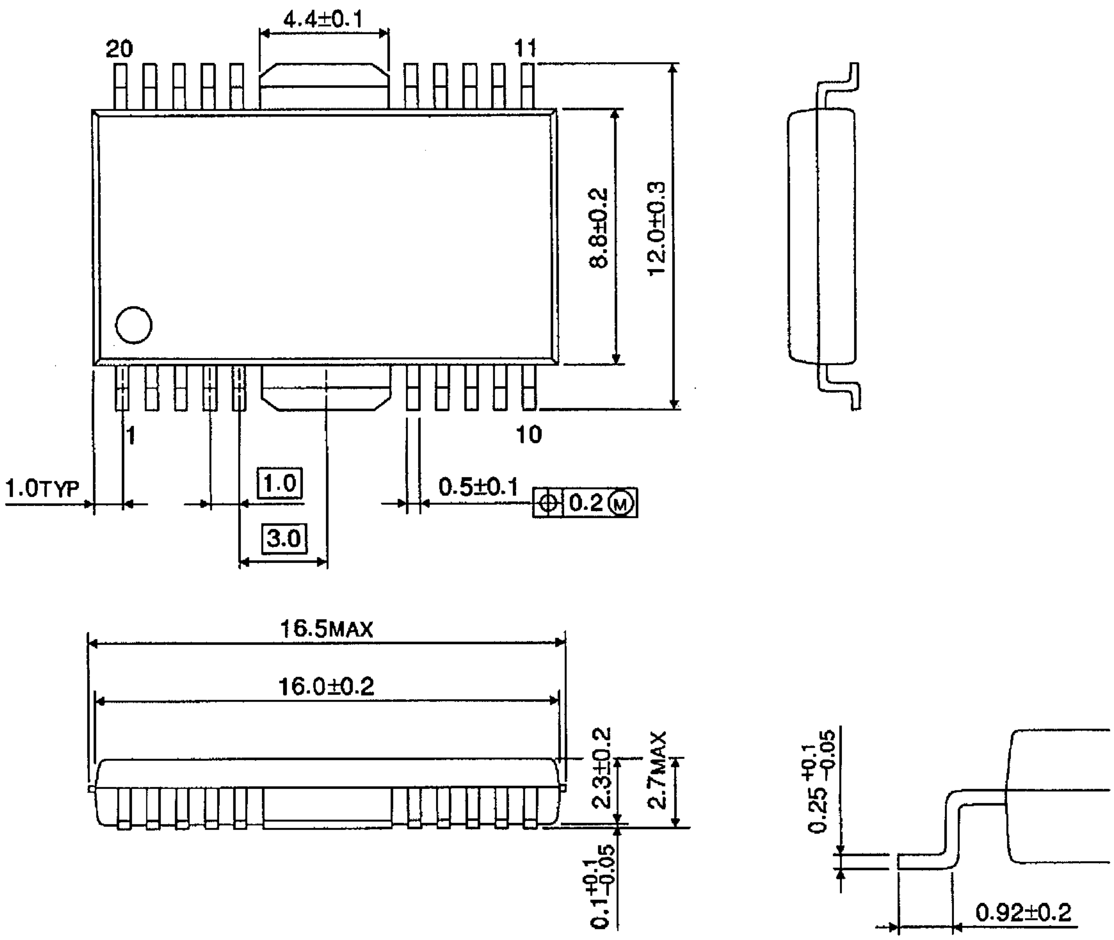
HDIP14−P−500−2.54A Unit: mm



Weight: 3.00 g (Typ.)

PACKAGE DIMENSIONS

HSOP20−P−450−1.00 Unit: mm



Weight: 0.79 g (Typ.)

RESTRICTIONS ON PRODUCT USE