TAFE1040
3 V, 10-BIT 42 MSPS, AREA CCD ANALOG FRONT-END

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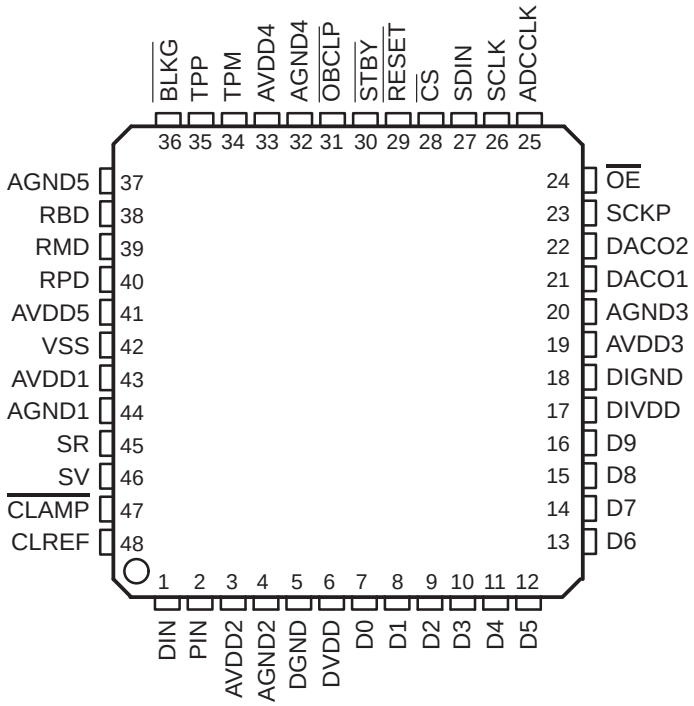
features

- Single-Chip CCD Analog Front-End
- 10-Bit, 42 MSPS, A/D Converter
- Single 3-V Supply Operation
- Programmable Timing Signal Delays
- Low Power: 180 mW Typ, 2-mW Power-down Mode
- Differential Nonlinearity Error
  – <±0.6 LSB Typ
- Integral Nonlinearity Error
  – <±1.5 LSB Typ
- Programmable Gain Amplifier (PGA) With 0 dB to 36 dB Gain Range (0.045 dB/Step)
- Automatic or Programmable Black Level and Offset Calibration With Digital Filter and Bad Pixel Limits
- Additional DACs for External Analog Setting
- Serial Interface for Register Configuration
- Internal Reference Voltages
- 48-Pin TQFP Package

applications

- Video Camcorde
- Digital Still Camera

PFB PACKAGE
(TOP VIEW)



description

The TAFE1040 is a complete area CCD analog front-end/digitizer designed for digital camera applications. The TAFE1040 performs all the analog processing functions necessary to maximize the dynamic range, corrects various errors associated with the CCD sensor, and then digitizes the results with an on-chip high-speed analog-to-digital converter (ADC). The key components of the TAFE1040 include: input clamp circuitry for the CCD and analog video signals, a correlated double sampler (CDS), a programmable gain amplifier (PGA) with 0 dB to 36 dB gain range, two internal digital-to-analog converters (DAC) for automatic or programmable optical black level and offset calibration, a 10-bit, 42 MSPS pipeline ADC, a parallel data port for easy microprocessor interface and a serial port for configuring internal control registers, two additional DACs for external system control, and internal reference voltages.

Designed in advanced CMOS process, the TAFE1040 operates from a single 3-V power supply with a normal power consumption of 180 mW at 42 MSPS and a 2-mW power-down mode.

Very high throughput rate, single 3 V operation, low power consumption, and fully integrated analog processing circuitry make the TAFE1040 an ideal area CCD signal processing solution for the high-resolution digital camera and camcorder applications.

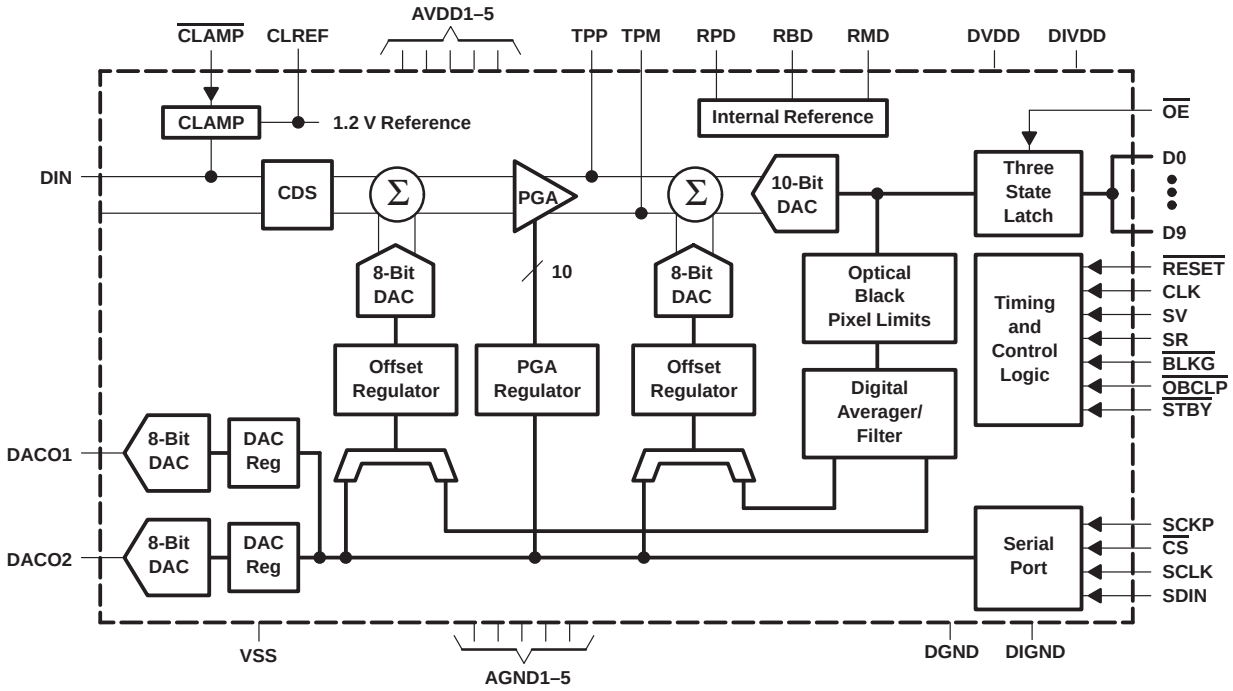
The part is available in a 48-pin TQFP package and is specified over –20°C to 75°C operating temperature range.

PRODUCT PREVIEW

AVAILABLE OPTIONS

T_A	PACKAGE DEVICES
	TQFP (PFB)
–20°C to 75°C	TAFE1040CPFB

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADCCLK	25	I	ADC clock input
DGND	5		Digital ground
AGND1	44		Analog ground for internal CDS circuits
AGND2	4		Analog ground for internal PGA circuits
AGND3	20		Analog ground for internal DAC circuits
AGND4	32		Analog ground for internal ADC circuits
AGND5	37		Analog ground for internal REF circuits
AVDD1	43		Analog supply voltage for internal CDS circuits, 3 V
AVDD2	3		Analog supply voltage for internal PGA circuits, 3 V
AVDD3	19		Analog supply voltage for internal DAC circuits, 3 V
AVDD4	33		Analog supply voltage for internal ADC circuits, 3 V
AVDD5	41		Analog supply voltage for internal ADC circuits, 3 V
$\overline{\text{BLKG}}$	36	I	Control input. The CDS operation is disabled when the BLKG is pulled low.
$\overline{\text{CLAMP}}$	47	I	CCD signal clamp control input
CLREF	48	O	Clamp reference voltage output
$\overline{\text{CS}}$	28	I	Chip select. A logic low on this input enables the TLV097A.
DACO1	21	O	Digital-to-analog converter output1
DACO2	22	O	Digital-to-analog converter output2
DIGND	18		Digital interface circuit ground
DIN	1	I	Input signal from CCD
DIVDD	17		Digital interface circuit supply voltage, 1.8 V–4.4 V
DVDD	6		Digital supply voltage, 3 V
D0–D9	7–16	O	10-Bit 3-state ADC output data or offset DACs test data
$\overline{\text{OBCLP}}$	31	I	Optical black level and offset calibration control input. Active low
$\overline{\text{OE}}$	24	I	Output data enable. Active low
PIN	2	I	Input signal from CCD
RBD	38	O	Internal bandgap reference for external decoupling
$\overline{\text{RESET}}$	29	I	Hardware reset input, active low. This signal forces a reset of all internal registers.
RMD	39	O	REF– output for external decoupling
RPD	40	O	Ref+ output for external decoupling
SCKP	23	I	This pin selects the polarity of SCLK. 0 – active low (high when SCLK is not running), 1 – active high (low when SCLK is not running)
SCLK	26	I	Serial clock input. This clock synchronizes the serial data transfer.
SDIN	27	I	Serial data input to configure the internal registers
SR	45	I	CCD reference level sample clock input
$\overline{\text{STDY}}$	30	I	Hardware power-down control input, active low
SV	46	I	CCD signal level sample clock input
TPM	34	O	Mux'ed test output: PGA noninverting output or inverted PGA clock
TPP	35	O	Mux'ed test output: PGA inverting output or inverted CDS clock
VSS	42		Silicon substrate, normally connected to analog ground

PRODUCT PREVIEW

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