

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

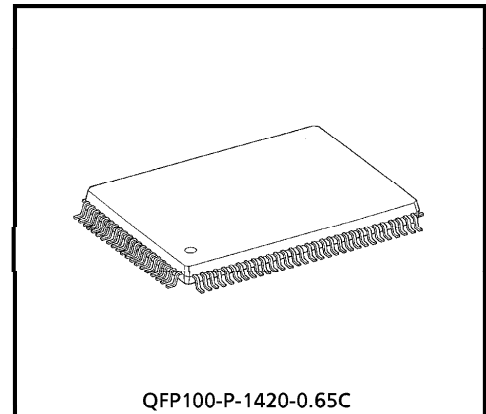
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64BIT SHIFT REGISTER / LATCH DRIVER

The TB62600F is specifically designed for 64bit Thermal Head drivers. And this IC is monolithic integrated circuits designed to be used together with Bi-CMOS (DMOS) integrated circuit. The devices consist of a 64bit shift register, dual 64bit latches, and 64 output DMOS structures.

FEATURE

- Built-in selection circuit : parallel-in parallel-out (8×8) or serial-in parallel-out (1×64)
- CMOS compatible inputs
- Open-drain DMOS outputs
- Low steady-state power consumption
- Built-in mono stable multi-vibrator for head protection
- Package : QFP100-P-1420C

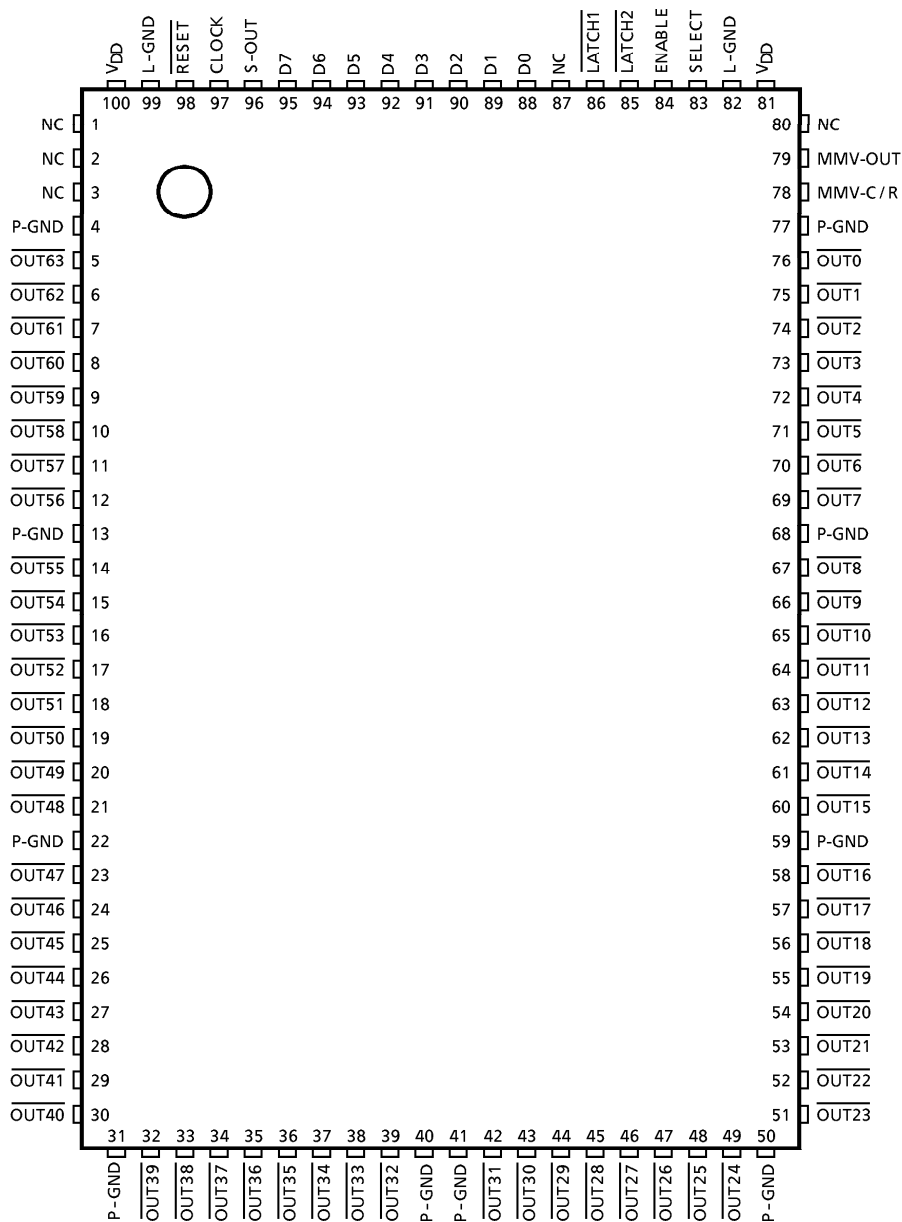


QFP100-P-1420-0.65C
Weight : 1.6g (Typ.)

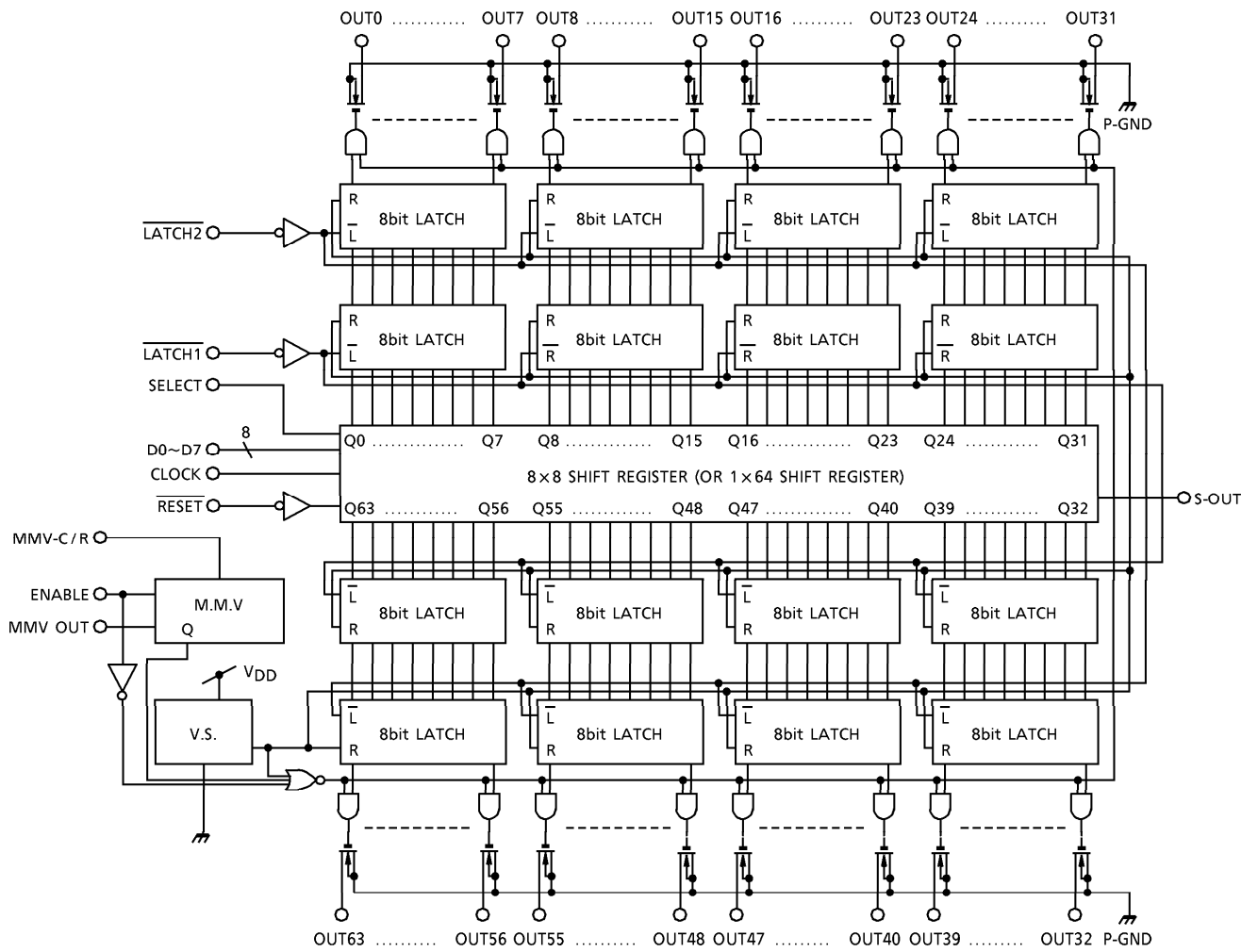
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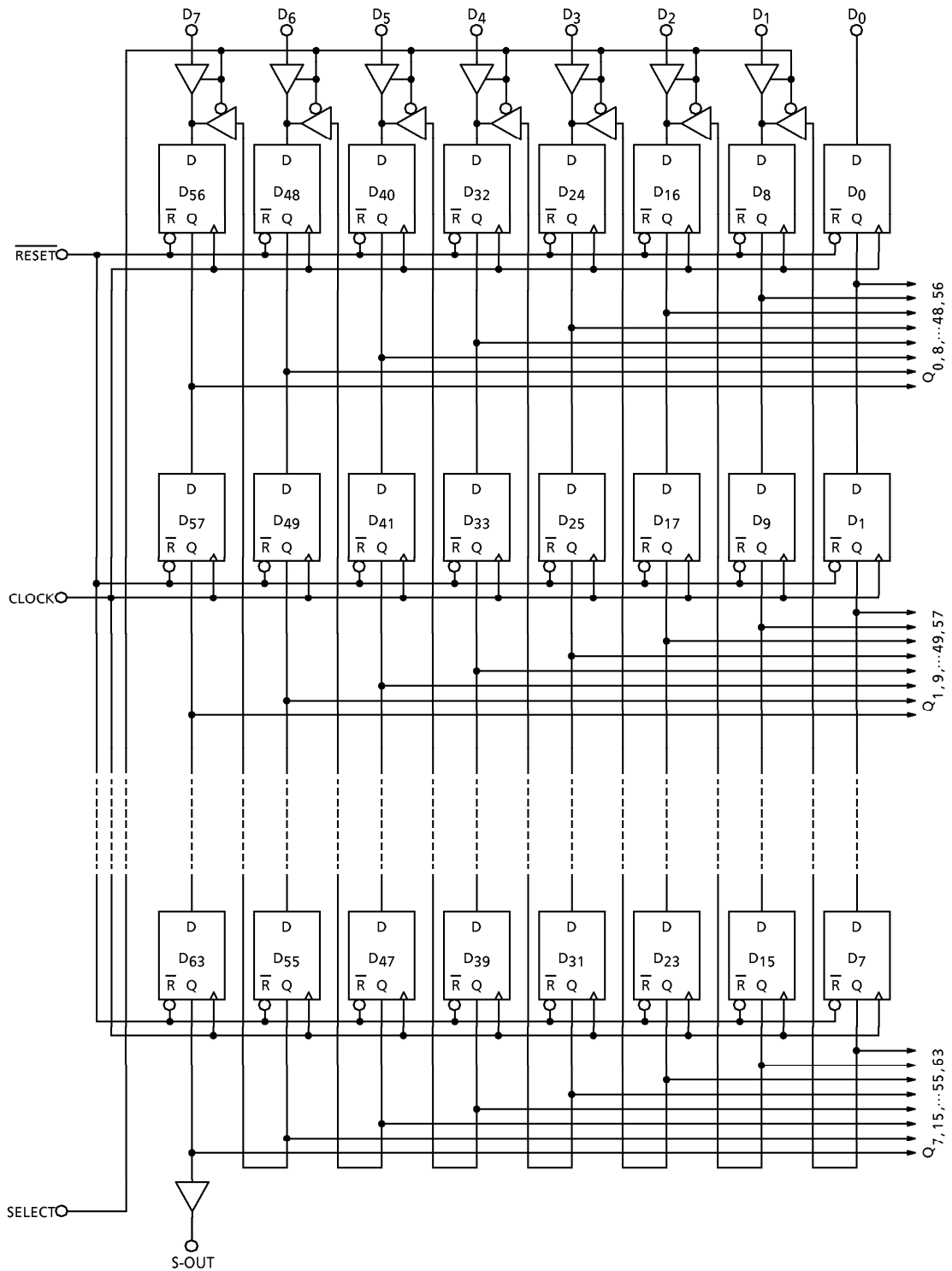
PIN CONNECTION (TOP VIEW)



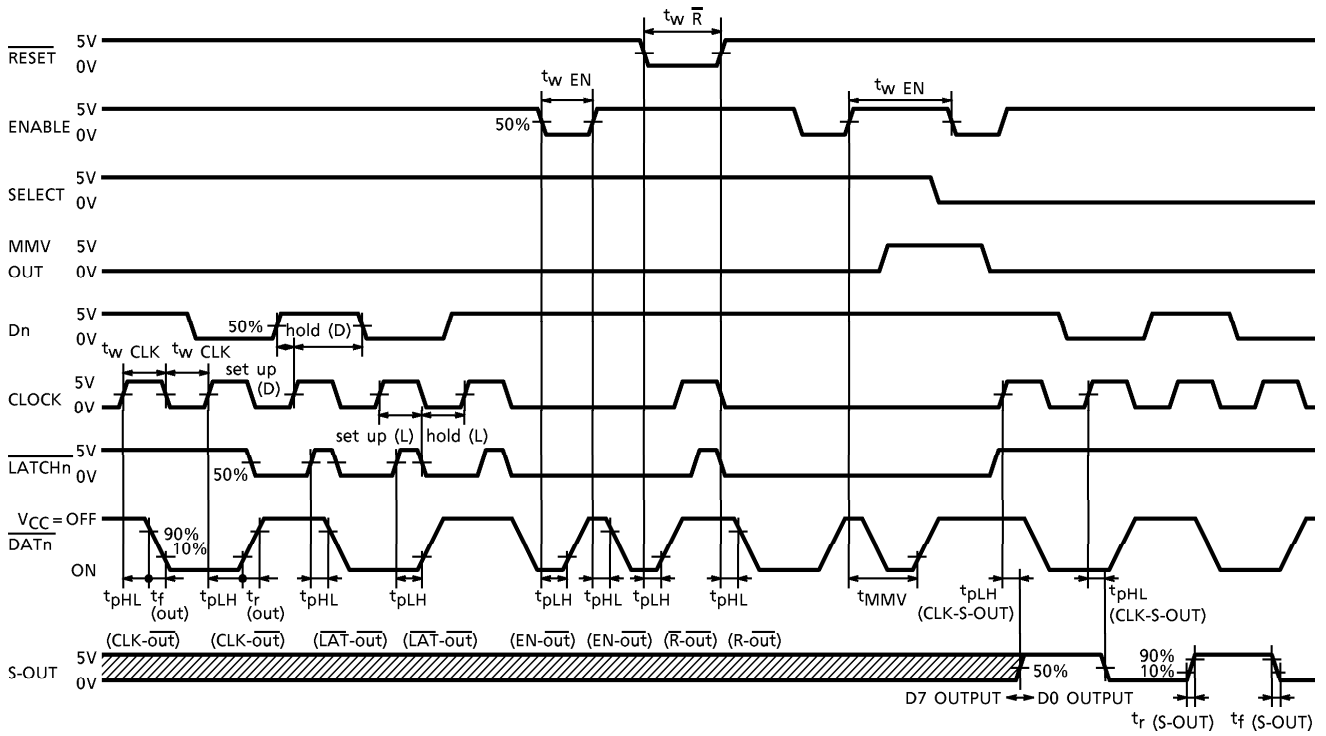
BLOCK DIAGRAM



BLOCK DIAGRAM (8×8, 1×64 shift register)



TIMING WAVEFORM



TERMINAL DESCRIPTION

PIN NAME	PIN No.	FUNCTION
CLOCK	97	Input Terminals for Shift register Clock.
ENABLE	84	"L" : All Outputs "On". Pull-Down Input Terminal.
$\overline{\text{RESET}}$	98	"L" : Reset shift register and latch. Pull-Down Input Terminal.
D0~D7	88~95	Input Terminals for Output Data. "H" : Output On, "L" : Output Off.
MMV-C/R	78	CR Connection Terminal for CR Timer (MMV).
MMV-OUT	79	Output Terminal for CR Timer (MMV).
$\overline{\text{OUT0}}\sim\overline{\text{63}}$	—	Output Terminals. These are Open Drain Outputs.
SELECT	83	Input Terminal for Input Mode Data. "H" : 8bit Parallel Input Mode, "L" : 1bit Serial Input Mode.
S-OUT	96	Output Terminal for Serial Data "D63".
$\overline{\text{LATCH1}}/\overline{\text{LATCH2}}$	86/85	Input Terminal for Latch. "H" : Data Through, "L" : Data Latch.
V _{DD}	81, 100	Supply Voltage Terminal for Control Logic.
L-GND	82, 99	Ground Terminal for Control Logic.
P-GND	—	Ground Terminal for Drivers. 10 Terminals.

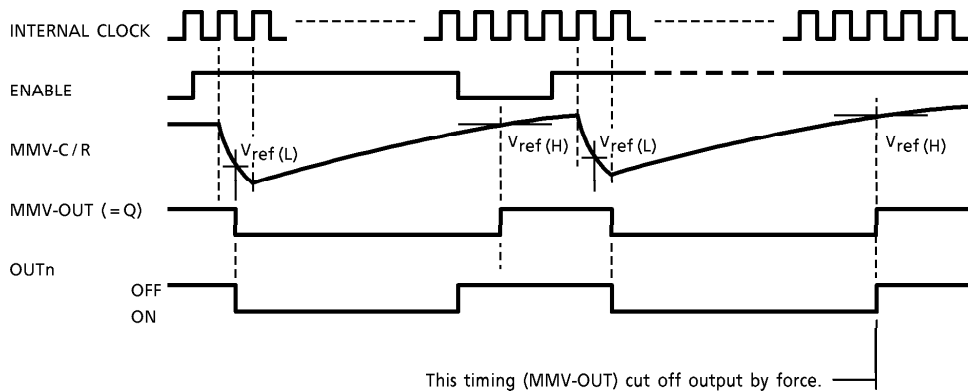
MMV OPERATION

MMV Output of Q becomes "L" when the MMV/E voltage becomes less than $V_{ref(L)}$ after the first rising edge of Internal Clock.

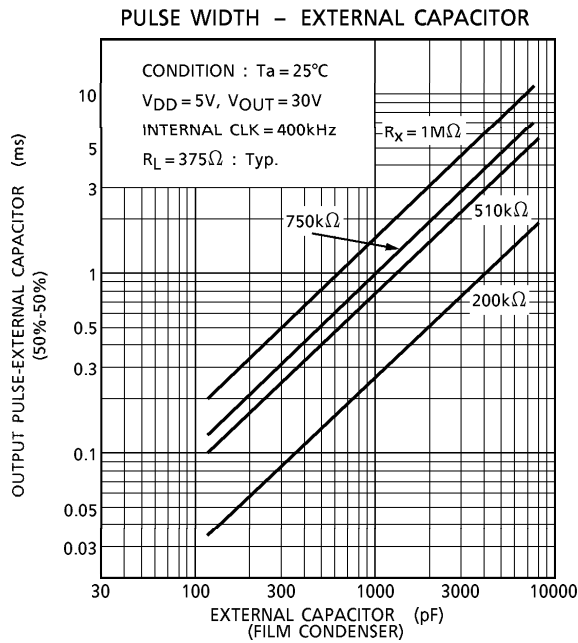
And becomes "H" when the MMV/E voltage above $V_{ref(H)}$ after re-changing of external capacitance connect to MMV/E. The external capacitance and resistor connect to MMV/E control MMV Output "ON" period.

So Output Load is protected from burn-out. It's required enough discharging time (decided by Time period of Internal Clock) of external capacitance.

(Refer to figure below)



- PULSE WIDTH OF MMV
See Below



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V _{DD}	-0.3~7.0	V
Output Drain-Source Voltage		V _{DS}	-0.4~30	V
Output Current		I _{DS}	130	mA / ch
Input Current		I _{IN}	± 5	mA
Input Voltage		V _{IN}	-0.3~V _{DD} ± 0.3	V
Power Dissipation	Free Air	P _D	1.0	W
	(Note 1) PCB		1.3	
Operating Temperature		T _{opr}	-40~85	°C
Storage Temperature		T _{stg}	-55~150	°C

(Note 1) 60×60×1.6mm Cu 24% Glass Epoxy PCB

RECOMMENDED OPERATING CONDITIONS (Ta = -40~85°C, V_{SS} = 0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage		V _{DD}	—	4.5	5	5.5	V	
Input Voltage	"H" LEVEL	V _{IH}	—	0.7 V _{DD}	—	V _{DD}	V	
	"L" LEVEL	V _{IL}	—	0	—	0.3 V _{DD}		
Output Drain-Source Voltage		V _{OUT}	—	—	—	24	V	
Output Current		I _{OUT}	Duty = 100% Duty = 80% Duty = 50%	All Output "L" Level	—	—	44	mA / ch
					—	—	49	
					—	—	62	
External Resistor		R _{EXT}	—	200	—	1000	kΩ	
External Capacitance		C _{EXT}	—	100	—	4000	pF	
Power Dissipation		P _D	—	—	—	0.67	mW	

ELECTRICAL CHARACTERISTICS (Ta = -10~80°C, VDD = 4.5~5.5V, VSS = 0V, "H" = VIH, "L" = VIL)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	"L" LEVEL	VDS1	—	IOUT = 40mA, Ta = 25°C	—	0.16	0.32	V
		VDS1	—	IOUT = 40mA	—	—	0.48	
		VDS2	—	IOUT = 100mA, Ta = 25°C	—	0.40	0.80	
		VDS2	—	IOUT = 100mA	—	—	1.20	
Output Current	"H" LEVEL	IOH	—	S-OUT VOH = 4.6V Ta = 25°C	—	0.2	0.5	mA
	"L" LEVEL	IOL	—	MMV-OUT VOL = 0.4V Ta = 25°C	—	0.2	0.5	
Output Resistor		RON	—	Ta = 25°C	—	4.00	8.00	Ω
Output Leakage Current		IOZ1	—	VOUT = 30V, EN = "L", 1bit	—	—	10	μA
		IOZ2	—	VOUT = 30V, EN = "L", 64bit	—	—	100	
Input Current		IIN	—	VIN = VDD or VSS	—	—	± 1	μA
Input Voltage	"H" LEVEL	VIH	—	—	0.7 VDD	—	—	V
	"L" LEVEL	VIL	—	—	—	—	0.3 VDD	
Voltage Supervisor Opating Voltage		VVS	—	—	2.0	—	4.0	V
Supply Current		IDD	—	—	—	—	300	μA
Operating Supply Current		IDD1	—	fCLK = 5MHz, Duty = 50% Data = 1/2 fCLK, OUTPUT off LATCH = "L", LATCH-Data = "L"	—	—	5.0	mA
		IDD2	—	fCLK = 1MHz, Duty = 50% Data = 1/64 fCLK All OUTPUT open LATCH = "H", 1bit ON	—	—	6.0	
Input Pull-Up Resistor		RVDD	—	VDD = 5.0V, Ta = 25°C	150	300	600	kΩ
Input Pull-Down Resistor		RVSS	—	VDD = 5.0V, Ta = 25°C	150	300	600	
Internal Clock Frequency		fint	—	VDD = 5.0V, Ta = 25°C	400	800	—	kHz

RECOMMENDED TIMING CONDITIONS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

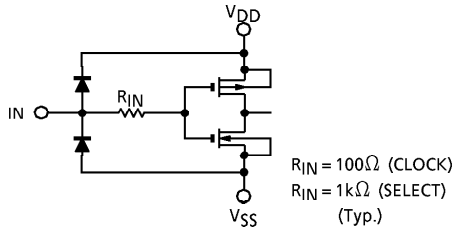
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	t_w CLK	—	50	—	—	ns
Enable Pulse Width	t_w EN	—	0.5	—	—	μs
Latch Pulse Width	t_w $\overline{\text{LAT}}$	—	50	—	—	ns
Clear Pulse Width	t_w CLR	—	80	—	—	ns
Data Set up Time	t_{setup}	—	37	50	—	ns
Data Hold Time	t_{hold}	—	50	—	—	ns

SWITCHING CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{OUT} = 26\text{V}$, $R_1 = 650\Omega$, $C_L = 15\text{pF}$)

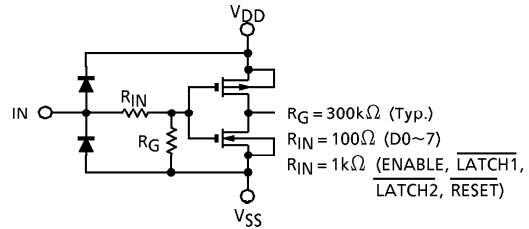
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (Low-to-High)	CLK- $\overline{\text{Outn}}$	t_{pLH}	MMV-C / R = "L"	—	—	1000
	$\overline{\text{R-Outn}}$					
	LAT1- $\overline{\text{Outn}}$					
	LAT2- $\overline{\text{Outn}}$					
	EN- $\overline{\text{Outn}}$					
Propagation Delay Time (High-to-Low)	CLK- $\overline{\text{Outn}}$	t_{pHL}	MMV-C / R = "L"	—	—	1000
	LAT1- $\overline{\text{Outn}}$					
	LAT2- $\overline{\text{Outn}}$					
	EN- $\overline{\text{Outn}}$					
Set up Time	CLK-LATn	$t_{\text{setup}}(\text{L})$	—	70	120	ns
	CLK-S-IN	$t_{\text{setup}}(\text{D})$	—	—	30	
Hold Time	CLK-LATn	$t_{\text{hold}}(\text{L})$	—	—	0	ns
	CLK-S-IN	$t_{\text{hold}}(\text{D})$	—	—	20	
Clock Pulse Width	t_w CLK	—	—	—	50	ns
Latch Pulse Width	t_w $\overline{\text{LATn}}$	—	—	—	50	ns
Reset Pulse Width	t_w $\overline{\text{R}}$	—	—	—	50	ns
Enable Pulse Width	t_w EN	—	—	—	400	ns
Output Rise Time	t_{or}	$\overline{\text{OUTn}}$	—	200	500	ns
Output Fall Time	t_{of}	$\overline{\text{OUTn}}$	—	200	500	ns
Maximum Clock Frequency	f_{MAX}	Duty = 50%	10	15	—	MHz
Voltage Supervisor Operating Pulse Width	t_w VS	$V_{DD}(\text{H}) = 5\text{V}$, $V_{DD}(\text{L}) = 2\text{V}$	—	200	—	ns
MMV Reset Time	t_{MMV}	R = 750k Ω , C = 2600pF, $T_a = 25^\circ\text{C}$	1	3	5	ms

EQUIVALENT OF INPUTS AND OUTPUT CIRCUIT

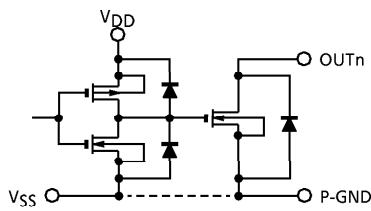
1. CLOCK, SELECT



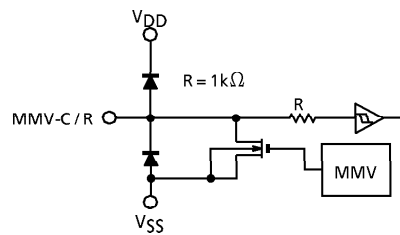
2. ENABLE, $\overline{LATCH1}$, $\overline{LATCH2}$, \overline{RESET} , D0~7



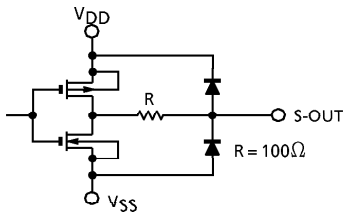
3. \overline{OUTn}



4. MMV-C/R



5. S-OUT, MMV-OUT

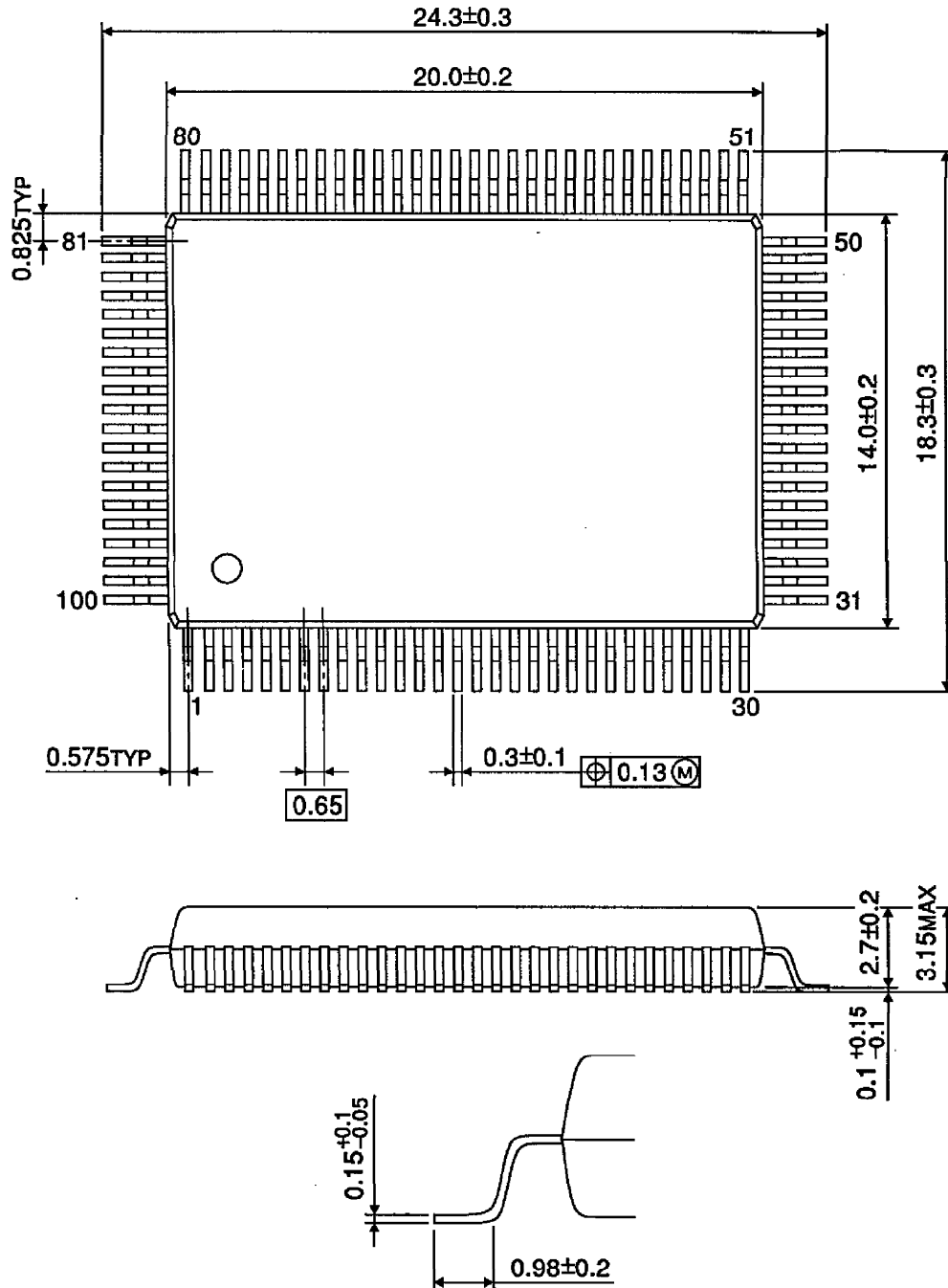


PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING
QFP100-P-1420-0.65C

Unit : mm



Weight : 1.6g (Typ.)