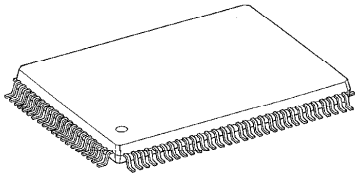
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62600F

64BIT SHIFT REGISTER / LATCH DRIVER

The TB62600F is specifically designed for 64bit Thermal Head drivers. And this IC is monolithic integrated circuits designed to be used together with Bi-CMOS (DMOS) integrated circuit. The devices consist of a 64bit shift register, dual 64bit latches, and 64 output DMOS structures.



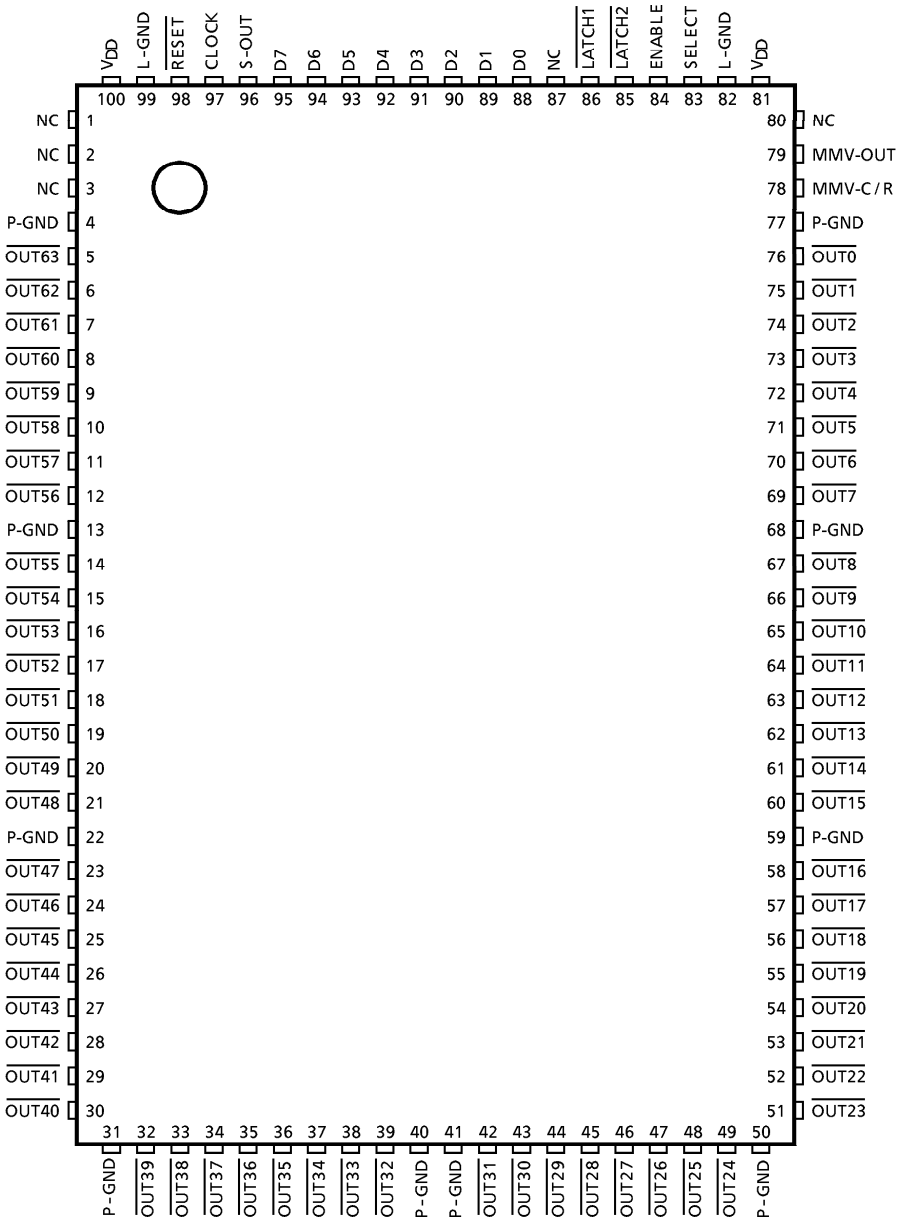
QFP100-P-1420-0.65C

Weight : 1.6g (Typ.)

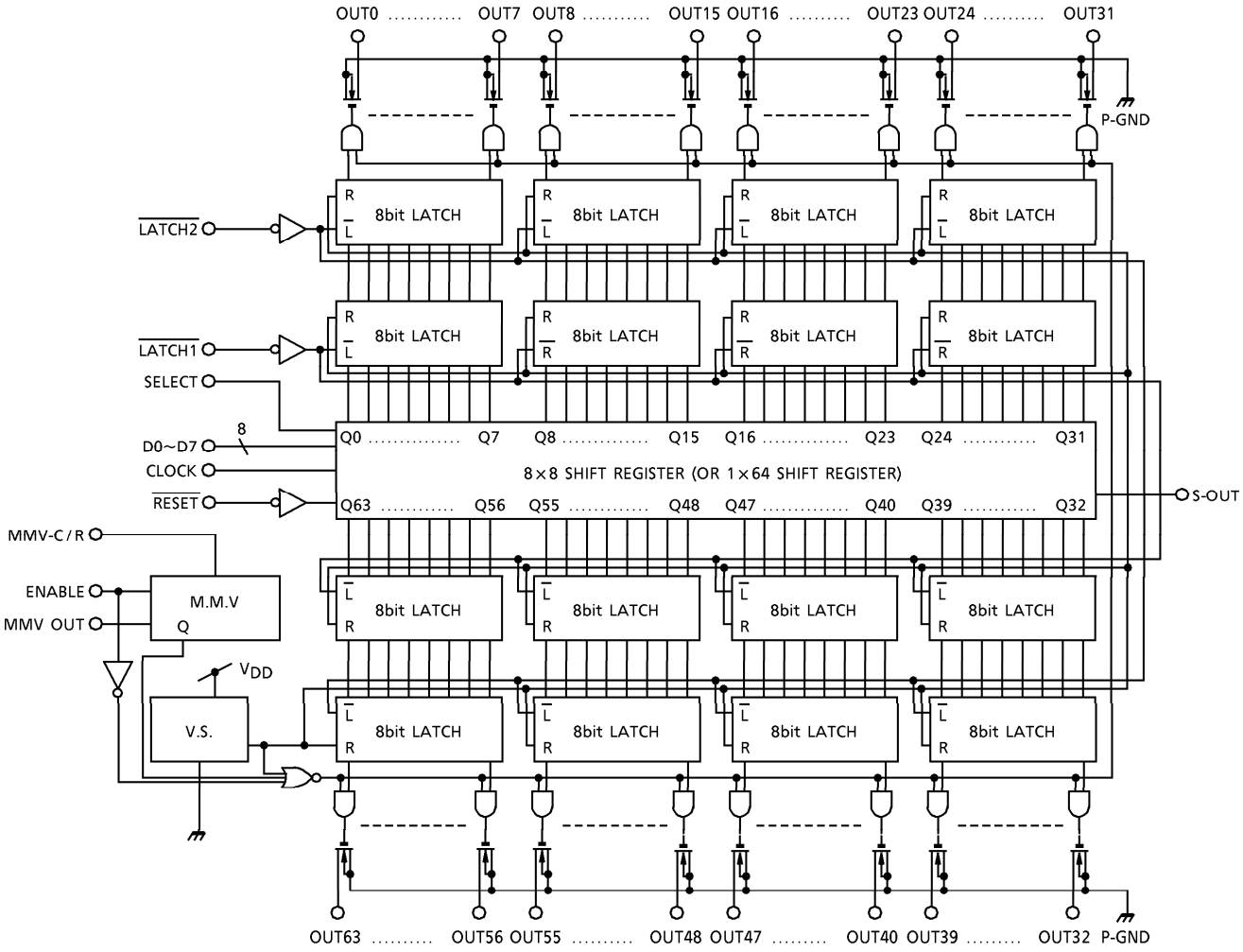
FEATURE

- Built-in selection circuit : parallel-in parallel-out (8×8) or serial-in parallel-out (1×64)
- CMOS compatible inputs
- Open-drain DMOS outputs
- Low steady-state power consumption
- Built-in mono stable multi-viblator for head protection
- Package : QFP100-P-1420C

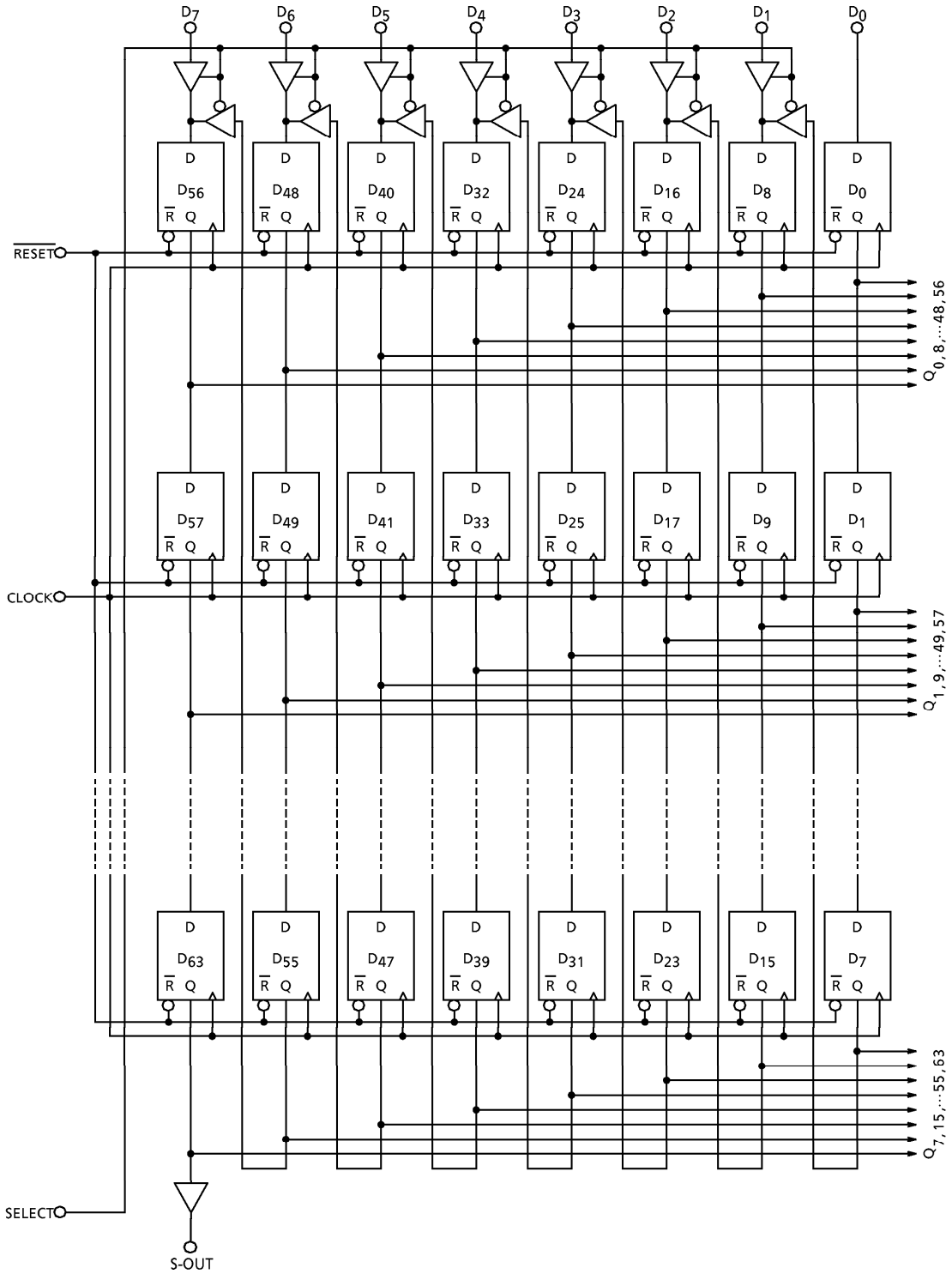
PIN CONNECTION (TOP VIEW)



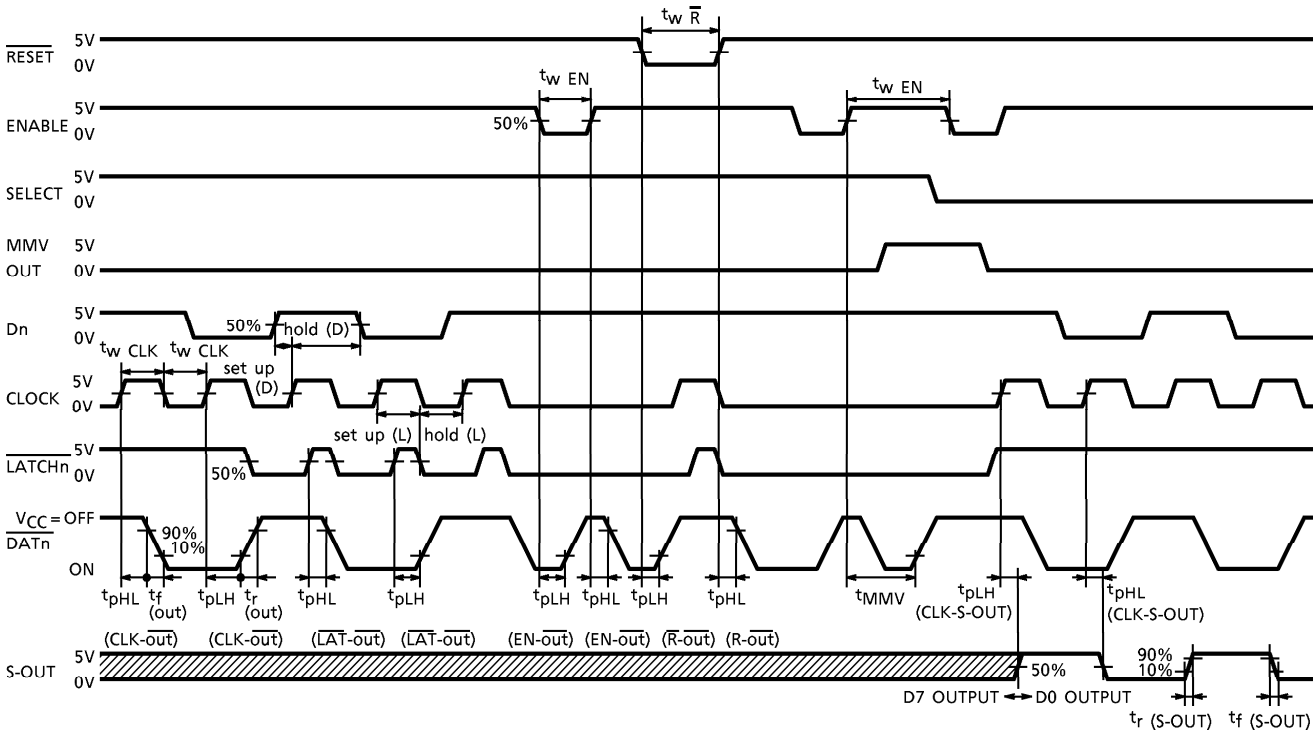
BLOCK DIAGRAM



BLOCK DIAGRAM (8×8, 1×64 shift register)



TIMING WAVEFORM

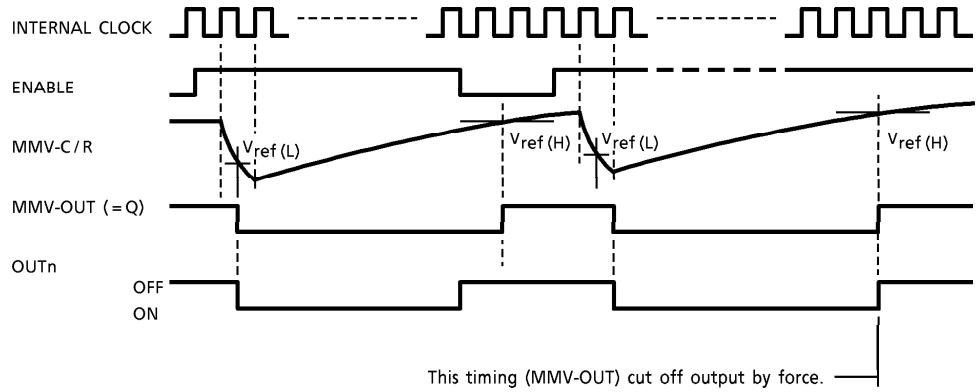


TERMINAL DESCRIPTION

PIN NAME	PIN No.	FUNCTION
CLOCK	97	Input Terminals for Shift register Clock.
ENABLE	84	"L" : All Outputs "On". Pull-Down Input Terminal.
$\overline{\text{RESET}}$	98	"L" : Reset shift register and latch. Pull-Down Input Terminal.
D0~D7	88~95	Input Terminals for Output Data. "H" : Output On, "L" : Output Off.
MMV-C / R	78	CR Connection Terminal for CR Timer (MMV).
MMV-OUT	79	Output Terminal for CR Timer (MMV).
$\overline{\text{OUT0}}$~$\overline{\text{63}}$	—	Output Terminals. These are Open Drain Outputs.
SELECT	83	Input Terminal for Input Mode Data. "H" : 8bit Parallel Input Mode, "L" : 1bit Serial Input Mode.
S-OUT	96	Output Terminal for Serial Data "D63".
$\overline{\text{LATCH1}}$ / $\overline{\text{LATCH2}}$	86 / 85	Input Terminal for Latch. "H" : Data Through, "L" : Data Latch.
V_{DD}	81, 100	Supply Voltage Terminal for Control Logic.
L-GND	82, 99	Ground Terminal for Control Logic.
P-GND	—	Ground Terminal for Drivers. 10 Terminals.

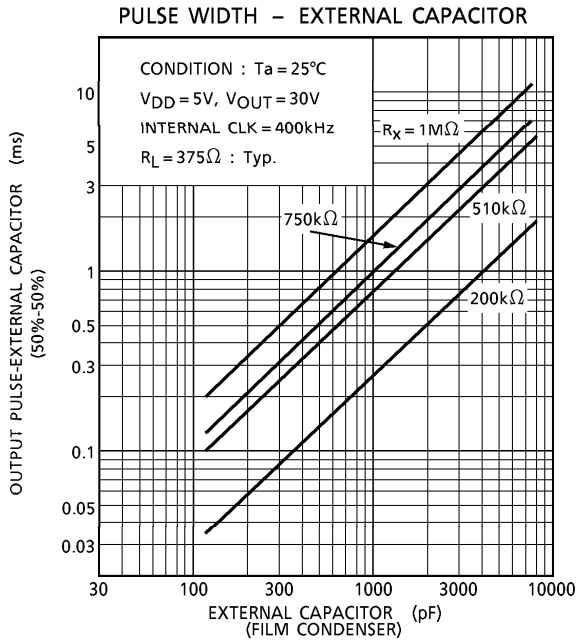
MMV OPERATION

MMV Output of Q becomes "L" when the MMV / E voltage becomes less than $V_{ref\,(L)}$ after the first rising edge of Internal Clock.
And becomes "H" when the MMV / E voltage above $V_{ref\,(H)}$ after re-changing of external capacitance connect to MMV / E. The external capacitance and resistor connect to MMV / E control MMV Output "ON" period.
So Output Load is protected from burn-out. It's required enough discharging time (decided by Time period of Internal Clock) of external capacitance.
(Refer to figure below)



- PULSE WIDTH OF MMV

  See Below



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	−0.3~7.0	V
Output Drain-Source Voltage		V_{DS}	−0.4~30	V
Output Current		I_{DS}	130	mA / ch
Input Current		I_{IN}	±5	mA
Input Voltage		V_{IN}	−0.3~V_{DD} ± 0.3	V
Power Dissipation	Free Air	P_D	1.0	W
	(Note 1) PCB		1.3	
Operating Temperature		T_{opr}	−40~85	°C
Storage Temperature		T_{stg}	−55~150	°C

(Note 1) 60 × 60 × 1.6mm Cu 24% Glass Epoxy PCB

RECOMMENDED OPERATING CONDITIONS (Ta = −40~85°C, V_{SS} = 0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{DD}	—		4.5	5	5.5	V
Input Voltage	"H" LEVEL	V_{IH}	—		0.7 V_{DD}	—	V_{DD}	V
	"L" LEVEL	V_{IL}	—		0	—	0.3 V_{DD}	
Output Drain-Source Voltage		V_{OUT}	—		—	—	24	V
Output Current		I_{OUT}	Duty = 100%	All Output "L" Level	—	—	44	mA / ch
			Duty = 80%		—	—	49	
			Duty = 50%		—	—	62	
External Resistor		R_{EXT}	—		200	—	1000	kΩ
External Capacitance		C_{EXT}	—		100	—	4000	pF
Power Dissipation		P_D	—		—	—	0.67	mW

ELECTRICAL CHARACTERISTICS (Ta = −10~80°C, V_{DD} = 4.5~5.5V, V_{SS} = 0V, "H" = V_{IH}, "L" = V_{IL})

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	"L" LEVEL	V_{DS1}	—	I_{OUT} = 40mA, Ta = 25°C		—	0.16	0.32	V
		V_{DS1}	—	I_{OUT} = 40mA		—	—	0.48	
		V_{DS2}	—	I_{OUT} = 100mA, Ta = 25°C		—	0.40	0.80	
		V_{DS2}	—	I_{OUT} = 100mA		—	—	1.20	
Output Current	"H" LEVEL	I_{OH}	—	S-OUT MMV-OUT	V_{OH} = 4.6V Ta = 25°C	—	0.2	0.5	mA
	"L" LEVEL	I_{OL}	—		V_{OL} = 0.4V Ta = 25°C	—	0.2	0.5	
Output Resistor		R_{ON}	—	Ta = 25°C		—	4.00	8.00	Ω
Output Leakage Current		I_{OZ1}	—	V_{OUT} = 30V, EN = "L", 1bit		—	—	10	μA
		I_{OZ2}	—	V_{OUT} = 30V, EN = "L", 64bit		—	—	100	
Input Current		I_{IN}	—	V_{IN} = V_{DD} or V_{SS}		—	—	±1	μA
Input Voltage	"H" LEVEL	V_{IH}	—	—		0.7 V_{DD}	—	—	V
	"L" LEVEL	V_{IL}	—	—		—	—	0.3 V_{DD}	
Voltage Superviser Opating Voltage		V_{VS}	—	—		2.0	—	4.0	V
Supply Current		I_{DD}	—	—		—	—	300	μA
Operating Supply Current		I_{DD1}	—	f_{CLK} = 5MHz, Duty = 50% Data = 1 / 2 f_{CLK}, OUTPUT off $\overline{LATCH}$ = "L", $\overline{LATCH}$-Data = "L"		—	—	5.0	mA
		I_{DD2}	—	f_{CLK} = 1MHz, Duty = 50% Data = 1 / 64 f_{CLK} All OUTPUT open $\overline{LATCH}$ = "H", 1bit ON		—	—	6.0	
Input Pull-Up Resistor		RV_{DD}	—	V_{DD} = 5.0V, Ta = 25°C		150	300	600	kΩ
Input Pull-Down Resistor		RV_{SS}	—	V_{DD} = 5.0V, Ta = 25°C		150	300	600	
Internal Clock Frequency		f_{int}	—	V_{DD} = 5.0V, Ta = 25°C		400	800	—	kHz

RECOMMENDED TIMING CONDITIONS (Ta = −40~85°C, V_{DD} = 4.5~5.5V, V_{SS} = 0V)

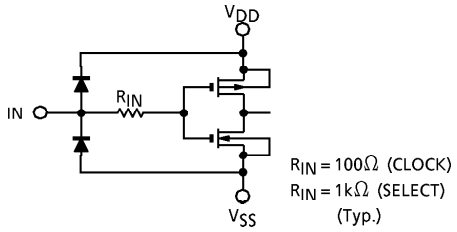
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	$t_{w\ CLK}$	—	50	—	—	ns
Enable Pulse Width	$t_{w\ EN}$	—	0.5	—	—	μs
Latch Pulse Width	$t_{w\ \overline{LAT}}$	—	50	—	—	ns
Clear Pulse Width	$t_{w\ CLR}$	—	80	—	—	ns
Data Set up Time	t_{setup}	—	37	50	—	ns
Data Hold Time	t_{hold}	—	50	—	—	ns

SWITCHING CHARACTERISTICS (Ta = 25°C, V_{DD} = 5V, V_{OUT} = 26V, R_1 = 650Ω, C_L = 15pF)

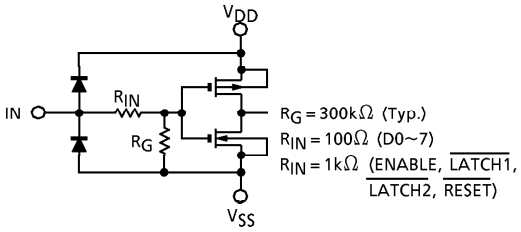
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (Low-to-High)	CLK-$\overline{Outn}$	t_{pLH}	MMV-C / R = "L"	—	—	1000	ns
	$\overline{R}$-$\overline{Outn}$		MMV-C / R = "L"	—	—	1000	
	$\overline{LAT1}$-$\overline{Outn}$		MMV-C / R = "L"	—	—	1000	
	$\overline{LAT2}$-$\overline{Outn}$		MMV-C / R = "L"	—	—	1000	
	EN-$\overline{Outn}$		R = 750kΩ, C = 2600pF, Ta = 25°C	—	—	2500	
Propagation Delay Time (High-to-Low)	CLK-$\overline{Outn}$	t_{pHL}	MMV-C / R = "L"	—	—	1000	ns
	$\overline{LAT1}$-$\overline{Outn}$		MMV-C / R = "L"	—	—	1000	
	$\overline{LAT2}$-$\overline{Outn}$		MMV-C / R = "L"	—	—	1000	
	EN-$\overline{Out_n}$		R = 750kΩ, C = 2600pF, Ta = 25°C	—	—	2500	
Set up Time	CLK-$\overline{LATn}$	$t_{setup\ (L)}$	—	—	70	120	ns
	CLK-S-IN	$t_{setup\ (D)}$	—	—	—	30	
Hold Time	CLK-$\overline{LATn}$	$t_{hold\ (L)}$	—	—	—	0	
	CLK-S-IN	$t_{hold\ (D)}$	—	—	—	20	
Clock Pulse Width		$t_{w\ CLK}$	—	—	—	50	ns
Latch Pulse Width		$t_{w\ \overline{LATn}}$	—	—	—	50	ns
Reset Pulse Width		$t_{w\ \overline{R}}$	—	—	—	50	ns
Enable Pulse Width		$t_{w\ EN}$	—	—	—	400	ns
Output Rise Time		t_{or}	$\overline{OUTn}$	—	200	500	ns
Output Fall Time		t_{of}	$\overline{OUTn}$	—	200	500	ns
Maximum Clock Frequency		f_{MAX}	Duty = 50%	10	15	—	MHz
Voltage Superviser Operating Pulse Width		$t_{w\ VS}$	$V_{DD\ (H)}$ = 5V, $V_{DD\ (L)}$ = 2V	—	200	—	ns
MMV Reset Time		t_{MMV}	R = 750kΩ, C = 2600pF, Ta = 25°C	1	3	5	ms

EQUIVALENT OF INPUTS AND OUTPUT CIRCUIT

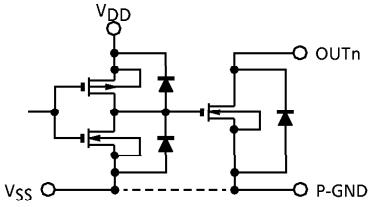
1. CLOCK, SELECT



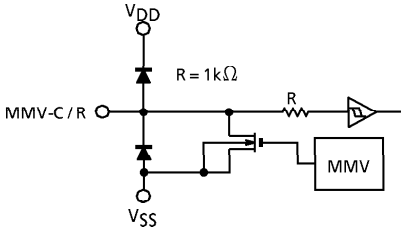
2. ENABLE, $\overline{\text{LATCH1}}$, $\overline{\text{LATCH2}}$, $\overline{\text{RESET}}$, D0~7



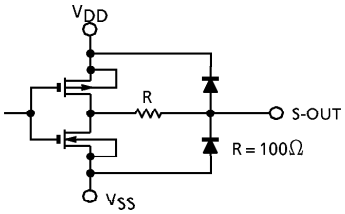
3. $\overline{\text{OUTn}}$



4. MMV-C / R



5. S-OUT, MMV-OUT

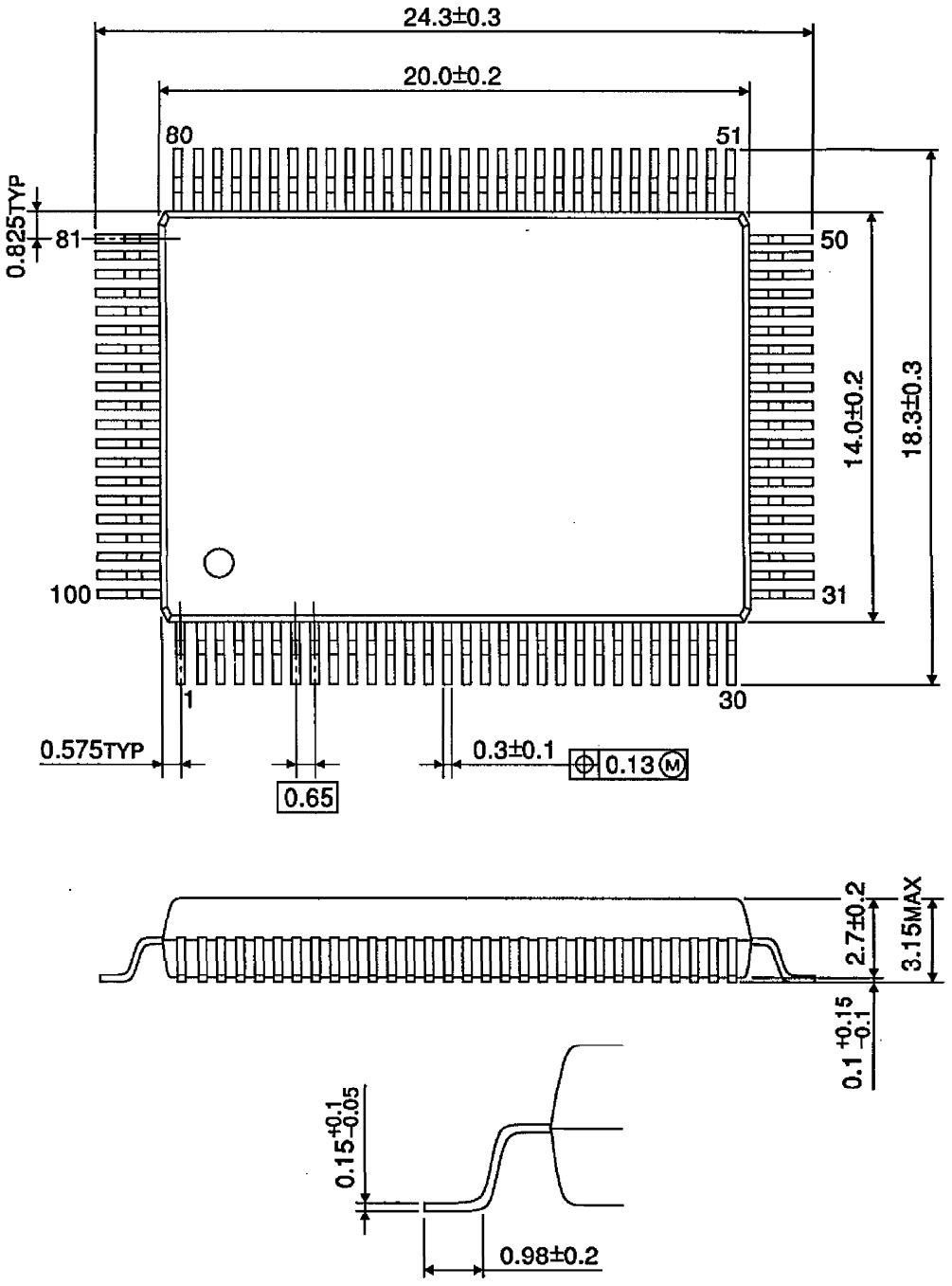


PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING

QFP100-P-1420-0.65C Unit : mm



Weight : 1.6g (Typ.)