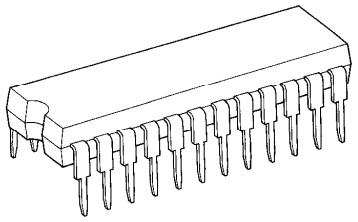
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62701AN

16BIT SHIFT REGISTER, LATCH & CONSTANT CURRENT DRIVERS

The TB62701AN is specifically designed for LED and LED-DISPLAY constant current drivers.
This constant current output circuit is able to set up external resister (I_{OUT} = 5 to 50mA).
This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.
The devices consist of 16bit Shift Register, Latch, AND-GATE and Constant Current Driver.



SDIP24-P-300-1.78
Weight : 1.2g (Typ.)

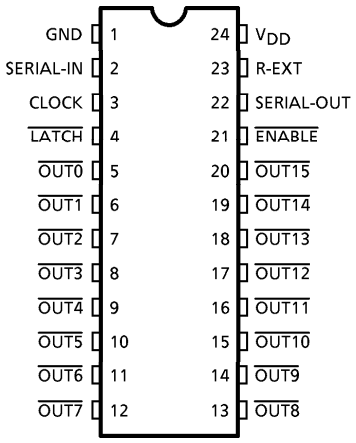
FEATURES

- OUTPUT CURRENT : Set-up at 50mA maximum with an external resister.
- A LITTLE CHANGE OF OUTPUT CURRENT (Ta = 25°C, V_{DD} = 5.0V)

OUT-GND VOLTAGE	A LITTLE CHANGE OF CHANNEL	I_{OUT} [mA]
≧0.4V	±7%	5~50mA
≧0.7V		

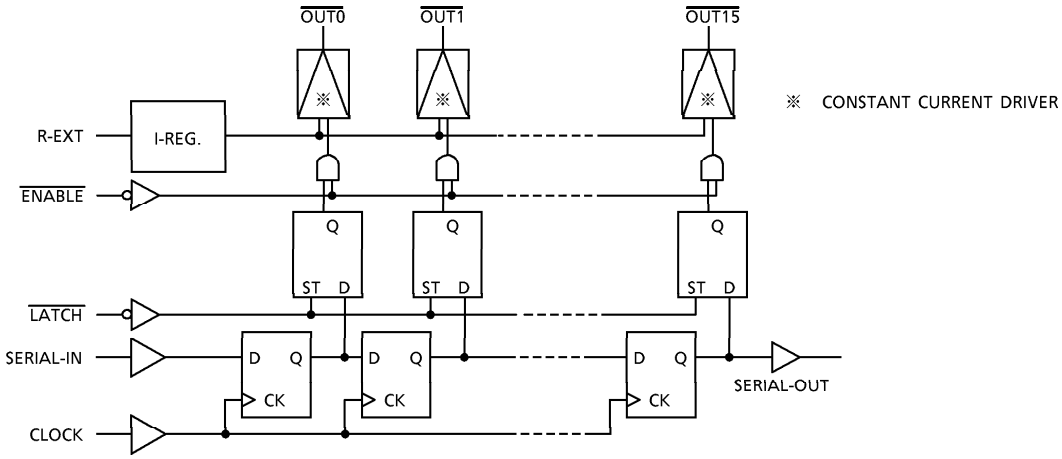
- 5V CMOS Compatible Input
- PACKAGE : SDIP-24 (SDIP24-P-300)
- MAXIMUM CLOCK FREQUENCY : f_{MAX} = 2.5MHz (cascade operation, Ta = 25°C)

PIN CONNECTION (TOP VIEW)

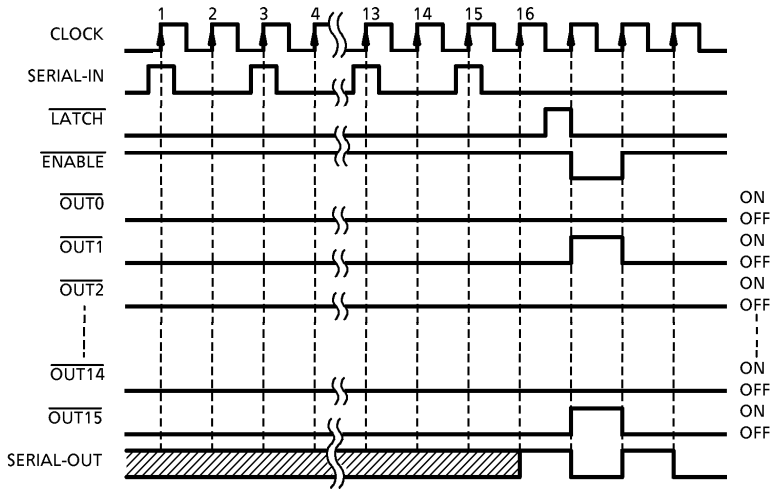


961001EBA2

BLOCK DIAGRAM



TIMING DIAGRAM



TERMINAL DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic driver
2	SERIAL-IN	Serial data input terminal for shift register
3	CLOCK	Clock input terminal for data shift to up-edge
4	$\overline{\text{LATCH}}$	"H" Level : data through, "L" Level : data hold
24	V_{DD}	Supply voltage terminal
5~12 13~20	OUTn	Output terminals
21	$\overline{\text{ENABLE}}$	"H" Level output off, "L" Level : latch data = "H" Level then output on, latch data = "L" Level then output off
22	SERIAL-OUT	Serial data output terminal for shift register
23	R-EXT	The register which connects between R-EXT and GND sets the constant output current.

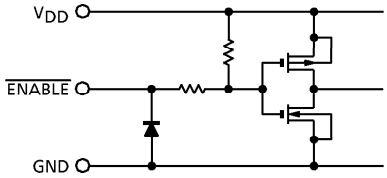
TRUTH TABLE

INPUT				OUTPUT $\overline{\text{OUTn}}$ (t = n)			
CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	$\overline{\text{OUT0}}$ ···	$\overline{\text{OUT7}}$ ···	$\overline{\text{OUT15}}$	SERIAL-OUT
↑	H	L	D_n	D_n	D_{n-7}	D_{n-15}	D_{n-15}
↑	L	L	D_n	No change			D_{n-15}
↑	※	H	D_n	OFF	OFF	OFF	D_{n-15}
↓	※	※	D_n	No change			No change

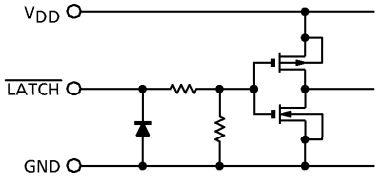
(Note) D_n~D_{n-15} = "H" then OUTn is ON, "L" then OUTn is OFF.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

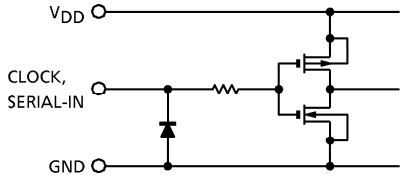
1. ENABLE terminal



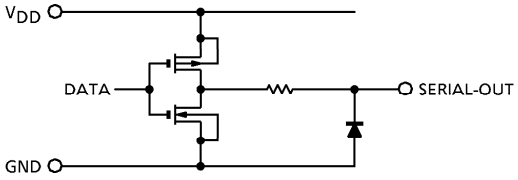
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Output Voltage	V_{CE}	−0.5~30	V
Output Current	I_{OUT}	50	mA
Input Voltage	V_{IN}	−0.4~V_{DD} + 0.4	V
GND Terminal Current	I_{GND}	800	mA
Clock Frequency	f_{CK}	2.5	MHz
Power Dissipation	P_D	1.78	W
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note) Ambient temperature delated above 25°C in the proportion of 14.2mW / °C.

RECOMMENDED OPERATING CONDITION (Ta = −40~85°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{DD}	—	4.5	5.0	5.5	V
Output Voltage		V_{OUT}	—	—	—	30.0	—
Output Current	$\overline{OUTn}$	I_{OUT}	DC 1 circuit	—	—	45	mA
	S-OUT	I_{OH}	—	—	—	−1.0	
		I_{OL}	—	—	—	1.0	
Input Voltage		V_{IN}	—	0	—	V_{DD}	V
Data Set Up Time		$t_{setup\,(D)}$	—	100	—	—	ns
Data Hold Time		$t_{hold\,(D)}$	—	20	—	—	ns
Latch Set Up Time		$t_{setup\,(L)}$	—	300	—	—	ns
Latch Hold Time		$t_{hold\,(L)}$	—	100	—	—	ns
Clock Pulse Width		$t_{w\ CLK}$	—	100	—	—	ns
		$t_{w\ \overline{CLK}}$	—	100			
Latch Pulse Width		$t_{w\ LAT}$	—	300	—	—	ns
		$t_{w\ \overline{LAT}}$	—	300			
Clock Frequency		f_{CK}	Cascade operation	—	—	2.0	MHz
Power Dissipation		P_D	Ta = 85°C	—	—	0.72	W

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, Ta = 25°C unless otherwise noted)

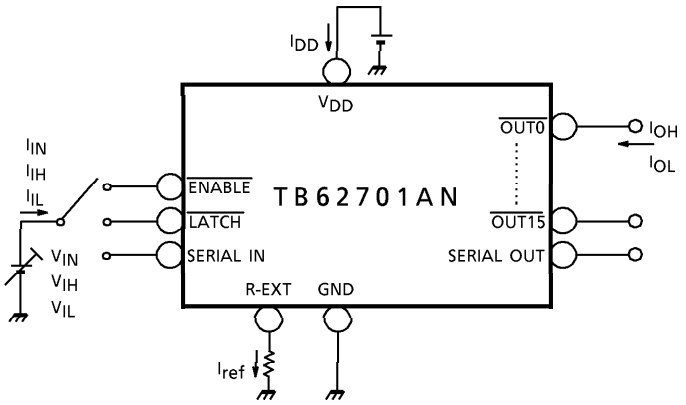
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	V_{IH}	—	—	70%V_{DD}	—	V_{DD}	V
	"L" level	V_{IL}	—	—	GND	—	30%V_{DD}	
Output Leakage Current		I_{OH}	—	V_{OH} = 30V	—	—	10	μA
Output Voltage	S-OUT	V_{OL}	—	I_{OL} = + 1.0mA	—	—	0.4	V
		V_{OH}	—	I_{OH} = − 1.0mA	4.6	—	—	
Output Current 1		I_{OL1}	—	V_{CE} = 0.7V, R_{EXT} = 560Ω	35.2	41.5	47.7	mA
		I_{OL2}	—	V_{CE} = 0.4V, R_{EXT} = 560Ω (include ΔI_{OL1})	33.1	39.0	44.9	
	Delta I_{OUT}	ΔI_{OL1}	—	R_{EXT} = 560Ω, I_{OUT} = 40mA, V_{CE} = 0.4V	—	±3.0	±7.0	%
Supply Voltage Regulation		% / V_{DD}	—	R_{EXT} = 560Ω	—	18	—	% / V
Reference Voltage		V_{ref}	—	R_{EXT} = 560Ω, Ta = − 40~85°C	—	1.26	—	V
Pull Up / Down Resister		R_{IN}	—	—	100	200	400	kΩ
Supply Current	"OFF"	I_{DD} (off) 1	—	R_{EXT} = OPEN, OUTn = Off	—	0.4	0.6	mA
		I_{DD} (off) 2	—	R_{EXT} = 560Ω, OUTn = Off	—	6.5	10.0	
	"ON"	I_{DD} (on)	—	R_{EXT} = 560Ω, OUTn = Off	—	13.5	20.0	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

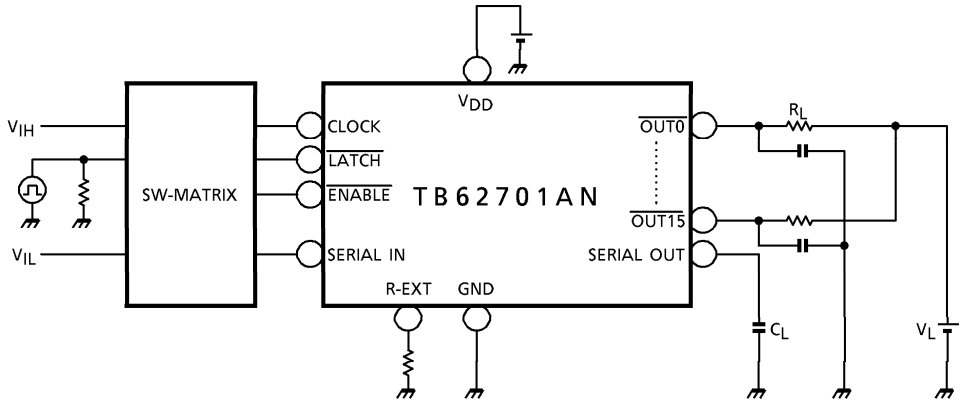
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CK-S-OUT	t_{pLH}	V_{DD} = 5.0V V_{CE} = 1.0V V_{IH} = VDD V_{IL} = GND f_{CK} = 2MHz R_{EXT} = 560Ω I_{OUT} = 30mA	—	95	500	ns
	CK-$\overline{OUTn}$			—	130	500	
	$\overline{LATCH}$-$\overline{OUTn}$			—	130	500	
	$\overline{EN}$-$\overline{OUTn}$			—	130	500	
Propagation Delay Time ("H" to "L")	CK-S-OUT	t_{pHL}		—	95	720	ns
	CK-$\overline{OUTn}$			—	130	500	
	$\overline{LATCH}$-$\overline{OUTn}$			—	130	500	
	$\overline{EN}$-$\overline{OUTn}$			—	130	500	
Maximum Clock Frequency		f_{MAX} (*1)		2.0	—	2.5	MHz
Minimum Pulse Width	CK	t_w CK		—	45	80	ns
	$\overline{LATCH}$	t_w $\overline{LAT}$		—	10	50	
Data Set Up Time		$t_{setup\ (D)}$		—	17	50	ns
Data Hold Time		$t_{hold\ (D)}$		—	− 7	10	
Latch Set Up Time	LH	$t_{\overline{LAT}setup}$		—	70	200	ns
	HL			—	70	200	
Latch Hold Time	LH	$t_{\overline{LAT}hold}$		—	− 70	50	ns
	HL			—	− 70	50	
Maximum Clock Rise Time		t_r		—	—	10	μs
Maximum Clock Fall Time		t_f		—	—	10	
Maximum Output Rise Time		t_{or}		—	35	80	ns
Maximum Output Fall Time		t_{of}		—	40	80	

*1 : Cascade operation

DC CHARACTERISTIC TEST CIRCUIT

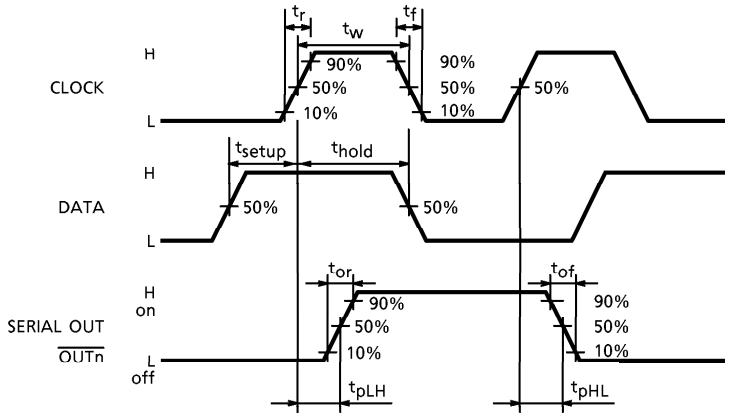


AC CHARACTERISTIC TEST CIRCUIT

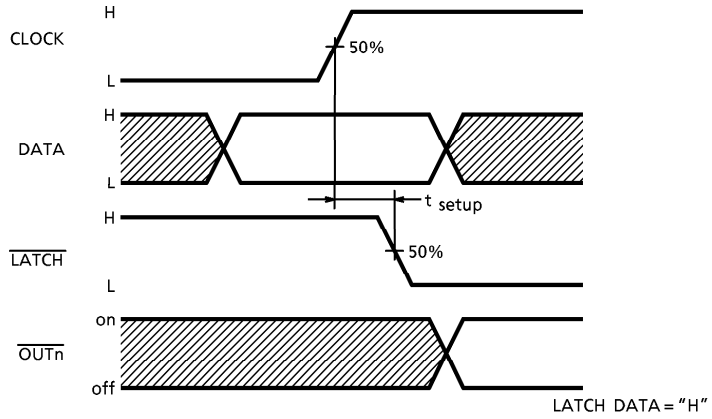


TIMING WAVE FORM

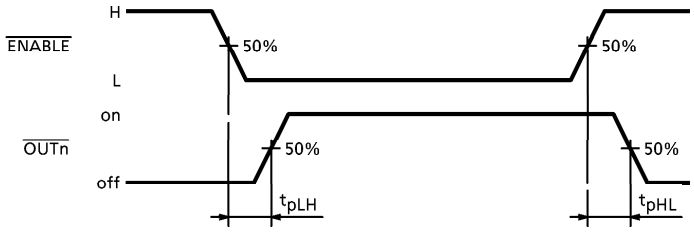
1. CLOCK-SERIAL OUT, OUTn



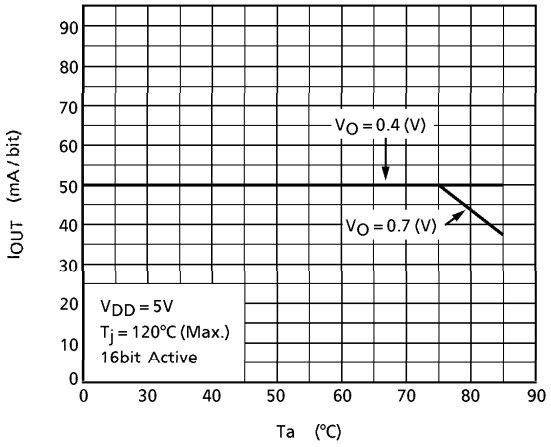
2. CLOCK-$\overline{LATCH}$



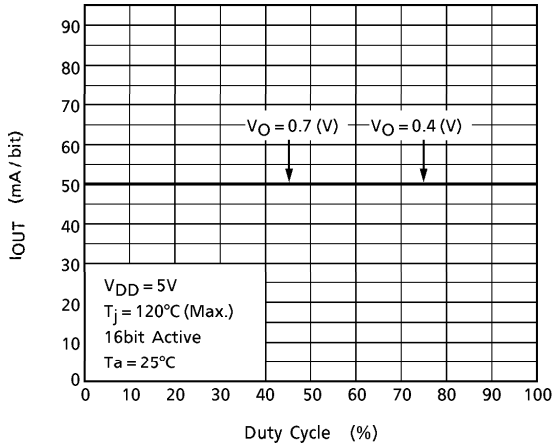
3. $\overline{ENABLE}$



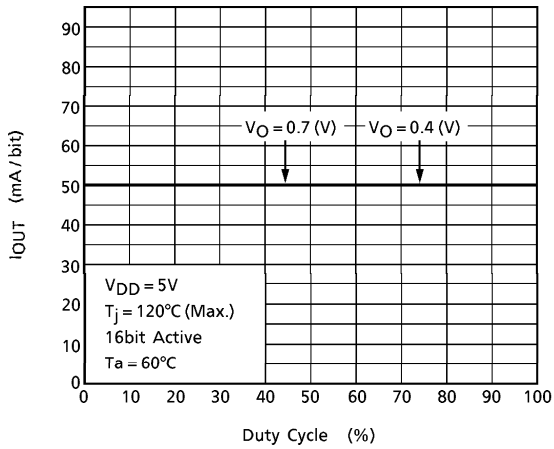
Ta – I_{OUT}



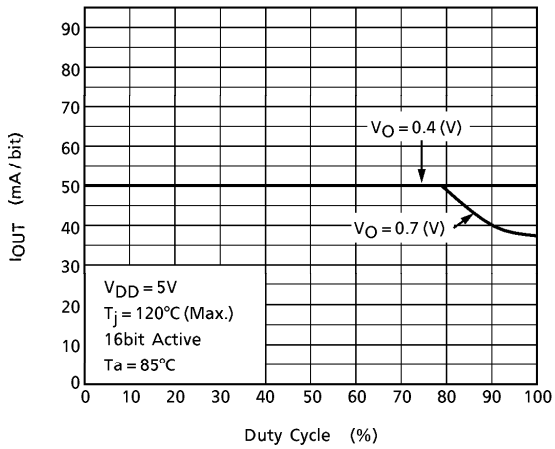
I_{OUT} – Duty Cycle



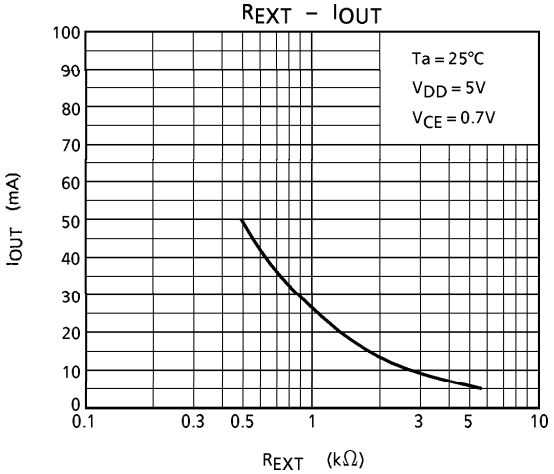
I_{OUT} – Duty Cycle



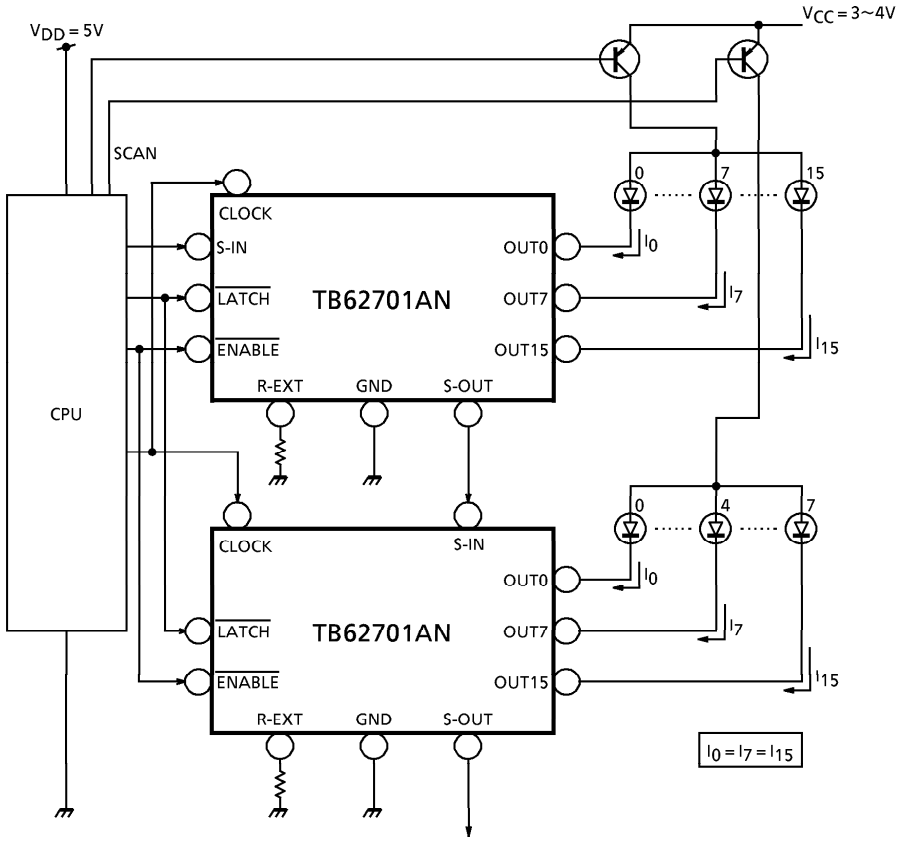
I_{OUT} – Duty Cycle



R_{EXT} – I_{OUT}



APPLICATION CIRCUIT

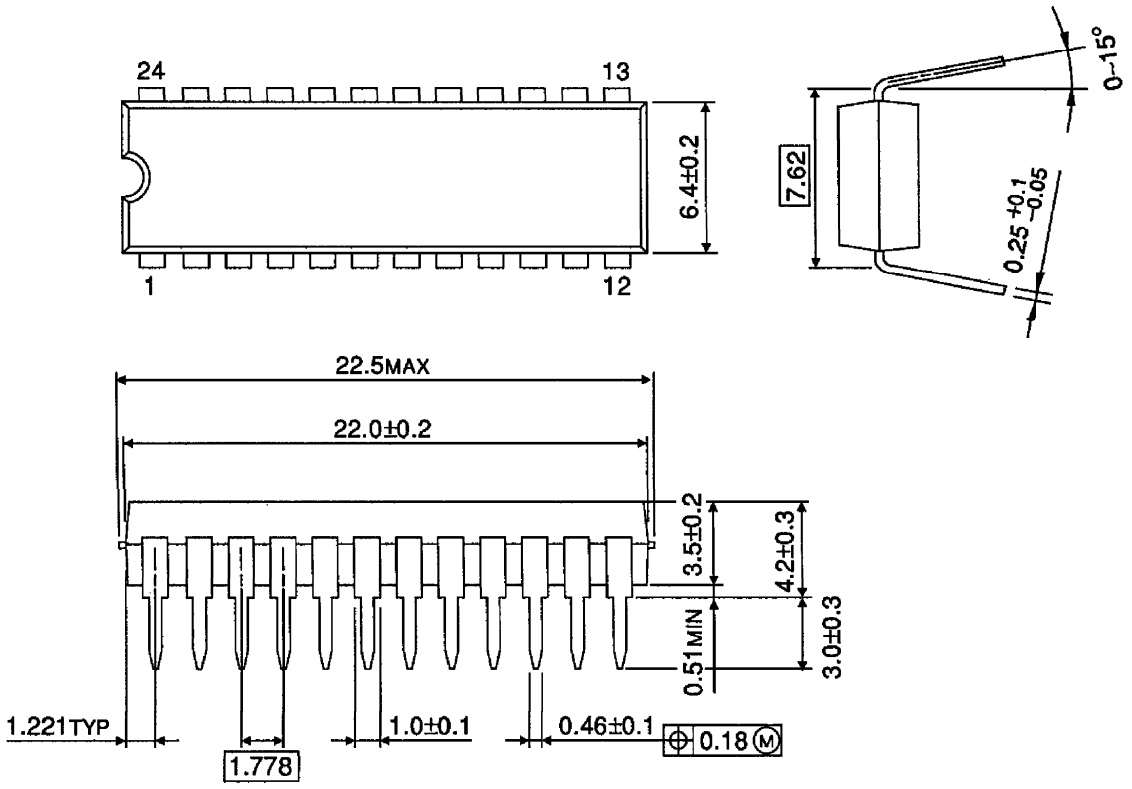


PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING

SDIP24-P-300-1.78 Unit : mm



Weight : 1.2g (Typ.)