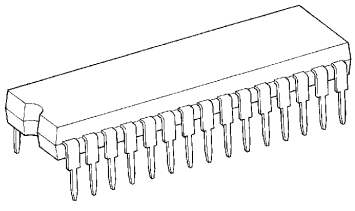
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62708N

16BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT SOURCE DRIVERS

The TB62708N is specifically designed for LED and LED DISPLAY (Cathode Common) constant current drivers. This constant current output circuits is able to set up external resistor (I_{OUT} = 5~90mA).
This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.
The devices consist of 16bit shift register, latch, AND-GATE and Constant Current Drivers.



SDIP30-P-400-1.78
Weight : 1.99g (Typ.)

FEATURES

- Constant Current Output :

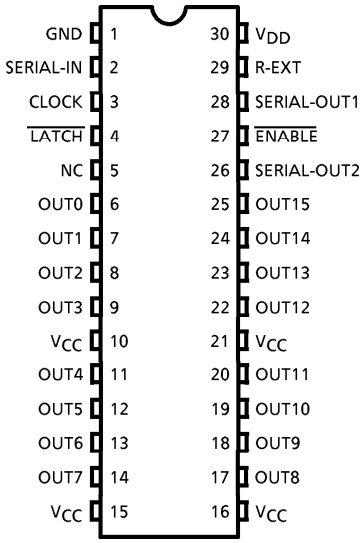
  Can set up all output current with one resistor for 5 to 90mA.

- Constant Output Current Matching :

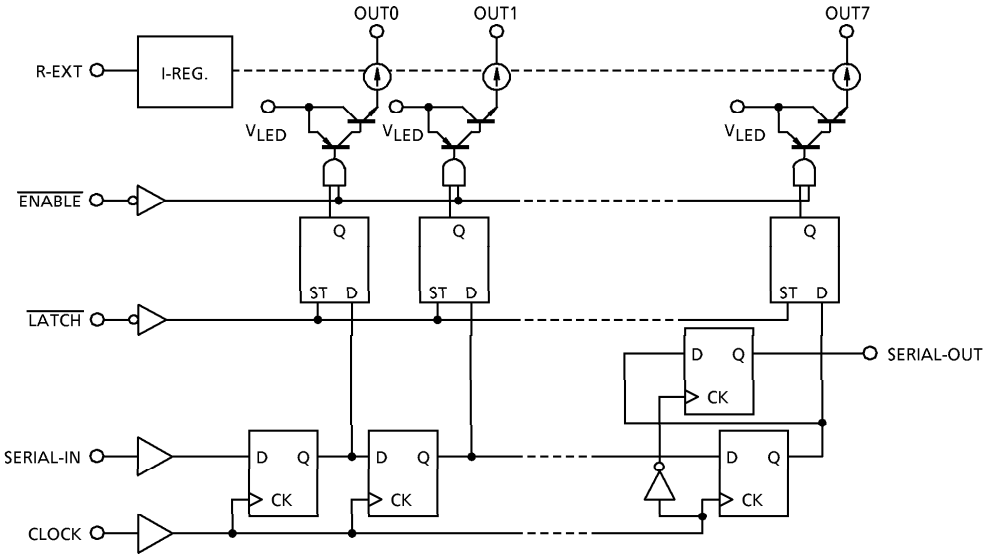
OUTPUT-GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
≧2.0 [V]	±6.0 [%]	−90 [mA]

- Maximum Clock Frequency : f_{CLK} = 15 [MHz] (Cascade Connected Operate, T_{opr} = 25°C)
- 5V CMOS Compatible Input
- Package : SDIP30-P-400-1.78 (TB62708N)

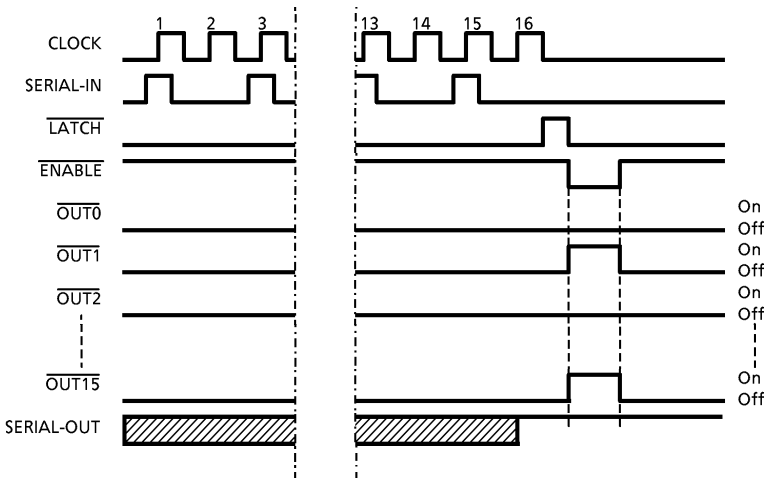
PIN CONNECTION (Top view)



BLOCK DIAGRAM



TIMING DIAGRAM



(Note) Latches are level sensitive, not rising edge sensitive and not synchronous CLOCK.
Input of $\overline{\text{LATCH}}$-terminal to "H" level, data passes latches, and input to "L" level, data hold latches.
Input of $\overline{\text{ENABLE}}$-terminal to "H" level, all output (OUT0~15) do off.

TERMINAL DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data for shift-register
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with "H" level input of $\overline{\text{LATCH}}$-terminal, and hold data with "L" level input.
6~9, 11~14, 17~20, 22~25	OUT0~15	Output terminals.
27	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of $\overline{\text{ENABLE}}$-terminal, and do on with "L" level input.
26	SERIAL-OUT2	Output terminal of a serial-data for next SERIAL-IN terminal.
28	SERIAL-OUT1	Output terminal of a serial-data for next SERIAL-IN terminal.
29	R-EXT	Input terminal of connects with a resister for to set up all output current.
30	V_{DD}	5V Supply voltage terminal
10, 15, 16, 20	V_{CC}	0~17V Supply voltage terminal for LED

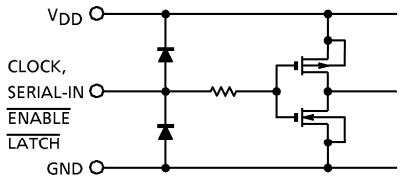
TRUTH TABLE

CLOCK	$\overline{LATCH}$	$\overline{ENABLE}$	SERIAL-IN	OUT0 ··· OUT7 ··· OUT15	SERIAL-OUT1	SERIAL-OUT2
UP	H	L	D_n	D_n ··· D_{n-7} ··· D_{n-15}	D_{n-15}	D_{n-16}
DOWN	H	L	D_n	D_n ··· D_{n-7} ··· D_{n-15}	No change	D_{n-15}
UP	L	L	D_{n+1}	No change (data hold)	D_{n-14}	No change
DOWN	L	L	D_{n+1}	No change (data hold)	No change	D_{n-14}
No Edge	H	L	D_{n+1}	D_{n+1} ··· D_{n-6} ··· D_{n-14}	No change	No change
No Edge	X	H	D_{n+1}	Off	D_{n-14}	No change

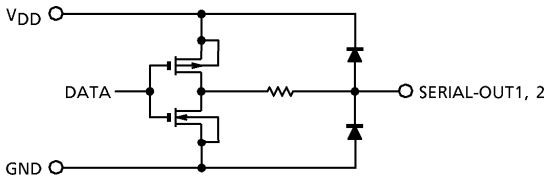
(Note) OUT0~15 = on in case of D_n = "H" level and OUT0~15 = off in case of D_n = "L" level. A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

1. $\overline{ENABLE}$, $\overline{LATCH}$, CLOCK & SERIAL-IN terminal



2. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Supply Voltage for LED	V_{CC}	0~17	V
Input Voltage	V_{IN}	−0.4~V_{DD} + 0.4	V
Output Current	I_{OUT}	−90	mA
Output Voltage	V_{CE}	−0.4~17.0	V
Clock Frequency	f_{CK}	15	MHz
GND Terminal Current	I_{VCC}	1440	mA
Power Dissipation	P_D	2.08 (ON PCB, Ta = 25°C)	W
		1.56 (FREE AIR, Ta = 25°C)	
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note) Ambient temperature delated above 25°C in the proportion of 16.64mW / °C on PCB. On PCB (100 × 150 × 1.6mm.Universal PCB).

RECOMMENDED OPERATING CONDITION (V_{DD} = 5V, Ta = −40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	4.5	5.0	5.5	V
Supply Voltage for LED	V_{CC}	GND Standard	0	—	17	V
Output Voltage	V_{OUT}	V_{CC} Standard	0	—	−17	V
Output Current	I_{OUT}	OUTn、DC 1 circuit	−5	—	−78	mA
	I_{OH}	SERIAL-OUT1, 2	—	—	1.0	
	I_{OL}	SERIAL-OUT1, 2	—	—	−1.0	
Input Voltage	V_{IH}	V_{DD} = 4.5~5.5V	0.7 V_{DD}	—	V_{DD} + 0.3	V
	V_{IL}		−0.3	—	0.3 V_{DD}	
$\overline{LATCH}$ Pulse Width	$t_{w\ LAT}$		100	—	—	ns
CLOCK Pulse Width	$t_{w\ CLK}$		50	—	—	ns
$\overline{ENABLE}$ Pulse Width	$t_{w\ EN}$		1000	—	—	ns
Set-Up Time	t_{setup}		50	—	—	ns
Hold Time	t_{hold}		30	—	—	ns
Clock Frequency	f_{CLK}	Cascade operation	—	—	10.0	MHz
Power Dissipation	P_D	ON PCB, Ta = 85°C	—	—	1.08	W

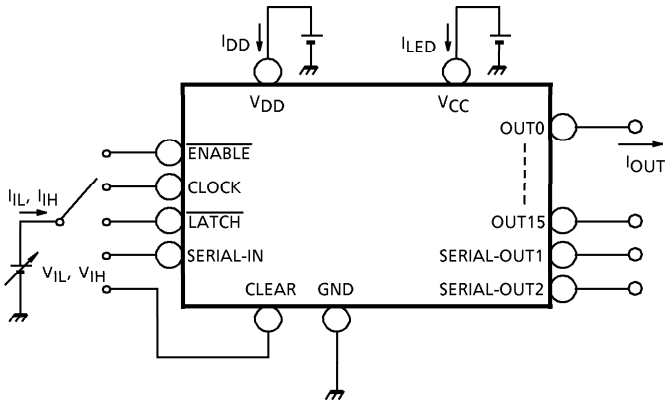
ELECTRICAL CHARACTERISTICS (V_{CC} = 17V, V_{DD} = 5V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}	—	—		0.7 V_{DD}	—	V_{DD}	V
	"L" Level	V_{IL}	—	—		GND	—	0.3 V_{DD}	
Output Leakage Current		I_{LEAK}	—	V_{CC} = 17.0V		—	—	−10	μA
Output Voltage	S-OUT	V_{OL}	—	I_{OL} = 1.0mA		—	—	0.4	V
		V_{OH}	—	I_{OH} = −1.0mA		4.6	—	—	
Output Current 1		I_{OL1}	—	V_{OUT} = V_{CC} − 2.0V	R_{EXT} = 360Ω (Include skew)	−66.3	−78	−89.7	mA
	Current Skew	ΔI_{OL1}	—	V_{OUT} = V_{CC} − 2.0V	R_{EXT} = 360Ω	—	±1.5	±6.0	%
Supply Voltage Regulation		% / V_{DD}	—	R_{EXT} = 360Ω, Ta = −40~85°C		—	1.5	5.0	% / V
Supply Current 1	"OFF"	$I_{DD\ (off)}$	—	R_{EXT} = OPEN, OUT0~15 = off		—	0.6	1.2	mA
	"ON"	$I_{DD\ (on)}$	—	R_{EXT} = 360Ω, DATA = "H" OUT0~15 = on		—	10.0	15.0	
Supply Current 2	"OFF"	$I_{CC\ (off)}$	—	R_{EXT} = 360Ω, ALL DATA = "L" OUT0~15 = off		—	1.0	2.0	mA
	"ON"	$I_{CC\ (on)}$	—	R_{EXT} = 360Ω, ALL DATA = "H" OUT0~15 = on		—	1260	—	mA

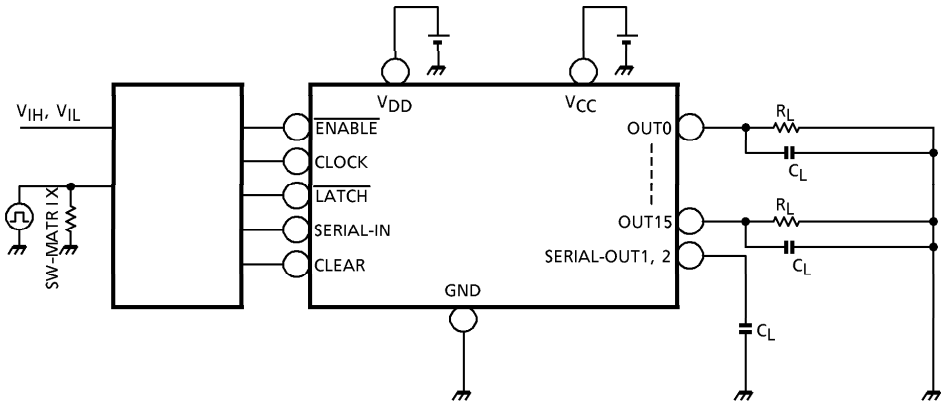
SWITCHING CHARACTERISTICS (Ta = 25°C, unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLK-OUTn	t_{pLH}	—	{CLK, LATCH & ENABLE to t_{pLH} & t_{pHL} : 50% to 50%} V_{DD} = 5.0V, V_{CC} = 17.0V V_{OUT} = V_{CC} − 2.0V V_{IH} = V_{DD} V_{IL} = GND R_{EXT} = 360Ω R_L = 300Ω	—	200	500	ns
	$\overline{\text{LATCH}}$-OUTn				—	200	500	
	$\overline{\text{ENABLE}}$-OUTn				—	200	500	
	CLK-SOUT				—	30	70	
Propagation Delay Time ("H" to "L")	CLK-OUTn	t_{pHL}	—		—	200	500	ns
	$\overline{\text{LATCH}}$-OUTn				—	200	500	
	$\overline{\text{ENABLE}}$-OUTn				—	200	500	
	CLK-SOUT				—	30	70	
Pulse Width	CLK	$t_{w\ CLK}$, CLK	—		—	20	30	ns
	LATCH	$t_{w\ LAT}$, LAT	—		—	10	25	
Set-Up Time for $\overline{\text{LATCH}}$ & CLOCK		$t_{setup\ LAT}$	—		—	25	50	ns
Hold Time for $\overline{\text{LATCH}}$ & CLOCK		$t_{hold\ LAT}$	—		—	0	15	ns
Maximum CLOCK Rise Time		t_r	—		—	—	10	μs
Maximum CLOCK Fall Time		t_f	—		—	—	10	μs
Output Rise Time		t_{or}	—		150	300	600	ns
Output Fall Time		t_{of}	—		150	300	600	ns

DC CHARACTERISTICS TEST CIRCUIT



AC CHARACTERISTICS TEST CIRCUIT

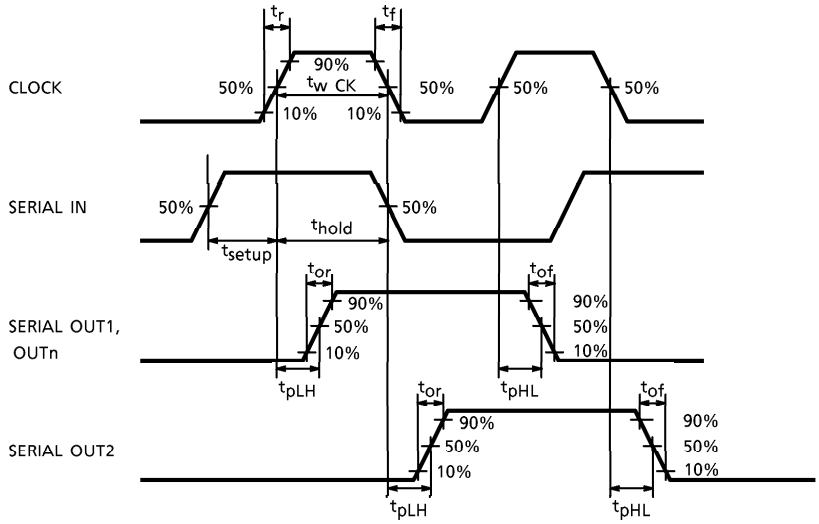


PRECAUTIONS for USING

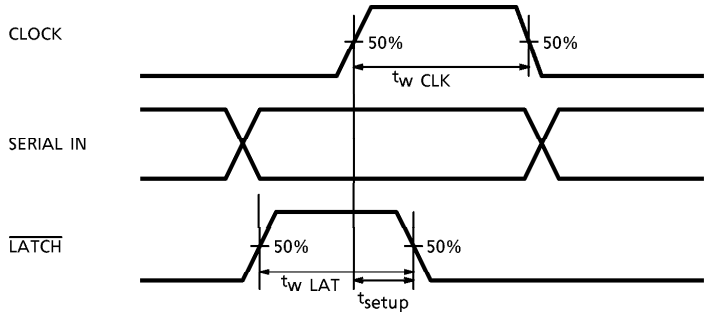
Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

TIMING WAVEFORM

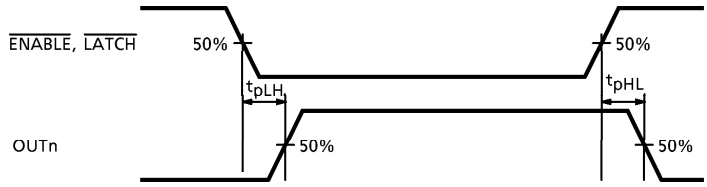
1. CLOCK-SERIAL OUT, OUTn

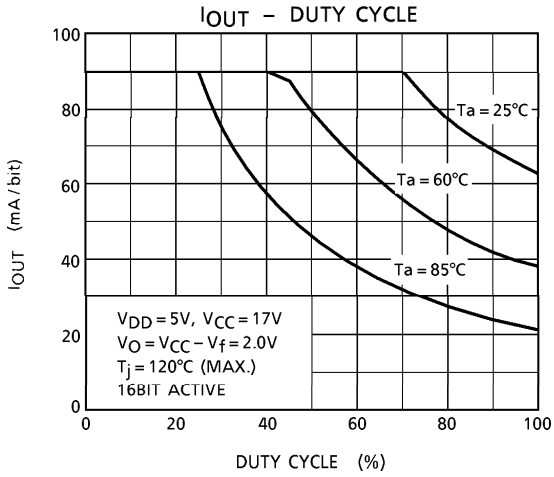


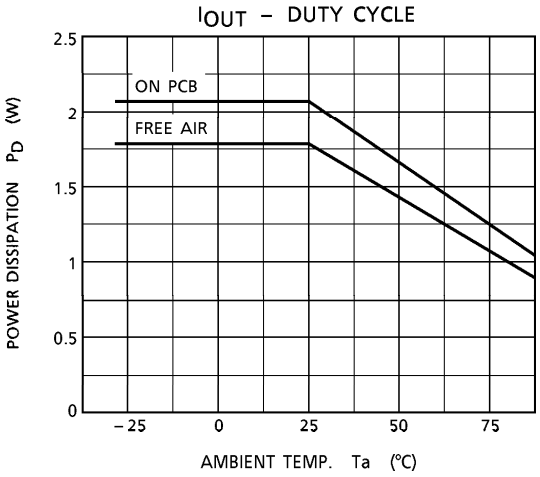
2. CLOCK-$\overline{\text{LATCH}}$



3. $\overline{\text{ENABLE}}$, $\overline{\text{LATCH}}$-OUTn

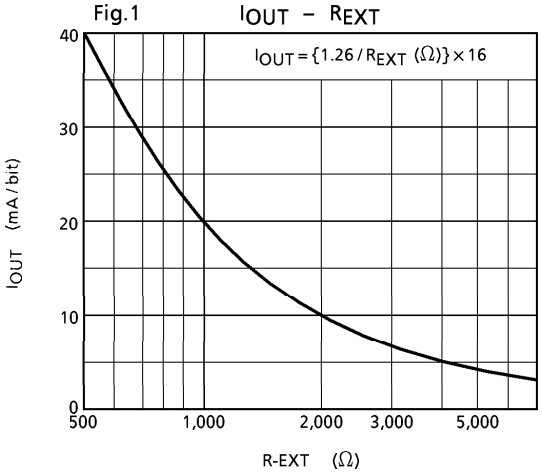






LED DRIVER TB6270X SERIES APPLICATION NOTE

Fig.1 I_{OUT} – R_{EXT}



[1] Output current (I_{OUT})

I_{OUT} is set by the enternal resistor (R-EXT) as shown in Fig.1.

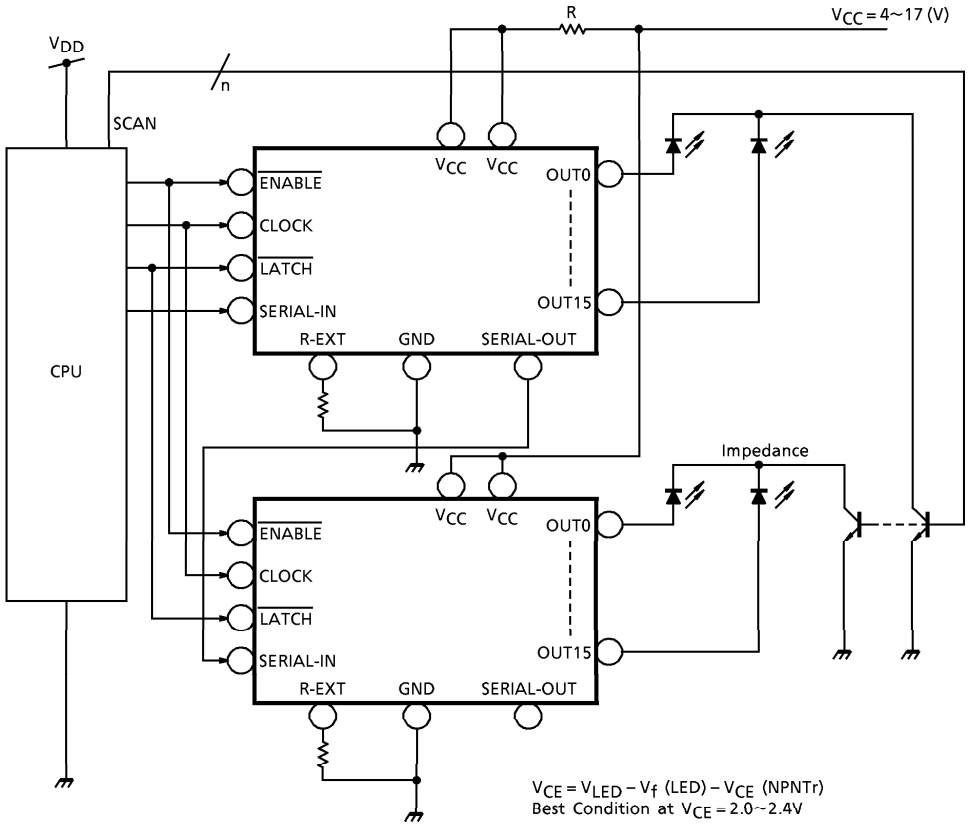
[2] Total supply voltage (V_{LED})

This device can operate 2.0~2.3V (V_O).
When a higher voltage is input to the devide, the excess voltage is consumed inside the device, that leads to power dissipation.
In order to minimize power dissipation and loss, we would like to recommended to set the total supply voltage as shown below.

V_{LED} (Total supply voltage)
$= V_{CE}$ (Tr V_{sat}) + V_f (LED Forward voltage) + V_O (IC supply voltage)

When the total supply is too high considering the power dissipation of this devide, an additional R can decrease the supply voltage (V_O).

APPLICATION

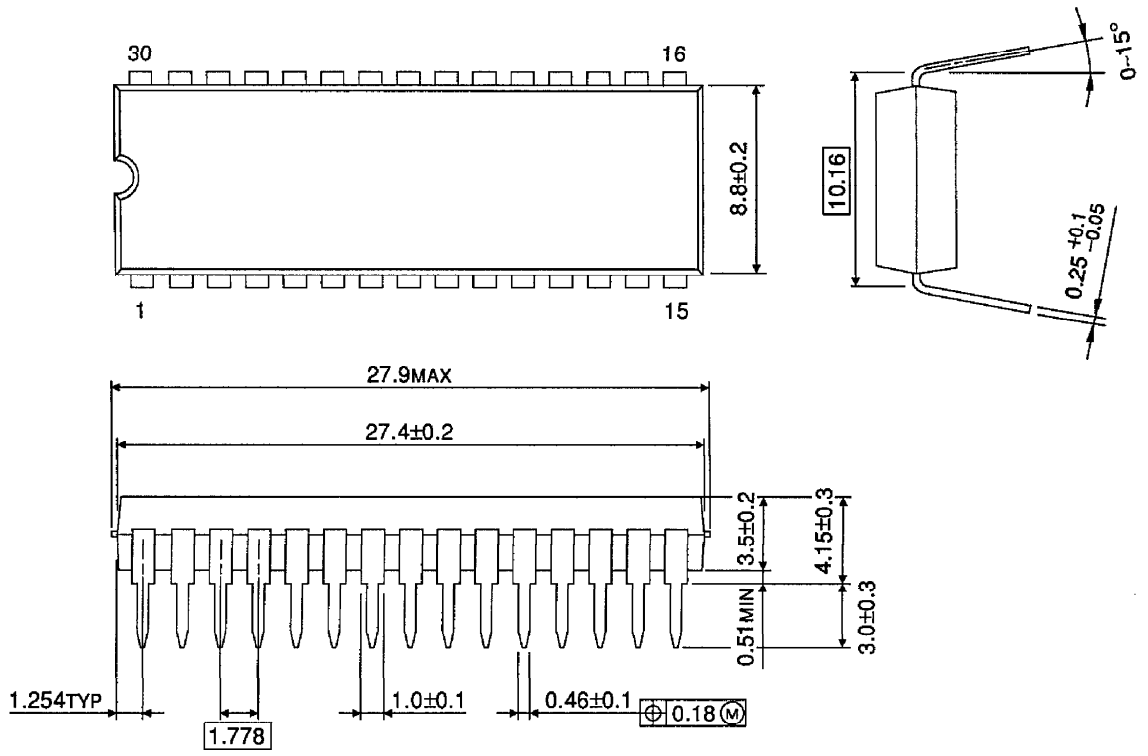


[3] Pattern layout

This device owns only one ground pin that means signal ground pin and power ground pin are common.
If ground pattern layout contains large inductance and impedance and the voltage between ground and $\overline{\text{LATCH}}$, CLOCK terminals exceeds 2.5V by switching noise in operation, this device may miss-operate. So we would life you to pay attention to pattern layout to minimize inductance.

OUTLINE DRAWING

SDIP30-P-400-1.78 Unit : mm



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