TBA990

PAL TV CHROMA DEMODULATOR

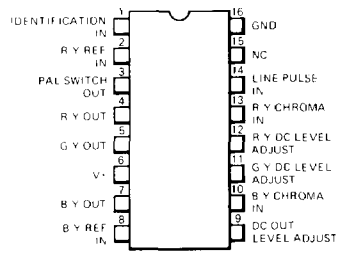
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA990 is an integrated color demodulator circuit for color television receivers incorporating two active synchronous demodulators for the R-Y and B-Y chrominance signals, a matrix (producing the G-Y color difference signal), PAL phase switch and flip-flop. It is suitable for dc coupled drive to the picture tube. When associated with the matrix integrated circuit (TBA530) it provides RGB output signals.

Special attention has been given in the design to minimizing dc level drift with temperature and direct interface with TBA530, TBA540 and TBA560. It is constructed on a single silicon chip using the Fairchild Planar* process.

- **DOUBLE BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **INTERNAL PAL SWITCH**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**
- **MINIMIZED DC LEVEL DRIFT WITH TEMPERATURE**
- **SIMULTANEOUS DC ADJUSTMENT ON CHROMA OUTPUTS**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

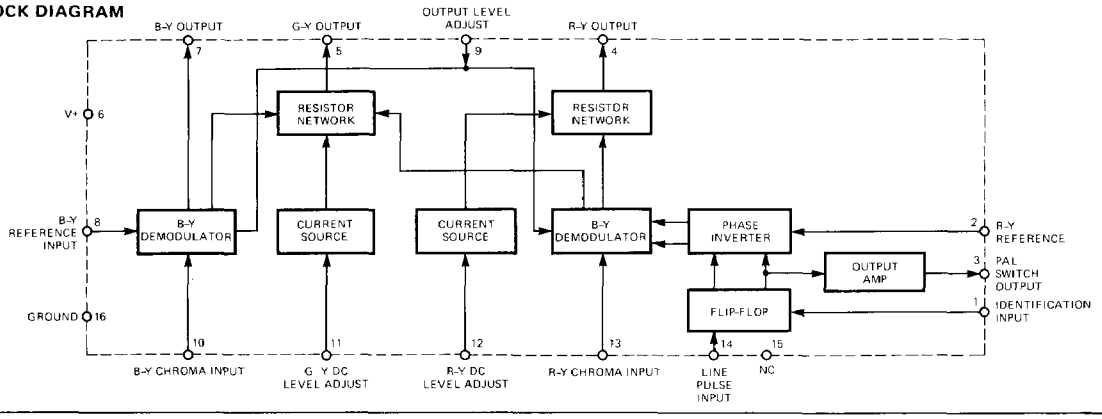
TYPE	PART NO.
990	TBA990
990Q	TBA990Q†

†Not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Internal Power Dissipation	300 mW
Operating Ambient Temperature	−20°C to +60°C
Storage Temperature	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM



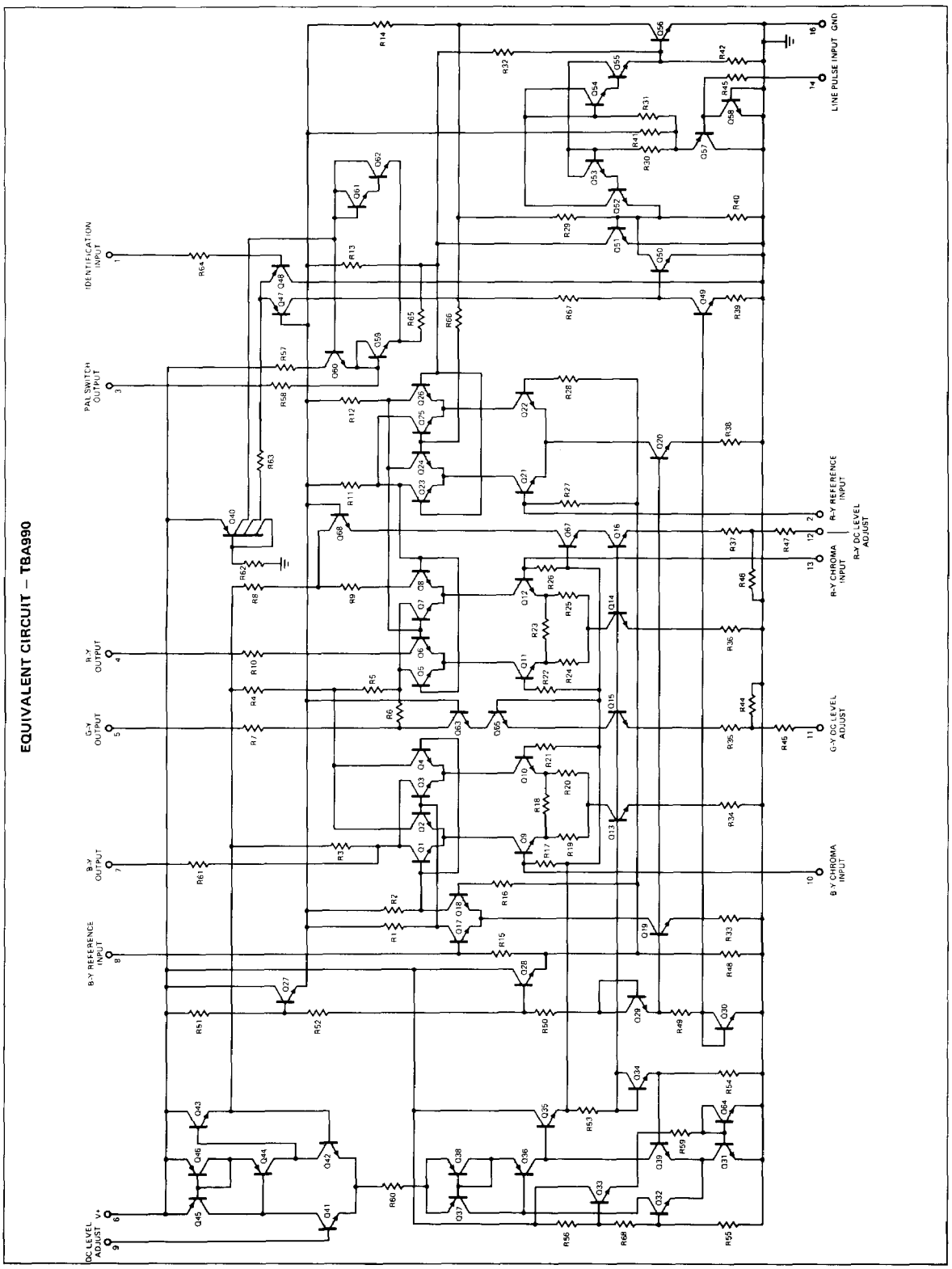
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12V$, See Test Circuit, unless otherwise specified.

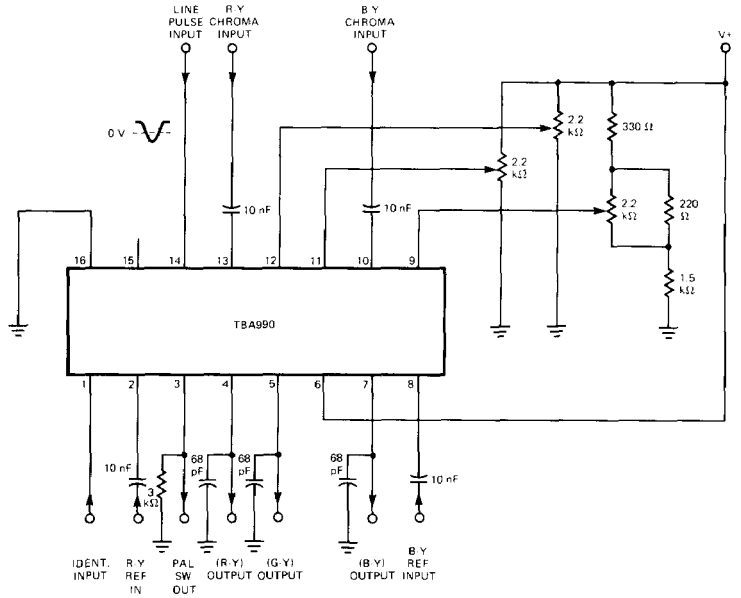
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_6)			17		mA
Color Difference Gain					
R-Y Channel ($A_{V4/13}$)	$V_{10} = V_{13} = 50$ mV pk-pk		3.8		V/V
B-Y Channel ($A_{V7/10}$)	f = 4.4 MHz		6.8		V/V
G-Y Channel	(Note 3)		(Note 1)		
Maximum Color Difference Output Voltage (Notes 2, 3)					
R-Y Output ($V_{4\ pk\text{-}pk}$)	(Notes 2, 3)	1.6			$V_{pk\text{-}pk}$
B-Y Output ($V_{7\ pk\text{-}pk}$)		2.0			$V_{pk\text{-}pk}$
G-Y Output ($V_{5\ pk\text{-}pk}$)		0.9			$V_{pk\text{-}pk}$
Color Difference DC Output Voltage					
R-Y Output (V_4)			7.5		V
B-Y Output (V_7)			7.5		V
G-Y Output (V_5)			7.5		V
Input Resistance of Chroma Inputs (R10, R13)	$V_{10} = V_{13} = 20$ mV rms (Sinusoidal) f = 4.4 MHz	800			Ω
Input Capacitance of Chroma Inputs (C10, C13)				10	pF
Output Resistance at Color Difference Terminals (R4, R5, R7)			3.0		kΩ
Input Resistance of Reference Inputs (R2, R8)			5.0		kΩ
Peak-to-Peak PAL Switch Output Voltage ($V_{3\ pk\text{-}pk}$)	(Note 4)		3.5		$V_{pk\text{-}pk}$
Activation Threshold Voltage (V_1)	Identification Circuit is Active	6.5			V
Deactivation Threshold Voltage (V_1)	Identification Circuit is Inactive			5.5	V
Identification Input Current (i_1)		−100			μA
Output Voltage Drift ($\Delta T_A = 40°C$)					
DC Output Voltage (V_4)		−50		+50	mV
DC Output Voltage (V_7)	$V_{11} = V_{12} = 6$ V	−50		+50	mV
DC Output Voltage (V_5)		−50		+50	mV
Relative DC Output Voltage Change between Channels		−20		+20	mV

NOTES:
1. G-Y output is typically equal to −0.51 (R-Y) −0.19 (B-Y).
2. Increase V_{10} and V_{13} until gain is equal to 0.7 of small signal gain.
3. Reference input ($V_{2\ pk\text{-}pk}$ and $V_{8\ pk\text{-}pk}$) range is 0.5 V to 2.0 V. (typically 1.0 V).
4. $f_o = 0.5 \times$ line pulse frequency; $V_{14} = 2.0$ to 5.0 $V_{pk\text{-}pk}$ (See application information).

EQUIVALENT CIRCUIT – TBA990



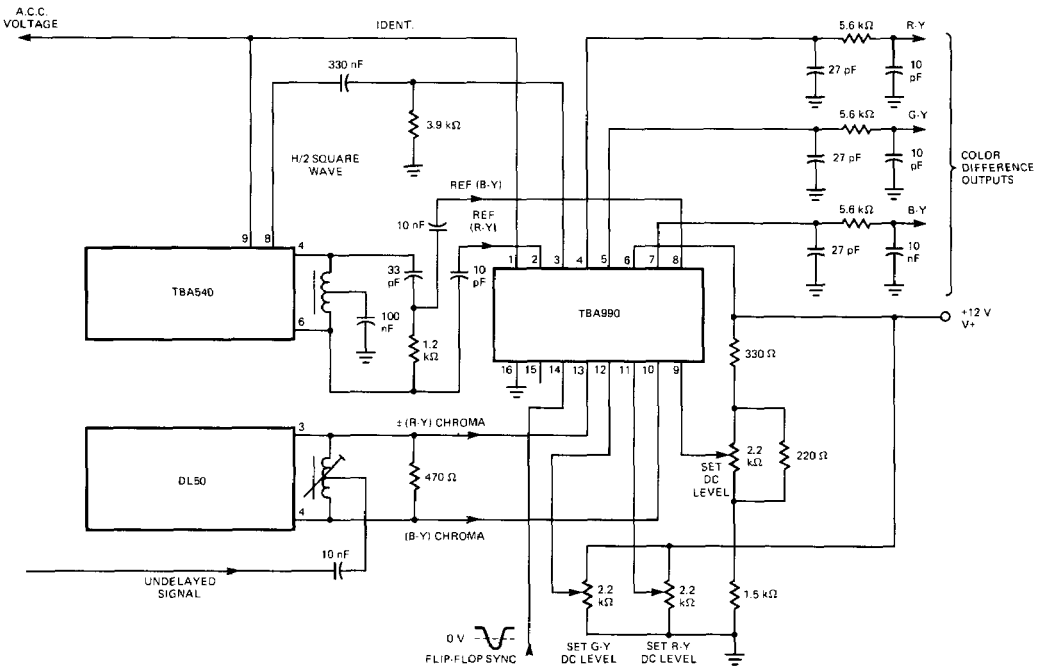
TEST CIRCUIT



$V_{11} = V_{12} = 6.0$ V

$V_9 = 9.5$ V

APPLICATION INFORMATION



APPLICATION INFORMATION (Cont'd)

The function is quoted against the corresponding lead number.

IDENTIFICATION BIAS

1. The PAL flip-flop is stopped, for identification purposes, when the voltage on pin 1 increases above 6 V. This threshold is internally generated and has a proportional behavior with the 12 V supply voltage. The threshold level of 6 V is chosen to match the output characteristic of the TBA540 and has sufficiently high safety margin above the zero chroma signal level of 4 V to eliminate spurious identifying.

R-Y SUBCARRIER REFERENCE INPUT

2. A 1 V pk-pk signal is required via a dc blocking capacitor. Under no circumstances should this signal be less than 0.5 V pk-pk. The input resistance at this pin is typically 5 kΩ.

PAL SQUARE WAVE CIRCUIT

3. The amplitude is 3.5 V pk-pk from an emitter follower.

R-Y SIGNAL OUTPUT (G-Y at pin 5 and B-Y at pin 7)

4. These outputs require no external dc loads except that direct connection must be made via the low pass filter to the appropriate pins on the RGB matrix TBA530.

   The signals produced are in the following ratios:

   $V_{B-Y} = 1.78\ V_{R-Y}$

   (a) $V_{G-Y} = 0.85\ V_{R-Y}$

   (b) $V_{G-Y} = 0.17\ V_{R-Y}$

   Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix.

   Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

   The dc levels should each be adjusted, starting with the (B-Y), to +7.5 V at nominal supply voltage. However, in a complete circuit using the TBA530 matrix and feedback integrated circuit these dc levels will be adjusted to give the correct setting of the picture tube drive black levels. The changes in dc level with supply voltage are approximately linear and track together.

   The unwanted products of demodulation occurring in the color difference outputs are chiefly 8.86 MHz and harmonics together with a small amount of 4.43 MHz due to possible unbalance in the demodulators. To avoid possible troubles in the receiver because of the radiation of these demodulation products from the RGB drive circuits, filters must be employed in each of the color-difference outputs from the TBA990. The roll-off should begin at about 1.5 MHz and attention should be given to the parallel resonance of the inductors to ensure that no serious attenuation will occur at less than 1.5 MHz. Also, some advantage may be secured by designing the inductor so that the dip due to its self-resonance occurs at about 4.43 MHz.

G-Y SIGNAL OUTPUT

5. See pin 4.

POSITIVE SUPPLY

6. The maximum allowable voltage on this pin is 13.2 V.

B-Y SIGNAL OUTPUT

7. See pin 4.

B-Y SUBCARRIER REFERENCE INPUT

8. The requirements here are identical with those for pin 2.

DC LEVEL SETTING FOR B-Y OUTPUT SIGNAL

9. See test circuit diagram, and also pin 4.

CHROMINANCE B-Y INPUT SIGNAL

10. An input signal of approximately 360 mV pk-pk (color bars) is required at this pin. The input impedance is greater than 800 Ω and the input capacitance is less than 10 pF.

DC LEVEL SETTING FOR G-Y OUTPUT SIGNAL

11. See test circuit diagram, and also pin 5.

DC LEVEL SETTING FOR R-Y OUTPUT SIGNAL

12. See test circuit diagram, and also pin 4.

CHROMINANCE R-Y INPUT SIGNAL

13. An input signal of approximately 500 mV pk-pk (color bars) is required at this pin. The input imedpance is the same as for pin 10.

LINE PULSE INPUT (flip-flop synchronizing)

14. A waveform derived from the line timebase can be used for synchronizing providing that its amplitude lies between 2 V and 5 V pk-pk. The trigger point occurs where the negative going edge crosses approximately +0.6 V.

NOT CONNECTED

15. This pin should not be used for external connections.

GROUND

16. See pin 16.