TC211
Timing of Full Frame CCD Image Sensor

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Abstract

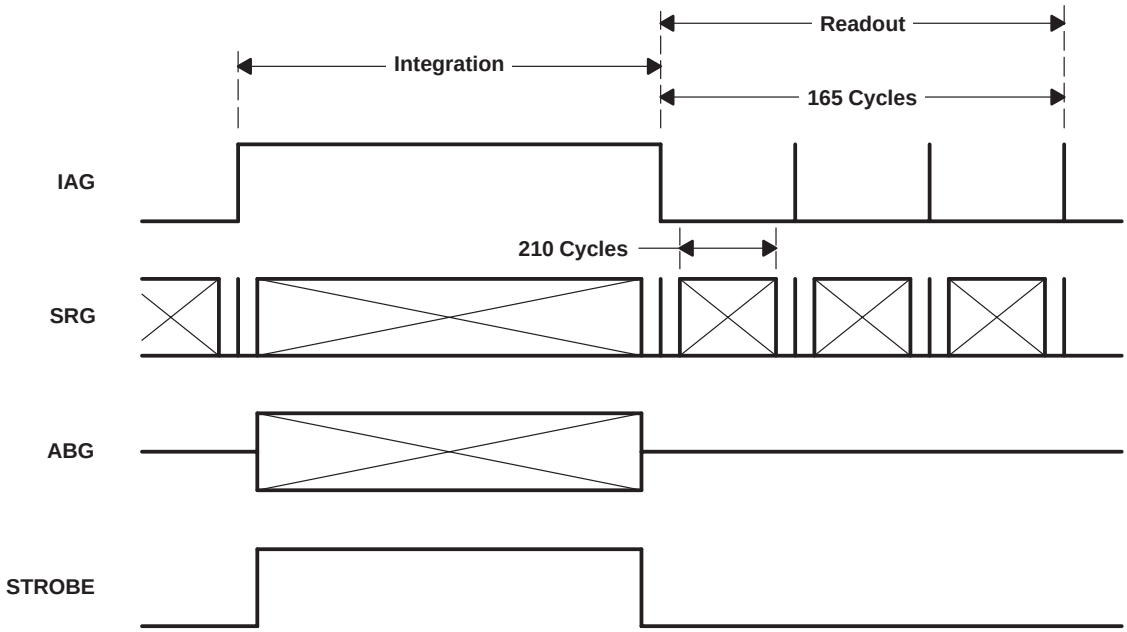
This application reports aids in the design of timing for Texas Instruments (TI™) full frame charge coupled device (CCD) image sensors. It also includes the timing needed to perform correlated double sampling (CDS) and antiblooming. The timing presented here represents only one method of operation, although the TI full frame CCD image sensor can be used in a variety of applications. This report gives a general explanation of CCD operation so that camera designers can customize the timing necessary for their application. The TI TC211 full frame CCD image sensor was used in the TCK-211 evaluation board to illustrate full frame CCD timing compatible with the EIA RS-170 standard. The scope pictures were taken with a Tektronix™ C-30 series camera on a Tektronix 2467B 400 MHz scope with a TEK™ P6137 10X probe. The probe was grounded using a lead wrapped around the probe and soldered to ground in close proximity to the signal pin.

Introduction

This application note was written to aid in the design of timing for TI full frame CCD image sensors. It also includes the timing needed to perform correlated double sampling (CDS) and antiblooming. It should be understood that the timing presented here is only one method of operation and the CCD sensor can be used in a wide variety of applications. The objective is to give a general understanding of CCD operation to the camera designer so that they can customize the timing necessary for their application.

Full Frame CCD Timing (TC211)

The TI full frame CCD sensor has an image area consisting of an array of pixels and a serial register, as illustrated by the TC211. The operation of the full frame CCD consists of an integration period and a readout period, which contains a line transfer and a serial readout. For this timing discussion, the TI TCK-211 evaluation board was used with the TC211 CCD image sensor, which has a resolution of 165 rows by 192 pixels. the TCK-211 evaluation board is compatible with the EIA RS-170 standard, which requires 244 horizontal television lines. This evaluation board centers the image in the raster and extends the horizontal and vertical blanking time. The timing diagrams for these periods are illustrated in Figure 1.



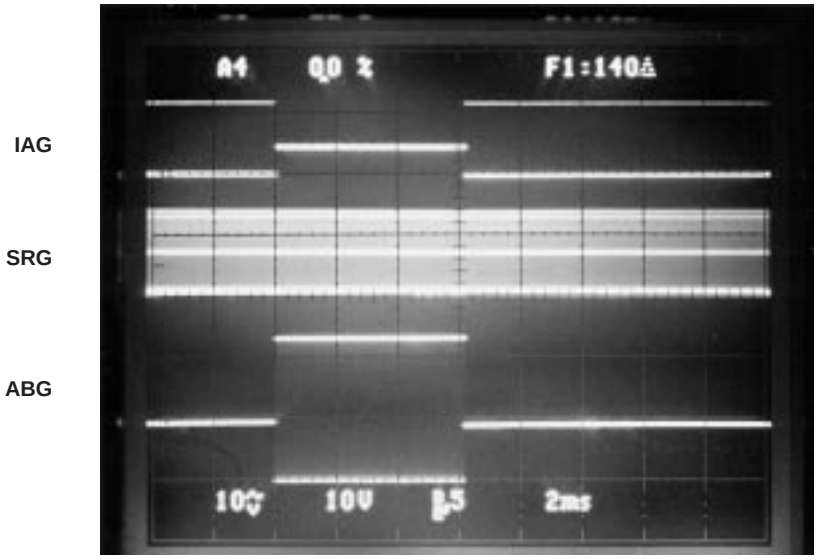


Figure 1. Timing Diagrams for the TC211

Eliminating Smear

In full frame devices, it is necessary to perform the readout period during a dark condition to eliminate smearing effects. To eliminate smearing effects, it is necessary to use a strobe light or a mechanical shutter. The strobe light should fire or the mechanical shutter should open during the integration time and allow the readout period to occur during this dark condition. The timing for the strobe light can be seen in Figure 1.

Integration Period

As light enters the CCD, the photons generate electrons which are stored in the wells of each pixel. The length of the integration period determines the number of electrons that are accumulated. As shown in Figure 1, the IAG pin is held to a mid-level voltage during integration, which allows electrons to be accumulated in both the virtual wells and the clocked wells. This accumulation in both virtual and clocked wells is necessary to perform a half pixel shift to increase the resolution in an interlaced readout. This half pixel shift is further explained in the Interlace Operation in TI Virtual-Phase CCD Image Sensors Application Report.

During the integration period, antiblooming is activated to protect saturated wells from overflowing to the surrounding wells. Antiblooming should be clocked at 2 MHz for maximum antiblooming protection. This timing is shown in Figure 1 on the ABG line. The SRG line is also clocked during the integration period to keep the detection node charged correctly and prevent dark current buildup in the serial register.

Readout Period

The readout period consists of a line transfer and a serial readout. These processes are accomplished using clock pulses.

Line Transfer

The readout period begins with a line transfer. This transfer moves charge from one row of the image area to the row below it. Charge in the last row in the image area is transferred to the serial register. Any charge that was in the serial register is transferred to the clearing drain. After the pixels are read out serially, the next line transfer occurs.

A line transfer is accomplished through a clock pulse on IAG and SRG, as shown in Figure 2. The ABG pin must be set to an intermediate voltage of about –2.5 V to transfer charge across the antiblooming gate. The critical edge in this transfer is the IAG falling edge, which must occur at least 350 ns (t3) before the SRG falling edge. If the time between falling edges is too small, the charge transfer efficiency drops. To achieve complete charge transfer from pixel to pixel, the pulse width must be at least 350 ns (t_{w1} and t_{w2}). Also, the line transfer pulses must be at least 70 ns (t1) from the serial readout pulses on the SRG. This timing is illustrated in Figure 2.

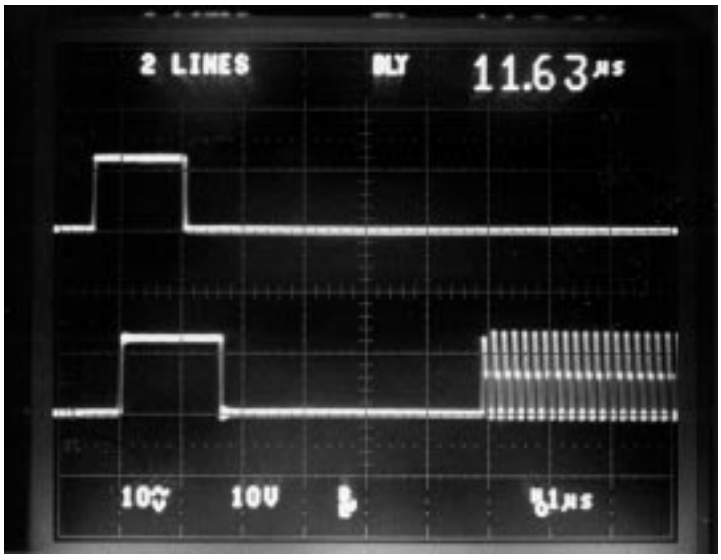


Figure 2. Line Transfer Timing

Serial Readout

Serial readout is the movement of charge from one pixel to the next in the serial register. The charge that is in the first pixel of the register is moved onto the detection node. This serial transfer is accomplished through clock pulses on SRG, as shown in Figure 3. The SRG in this figure is read out at 6.1 MHz, although it can be read out at any speed up to a maximum of 10 MHz.

(a)

(b)

Figure 3. (a) SRG and OUT in Dark Condition
(b) SRG and OUT in Saturated Condition

Correlated Double Sampling (CDS)

The SRG timing in Figure 3 utilizes a tri-level clock which is necessary for off-chip CDS. In the TC211 sensor, the detection node is reset by the SRG line and not by a separate reset line. When SRG is at its high level, the detection node is reset when the SRG moves to a mid-level voltage, this turns off the reset transistor but this voltage is not low enough to transfer charge to the detection node. This is the point where the reset voltage level is sampled. SRG is then set to the low level voltage which transfers charge to the detection node. At this point, a second sample and hold is used to measure the voltage level after the charge transfer. The active video level is obtained by subtracting these two voltages. Figure 4 shows this timing with a block diagram of one possible CDS circuit.

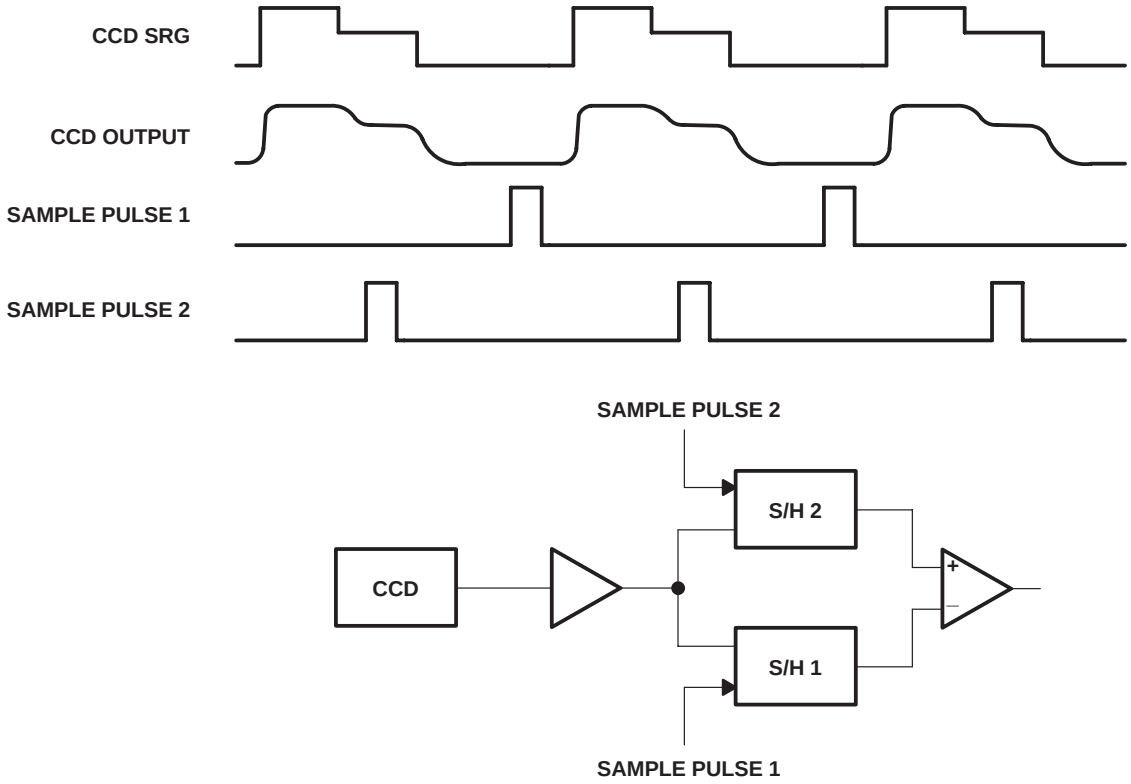


Figure 4. Correlated Double Sampling