TOSHIBA

0.13μm (Ldrawn=0.11μm) CMOS ASIC TC280 Family

NEW PRODUCT GUIDE

AN IDEAL SYSTEM-LEVEL INTEGRATION (SLI) PLATFORM TO ENABLE THE BROADBAND AGE

Premium ASIC for high-performance and ultra-low power applications

TC280 Family

Broadband Internet access is rapidly reaching a huge number of people. With worldwide Internet traffic projected to double in just six months, the computer and communications industries are modernizing the telecommunications infrastructure at a furious pace by using xDSL, wireless and optical fiber technologies.

The TC280 family is meant to be used as a system-level integration (SLI) platform for next-generation high-performance products that will enable real broadband Internet connections.

The new CMOS3 process technology not only offers unprecedented embedded DRAM capability, but also permits easy mixing of analog and application-specific IP cores on the same chip. The TC280 family capitalizes on copper technology, low-k dielectric and the industry's most aggressive 0.13-micron-generation process with 0.11-micron-drawn gate lengths. The process supports up to eight layers of copper metal interconnect for TC280 logic densities up to 206,000 usable gates/mm^2.

The design methodology used to create megagate ASIC designs has already been silicon-proven for the previous 0.14-micron-drawn gate TC260 family to provide maximum design throughput and quality.

Toshiba's TC280 family offers an ideal solution for multimedia and high-speed networking applications, or any other application where both speed and low power consumption are important such as PDAs and portable devices.

Features and Benefits

Ultra-High Density and Ultra-Low Power

The TC280 family is fabricated using Toshiba's new CMOS3 process.

■ Design Rule

World-class 0.13-micron generation with 0.11-micron-drawn-gate CMOS process

■ Copper Interconnect

Up to eight levels of copper wiring combined with low-k dielectric

Improvements over the TC260 Family (Ldrawn=0.14 µm)

1. **X1.7 improvement in logic density**
2. **30% power savings per gate**
3. **20% reduction in gate delay**

Cell Library

■ Primitive Cells

The TC280 family offers synthesis-friendly primitive cells for both high-performance- and low-power-intended chip designs. The ability to mix and match the cells of both standard and high-speed libraries delivers ultimate results.

■ I/O Cells

The TC280 family offers I/O cells in two shapes: standard-height I/O cells for pad-limited designs and low-height I/O cells for core-limited designs.

■ SRAM

High-speed SRAM: Max. 600 MHz, 1-Port, 2-Port
High-density SRAM: Half the size of conventional SRAMs, 1-Port, 2-Port

IP Cores

Toshiba supports an ever-growing selection of IP cores compliant with the VSI standard.

MPU:	TX System RISC, ARM processors
Protocol Controllers:	IEEE1394, USB, IrDA
High-Speed I/O:	PCI, AGP, USB, LVDS, Direct RAC, HSTL
Multimedia:	NTSC/PALVideo Encoder, JPEG, MPEG
Networking:	Ethernet
Analog Functions:	ADC, DAC, PLL
Memory:	DRAM, SRAM, FIFO, ROM

High-Bandwidth SD-DRAM
(Compliant with the synchronous DRAM standard)

Max. Clock Rate:	200 MHz
Max. Data Rate:	6.45 GB/s
Clock Cycle:	5 ns
Size:	2 to 32 Mbits per macro

Fast-Access FA-DRAM
(High-density design for SRAM replacement)

Random Access Time:	10 ns
I/O Bit Width:	256 bits
Size:	2/4/8 Mbits per macro

■ DRAM Core Overview

The embedded DRAM cores are based on Toshiba's leading trench capacitor technology that doesn't degrade logic performance. The DRAM Generator can automatically construct fully assembled DRAMs with a specified size. Embedded DRAM cores provide high memory bandwidth with a bus width selectable from 64, 128 and 256 bits. They also feature low power dissipation due to lower-capacitance on-chip connections and low switching noise on the data bus between memory and logic. Toshiba offers two types of DRAM cores: one targeted for high bandwidth, the other for fast (low-latency) access.

Design Methodology for Multimillion-Gate and High-Performance ASICs

Our megagate design methodology has a solid track record with the 0.14-micron-drawn gate TC260 family. To help customers reduce design time and iterations, Toshiba continues to innovate and deliver new ASIC design solutions.

1 Hierarchical Design

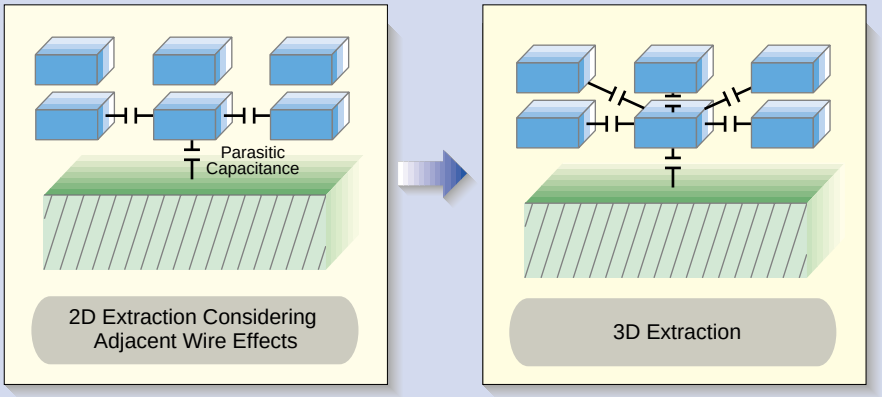
Toshiba provides support for hierarchical design approaches combined with a timing-driven gate design flow. This allows a design team to create sub-blocks in parallel and resolve timing problems at the block level.

2 Predictable Timing Closure

The advanced synthesis technique utilizes physical information to generate accurate wire models during RTL synthesis. Timing-driven layout leverages the power of this synthesis capability to tie logical and physical design together in a manner that enables rapid timing closure.

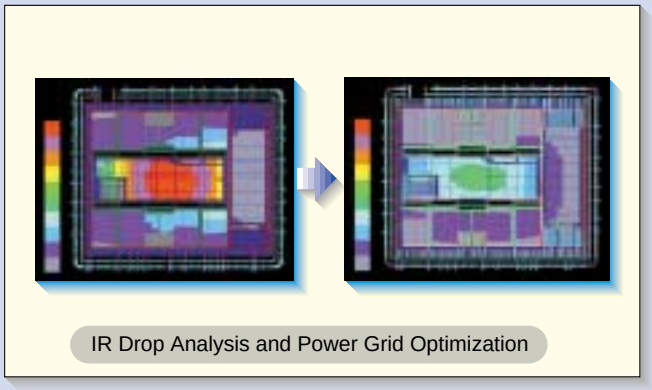
3 3D Capacitance Extraction

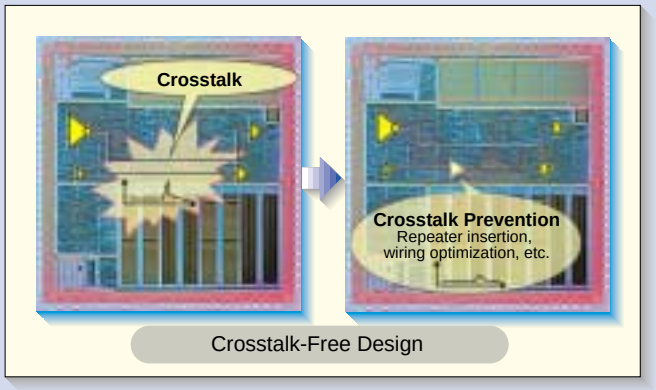
In today's deep-submicron ASICs, delays caused by interconnect are becoming increasingly dominant over gate delays. To accurately calculate deep-submicron delays, new techniques must be used. Toshiba employs 3D capacitance extraction to improve the accuracy of timing estimates for multi-layer metal processes.



4 Solutions to Signal Integrity Problems

To ensure signal integrity, Toshiba optimizes power grid routing, based on IR drop estimation, early in the design cycle. Additionally, electromigration, antenna effects, hot carrier and electromagnetic interference are all considered. The TC280 design flow also embraces crosstalk analysis and elimination.


IR Drop Analysis and Power Grid Optimization



Crosstalk-Free Design

Packaging

Toshiba offers the industry's most diverse portfolios of advanced packaging solutions, enabling high-performance system-level integration (SLI) ASICs. Four-layer EPBGAs with 352 to 576 pins address electrical requirements; FC-BGAs with over 800 pins offer the highest pin count and density; PFBGAs, also known as chip-scale packages, are offered with pin counts from 109 to 265 pins; TBGAs with 256 to 1849 pins combine the fine die pad pitch interconnect advatanges of TAB with the assembly ease of BGAs; QFPs with 44 to 304 pins offer a robust set of cost/performance, thermal and low-profile options.

General Product Specifications

Design Rule	0.13-µm generation (with 0.11-µm-drawn gate), CMOS process, 8-layer Cu
Power Supply	VDD = 1.5 V (core); 2.5V (analog); 2.5 V or 3.3 V (I/O)
Gate Delay (F/O=1, CIVX2 Gate)	14 ps (Standard Library), 11 ps (High-Speed Library) * Two types of transistors are available with different threshold voltages.
Gate Density	206 kgates/mm^2 (usable gates in cell-based design)
Power Dissipation	10 nW/MHz/gate (CIVXL gate)

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