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Product Brief

TC358762 De-serializer Display Bridge

Highlights

- De-serializer display bridge for connectivity of panels using legacy parallel interface to the Baseband or Application Processors with MIPI® Display Serial Interface.
- Solutions are based on the latest versions of industry standard MIPI DSI 1.01 interface to ensure high speed data rates of up to 800 Mbps per lane.
- Legacy interfaces such as MIPI DPI and MIPI DBI are also supported.
- Applicable to a range of mobile product platforms such as smartphones, netbooks, smartbooks, MIDs and PNDs.

Description

The Toshiba TC358762XBG de-serializer display bridge is optimized for mobile handsets using the Host processor with MIPI® DSI (Display Serial Interface) connectivity. The TC358762XBG de-serializes the high-speed serial data stream from the Host via DSI interface into a parallel stream to output to the display panel.

The TC358762XBG bridge supports MIPI DSI dual lane with up to 800 Mbps per data lane. The bridge supports legacy display interface protocols such as MIPI DPI (Display Pixel Interface) and MIPI DBI (Display Bus Interface) to the panel side. The parallel output bus can either be a DPI or DBI bus and they are mutually exclusive. The bridge supports both DCS (Display Command Set) and generic commands. A 1024 x 24 dual port video buffer is used to buffer the burst video data received from DSI link before transmitting out from DPI/DBI port.

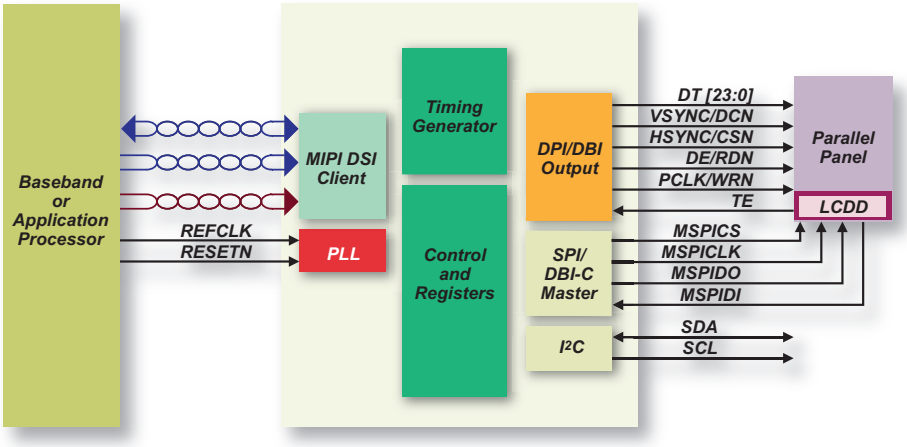
The TC358762XBG is a 64-pin device in small 5 mm x 5 mm x 1.0 mm sized package suitable for mobile applications.

The Toshiba proprietary Magic Square algorithm can interpolate RGB666 to pseudo RGB888 image data to display up to 16 million colors.

Features

- MIPI standard implemented
  - MIPI DSI version 1.01, Feb 2008
  - MIPI D-PHY version 0.9, Oct 2007
  - MIPI DPI version 2.0, Sep 2005
  - MIPI DBI-2 version 2.0, Nov 2005
  - MIPI DCS version 1.02, Dec 2008

System Block Diagram of TC358762XBG



The TC358762XBG supports data transfer from input port to output port as shown in the following use case scenarios:

Use Case 1: MIPI DPI Mode: The DPI interface is used to transfer video data and the SPI interface is used to transfer command data. The DSI link operates in non-burst mode.

Use Case 2: CPU Mode: Both video and command data are routed via the DBI interface.

Use Case 3: DBI-B Mode: Both video and command data are routed via the DBI interface. The TC358762 switches to DBI-B mode when DCS packets are received via DSI link.

Use Case 4: DBI-B/C Mode: The DBI interface is used to transfer video data; the DBI-C interface is used to transfer command data.

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- DSI Receiver
  - MIPI DSI-RX Data 2-lane, CLK 1-lane with data rates up to 800 Mbps/lane
  - Video input frame rates: Up to 60 fps for XGA, 30 fps for 720P
  - Video input data formats: RGB888, RGB666 and RGB565.
- DPI Host
  - Bus speed up to 70 MHz with data rate up to 210 Mbytes/s
  - Supports up to 60 fps for XGA, 30 fps for 720P
  - Supports the following pixel formats:
    - RGB666 18 bits per pixel
    - RGB666 loosely packed 18 bits per pixel
    - RGB565 16 bits per pixel
    - RGB565 loosely packed 16 bits per pixel
    - RGB888 24 bits per pixel
- DBI Host
  - Read/Write Data/Command from the external DBI slave device
  - Supports DCS commands, which is compliant with MIPI DBI-B standard
  - Supports the Intel® 80xx CPU I/F with either 8-bit or 16-bit commands
  - Supports up to 864 x 480 at 60 fps or 1280 x 720 at 30 fps
  - Programmable Output Data Format and Bus Width:
    8-bit, 9-bit, 16-bit, 18-bit, 24-bit bus
- Peripheral Control Ports
  - 4-pin SPI master; support for two SPI slaves at data rates of up to 10 Mbps
  - 3-pin DBI-C host interface; shared with SPI I/F and only one can be active at a time
  - I^2C compliant interface Slave port with data rates of up to 400 KHz. External I^2C master can access TC358762 internal registers via this port.
- Clock Source
  - Recommended external clock is 16.667 or 19.2 MHz
  - A programmable PLL can be used to adjust the output video clock both in DPI and DBI output modes
- Power Supply
  - Core : 1.2V ±0.1V
  - DSI I/O : 1.2 ±0.1V
  - I/O : 1.8 ±0.1V to 3.3 ±0.3V
- Package
  - P-VFBGA 64-pin 5 mm x 5 mm, 1.0 mm height, 0.5 mm ball pitch

Toshiba Mobile Initiative

This chipset is a member of the Toshiba mobile initiative product family. The Toshiba Mobile Strategic Initiative is a comprehensive program designed to offer its U.S.-based mobile handset/mobile consumer device customers a product portfolio that aims to provide faster time-to-market and helps them stay competitive.

As part of this initiative, Toshiba provides local application and design-in support and access to a host of analog peripheral ICs, including the Toshiba CMOS image sensor family, display controllers/drivers, I/O expander, bridge ICs, memory products and LCD modules.

The expanded portfolio also includes support tools, reference designs and evaluation boards.

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