

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1,048,576-WORD BY 16-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V16100FTI is a 16,777,216-bit high-speed static random access memory (SRAM) organized as 1,048,576 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable (\overline{CE}) can be used to place the device in a low-power mode, and output enable (\overline{OE}) provides fast memory access. Data byte control signals (\overline{LB} , \overline{UB}) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. It guarantees -40° to 85°C operating temperature so it is suitable for use in wide operating temperature system. The TC55V16100FTI is available in plastic 54-pin TSOP with 400mil width for high density surface assembly.

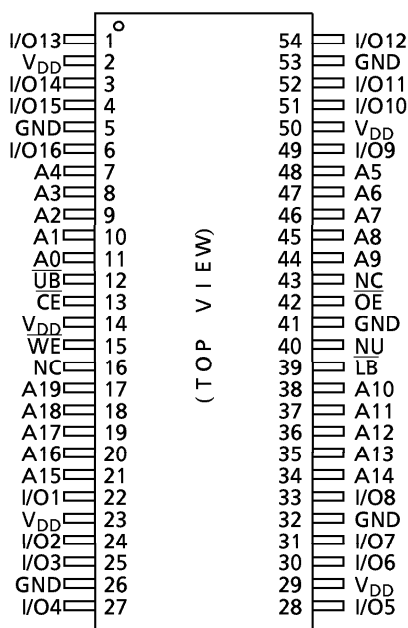
FEATURES

- Fast access time(the following are maximum values)
 - TC55V16100FTI-12: 12 ns
 - TC55V16100FTI-15: 15 ns
- Low-power dissipation
- Single power supply voltage : $3.3\text{V} \pm 0.3\text{V}$
- Fully static operation
- Operating temperature range : -40° to 85°C
- All inputs and outputs are LVTTL compatible
- Output buffer control using \overline{OE}
- Data byte control using \overline{LB} (I/O1 to I/O8) and \overline{UB} (I/O9 to I/O16)
- Package:
 - TSOP II 54-P-400-0.80B (Weight: 0.55g typ)

| | | | |
|-----------------|-----|-----|----|
| Cycle Time | 12 | 15 | ns |
| Operation (max) | 420 | 380 | mA |

Standby : 4mA(max)

PIN ASSIGNMENT



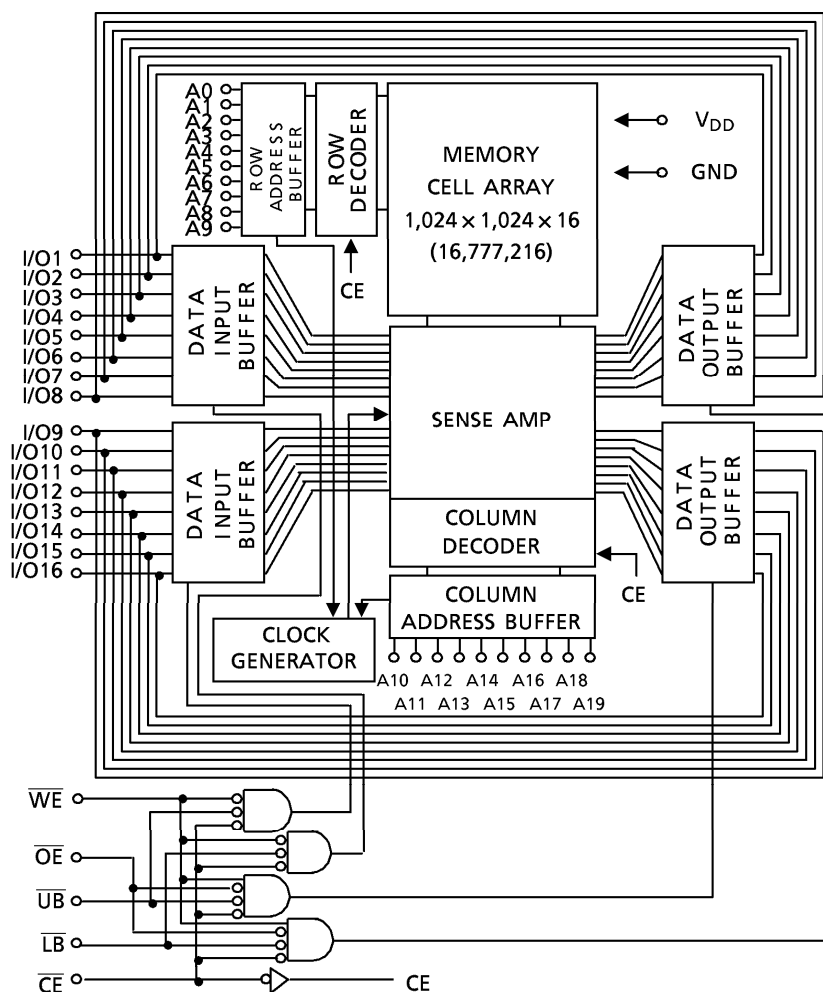
PIN NAMES

| | |
|-----------------------------------|--------------------------|
| A0 to A19 | Address Inputs |
| I/O1 to I/O16 | Data Inputs / Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{LB} , \overline{UB} | Data Byte Control Inputs |
| V_{DD} | Power (+ 3.3V) |
| GND | Ground |
| NC | No Connection |
| NU | Not Usable |

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BLOCK DIAGRAM



MAXIMUM RATINGS

| SYMBOL | RATING | VALUE | UNIT |
|---------------------|-------------------------------|-----------------------------------|------|
| V _{DD} | Power Supply Voltage | - 0.5 to 4.6 | V |
| V _{IN} | Input Terminal Voltage | - 0.5* to 4.6 | V |
| V _{I/O} | Input/Output Terminal Voltage | - 0.5* to V _{DD} + 0.5** | V |
| P _D | Power Dissipation | 1.8 | W |
| T _{solder} | Soldering Temperature (10 s) | 260 | °C |
| T _{strg} | Storage Temperature | - 65 to 150 | °C |
| T _{opr} | Operating Temperature | - 40 to 100 | °C |

* : -1.5V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : V_{DD}+1.5V with a pulse width of 20% · t_{RC} min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (T_a = - 40° to 85°C)

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|-----------------|----------------------|--------|-----|-------------------------|------|
| V _{DD} | Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V _{IH} | Input High Voltage | 2.0 | - | V _{DD} + 0.3** | V |
| V _{IL} | Input Low Voltage | - 0.3* | - | 0.8 | V |

* : -1.0V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : V_{DD}+1.0V with a pulse width of 20% · t_{RC} min (4ns max)

DC CHARACTERISTICS (Ta = -40° to 85°C, V_{DD} = 3.3V ± 0.3V)

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT | |
|--------------------|--|--|---------------------------|-----|-----|------|----|
| I _{IL} | Input Leakage Current (Except NU pin) | V _{IN} = 0 to V _{DD} | -1 | - | 1 | μA | |
| I _{LO} | Output Leakage Current | $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 to V _{DD} | -1 | - | 1 | μA | |
| I _{I(NU)} | Input Current (NU pin) | V _{IN} = 0 to 0.8V | -1 | - | 20 | μA | |
| | | V _{IN} = 0 to 0.2V | -1 | - | 1 | | |
| V _{OH} | Output High Voltage | I _{OH} = -2mA | 2.4 | - | - | V | |
| | | I _{OH} = -100μA | V _{DD} - 0.2 | - | - | | |
| V _{OL} | Output Low Voltage | I _{OL} = 2mA | - | - | 0.4 | | |
| | | I _{OL} = 100μA | - | - | 0.2 | | |
| I _{DDO} | Operating Current | $\overline{CE} = V_{IL}$, I _{out} = 0mA $\overline{OE} = V_{IH}$ Other Inputs = V _{DD} - 0.2V or 0.2V | t _{cycle} = 12ns | - | - | 420 | mA |
| | | | t _{cycle} = 15ns | - | - | 380 | |
| I _{DDS1} | Standby Current | $\overline{CE} = V_{IH}$, Other Inputs = V _{IH} or V _{IL} | - | - | 105 | mA | |
| I _{DDS2} | | $\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V | - | - | 4 | | |

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MAX | UNIT |
|------------------|--------------------------|------------------------|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = GND | 6 | pF |
| C _{I/O} | Input/Output Capacitance | V _{I/O} = GND | 8 | pF |

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

| MODE | \overline{CE} | \overline{OE} | \overline{WE} | \overline{LB} | \overline{UB} | I/O1 to I/O8 | I/O9 to I/O16 | POWER |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|------------------|
| Read | L | L | H | L | L | Output | Output | I _{DDO} |
| | | | | H | L | High Impedance | Output | I _{DDO} |
| | | | | L | H | Output | High Impedance | I _{DDO} |
| Write | L | x | L | L | L | Input | Input | I _{DDO} |
| | | | | H | L | High Impedance | Input | I _{DDO} |
| | | | | L | H | Input | High Impedance | I _{DDO} |
| Outputs Disable | L | H | H | x | x | High Impedance | High Impedance | I _{DDO} |
| | L | x | x | H | H | | | |
| Standby | H | x | x | x | x | High Impedance | High Impedance | I _{DDS} |

x: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V. You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS (Ta = - 40° to 85°C (Note 1), V_{DD} = 3.3V ± 0.3V)

READ CYCLE

| SYMBOL | PARAMETER | TC55V16100FTI-12 | | TC55V16100FTI-15 | | UNIT |
|------------------|---|------------------|-----|------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t _{RC} | Read Cycle Time | 12 | – | 15 | – | ns |
| t _{ACC} | Address Access Time | – | 12 | – | 15 | |
| t _{CO} | Chip Enable Access Time | – | 12 | – | 15 | |
| t _{OE} | Output Enable Access Time | – | 6 | – | 8 | |
| t _{BA} | Upper Byte, Lower Byte Access Time | – | 6 | – | 8 | |
| t _{OH} | Output Data Hold Time from Address Change | 3 | – | 3 | – | |
| t _{COE} | Output Enable Time from Chip Enable | 3 | – | 3 | – | |
| t _{OEE} | Output Enable Time from Output Enable | 1 | – | 1 | – | |
| t _{BE} | Output Enable Time from Upper Byte, Lower Byte | 1 | – | 1 | – | |
| t _{COD} | Output Disable Time from Chip Enable | – | 7 | – | 8 | |
| t _{ODO} | Output Disable Time from Output Enable | – | 7 | – | 8 | |
| t _{BD} | Output Disable Time from Upper Byte, Lower Byte | – | 7 | – | 8 | |

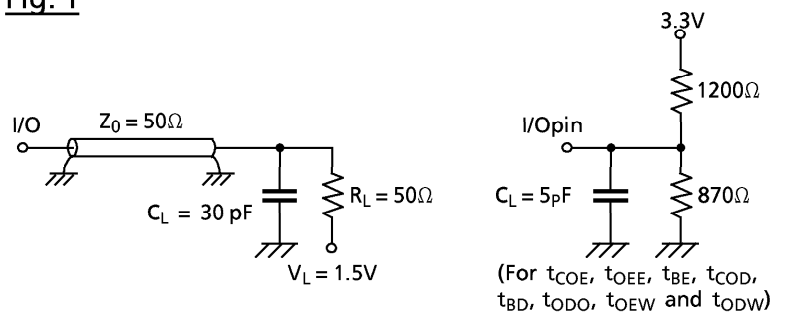
WRITE CYCLE

| SYMBOL | PARAMETER | TC55V16100FTI-12 | | TC55V16100FTI-15 | | UNIT |
|-----------------------------|---|------------------|-----|------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t _{WC} | Write Cycle Time | 12 | – | 15 | – | ns |
| t _{WP} | Write Pulse Width | 8 | – | 10 | – | |
| t _{CW} | Chip Enable to End of Write | 9 | – | 11 | – | |
| t _{BW} | Upper Byte, Lower Byte Enable to End of Write | 9 | – | 11 | – | |
| t _{AW} | Address Valid to End of Write | 9 | – | 11 | – | |
| t _{AS} | Address Setup Time | 0 | – | 0 | – | |
| t _{WR} | Write Recovery Time | 0 | – | 0 | – | |
| t _{DS} | Data Setup Time | 7 | – | 8 | – | |
| t _{DH} | Data Hold Time | 0 | – | 0 | – | |
| t _{OE_W} | Output Enable Time from Write Enable | 1 | – | 1 | – | |
| t _{OD_W} | Output Disable Time from Write Enable | – | 7 | – | 8 | |

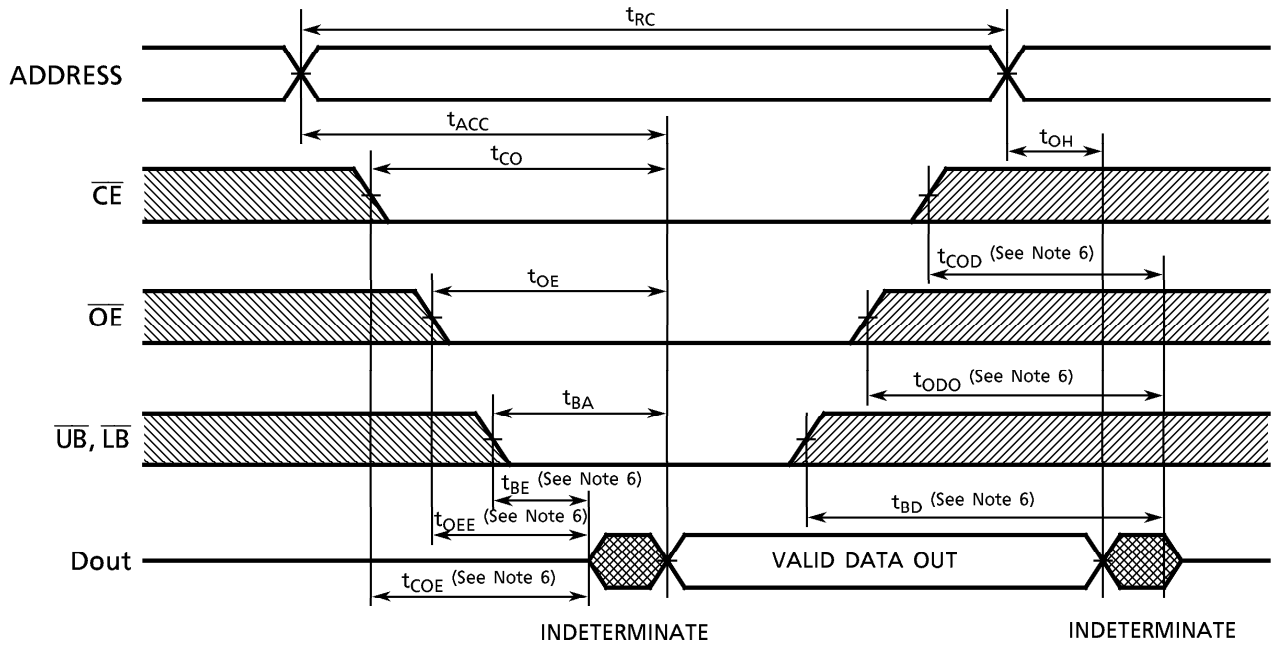
AC TEST CONDITIONS

| | |
|---|-----------|
| Input Pulse Level | 3.0V/0.0V |
| Input Pulse Rise and Fall Time | 2ns |
| Input Timing Measurement Reference Level | 1.5V |
| Output Timing Measurement Reference Level | 1.5V |
| Output Load | Fig. 1 |

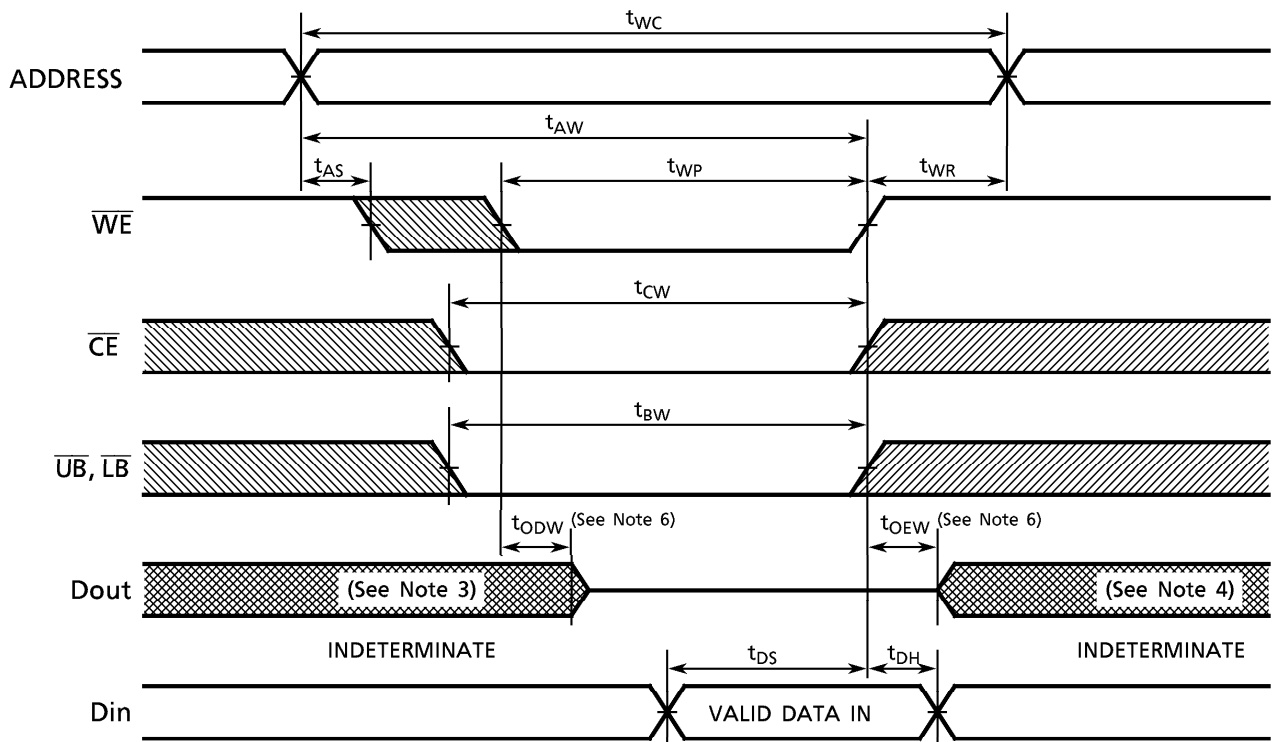
Fig. 1



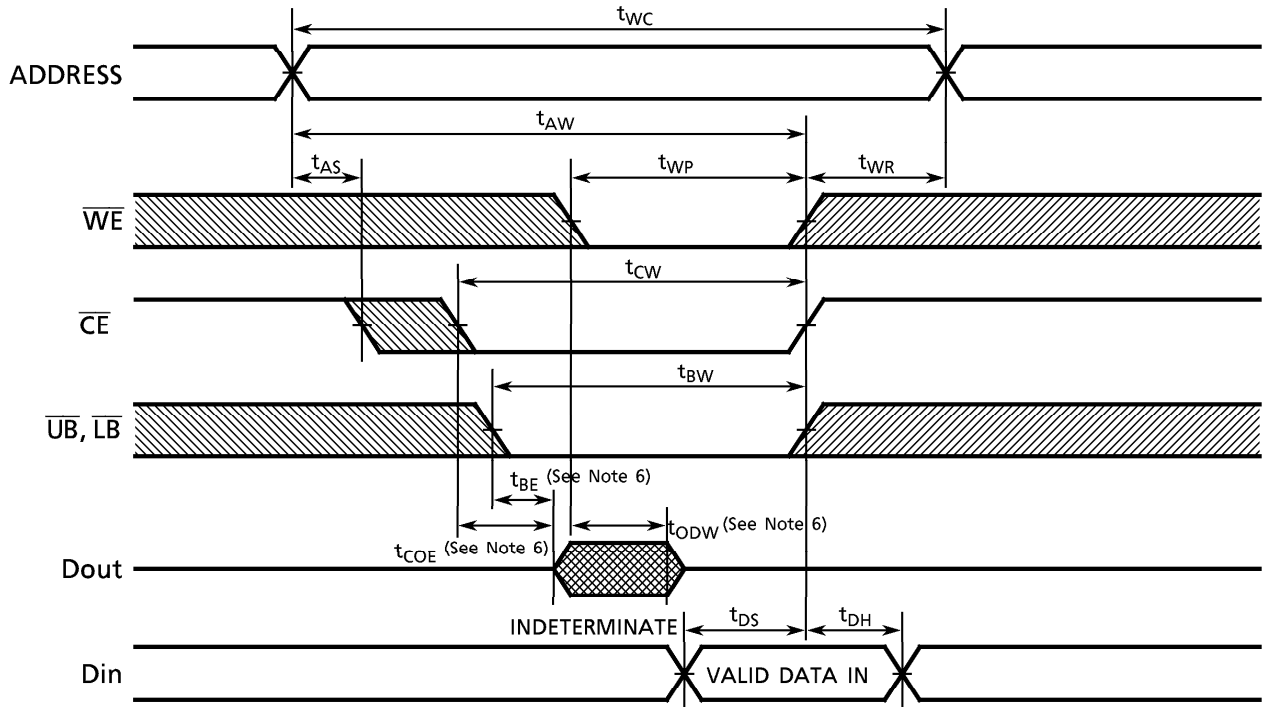
TIMING DIAGRAMS
READ CYCLE (See Note 2)



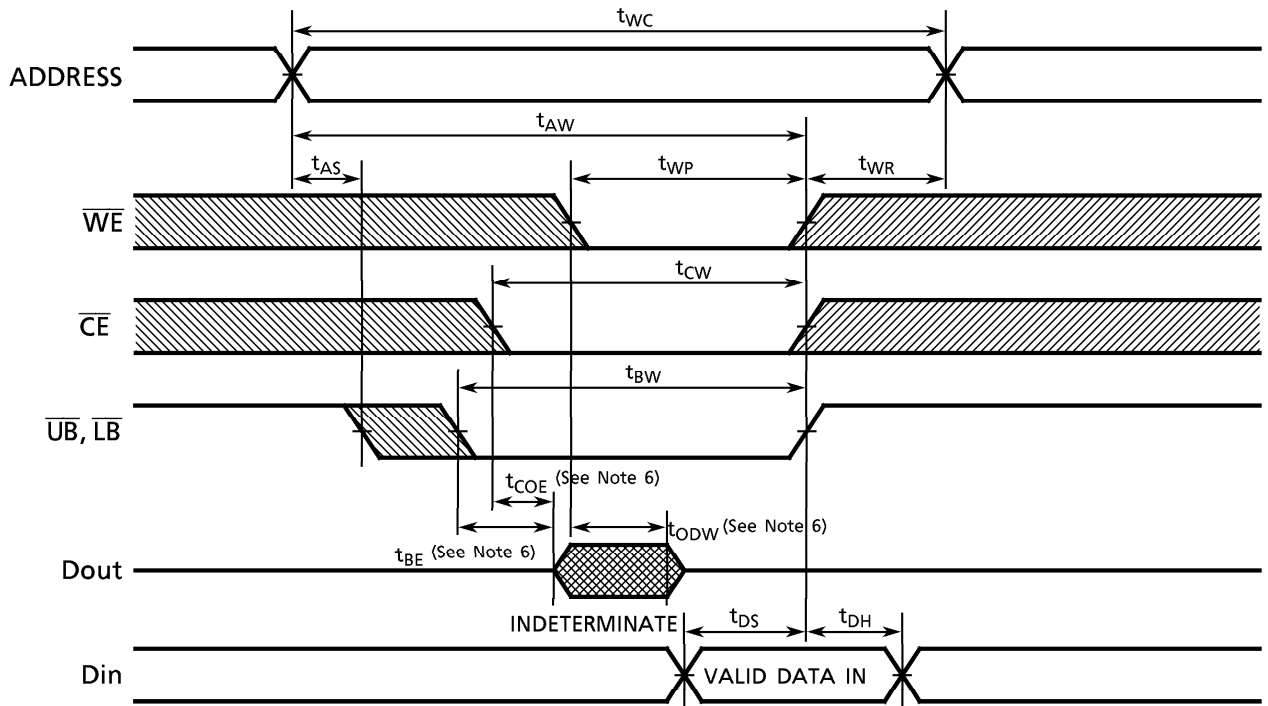
WRITE CYCLE 1 (\overline{WE} CONTROLLED) (See Note 5)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 5)



WRITE CYCLE 3 ($\overline{UB}, \overline{LB}$ CONTROLLED) (See Note 5)



Note: (1) Operating temperature (T_a) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) \overline{WE} remains HIGH for the Read Cycle.

(3) If \overline{CE} goes LOW coincident with or after \overline{WE} goes LOW, the outputs will remain at high impedance.

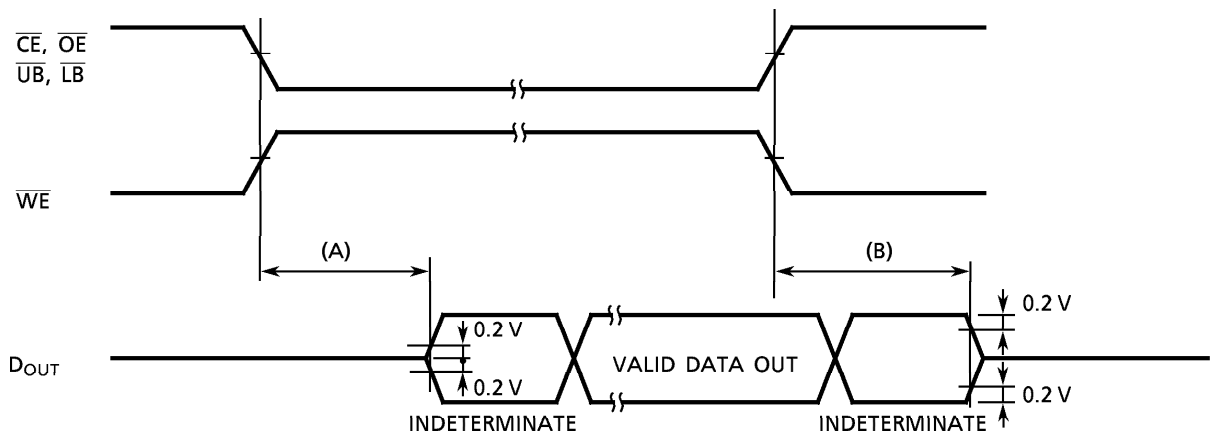
(4) If \overline{CE} goes HIGH coincident with or before \overline{WE} goes HIGH, the outputs will remain at high impedance.

(5) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A) $t_{COE}, t_{OEE}, t_{BE}, t_{OEw}$ Output Enable Time

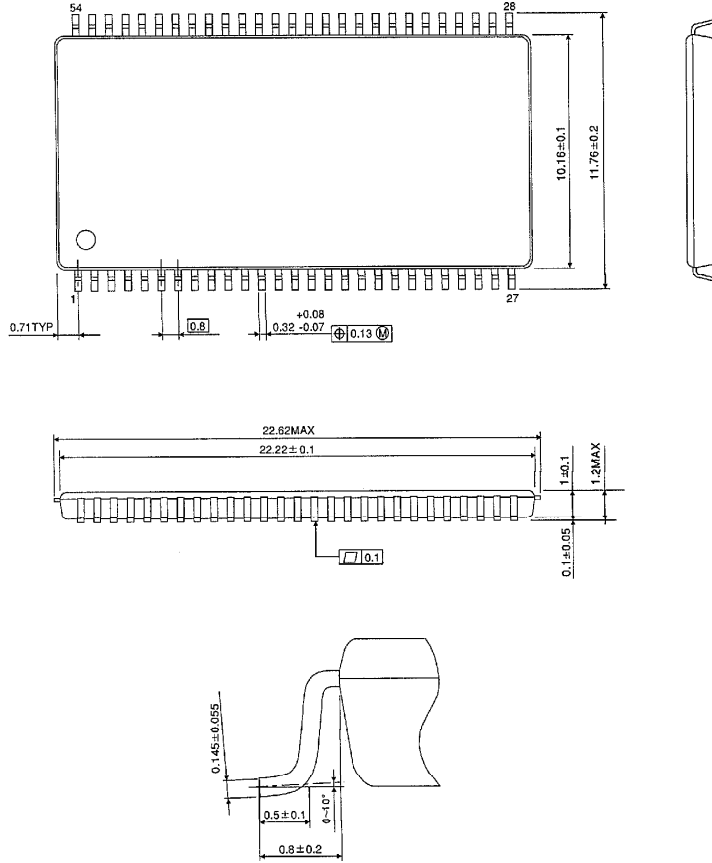
(B) $t_{COD}, t_{ODO}, t_{BD}, t_{ODW}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 54-P-400-0.80B)

Unit in mm



Weight : 0.55g (Typ)