

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT FULL CMOS STATIC RAM

## DESCRIPTION

The TC55W400XB is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.3 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 0.5  $\mu$ A standby current (at  $V_{DD} = 3$  V,  $T_a = 25^\circ\text{C}$ , maximum) when chip enable ( $\overline{CE1}$ ) is asserted high or ( $\overline{CE2}$ ) is asserted low. There are three control inputs.  $\overline{CE1}$  and  $\overline{CE2}$  are used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. Data byte control pin ( $\overline{LB}$ ,  $\overline{UB}$ ) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of  $-40^\circ$  to  $85^\circ\text{C}$ , the TC55W400XB can be used in environments exhibiting extreme temperature conditions. The TC55W400XB is available in a plastic 48-ball BGA.

## FEATURES

- Low-power dissipation  
Operating: 9.9 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.3 V
- Power down features using  $\overline{CE1}$  and  $\overline{CE2}$
- Data retention supply voltage of 1.5 to 3.3 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of  $-40^\circ$  to  $85^\circ\text{C}$
- Standby Current (maximum):

3.3 V	10 $\mu$ A
3.0 V	5 $\mu$ A

- Access Times (maximum at  $V_{DD} = 2.7$  to  $3.3$  V):

	TC55W400XB	
	5	7
Access Time	55 ns	70 ns
$\overline{CE1}$ Access Time	55 ns	70 ns
$\overline{CE2}$ Access Time	55 ns	70 ns
$\overline{OE}$ Access Time	30 ns	35 ns

- Package:  
P-TFBGA48-0608-0.75BZ (Weight: 0.09 g typ)

## PIN ASSIGNMENT (TOP VIEW)

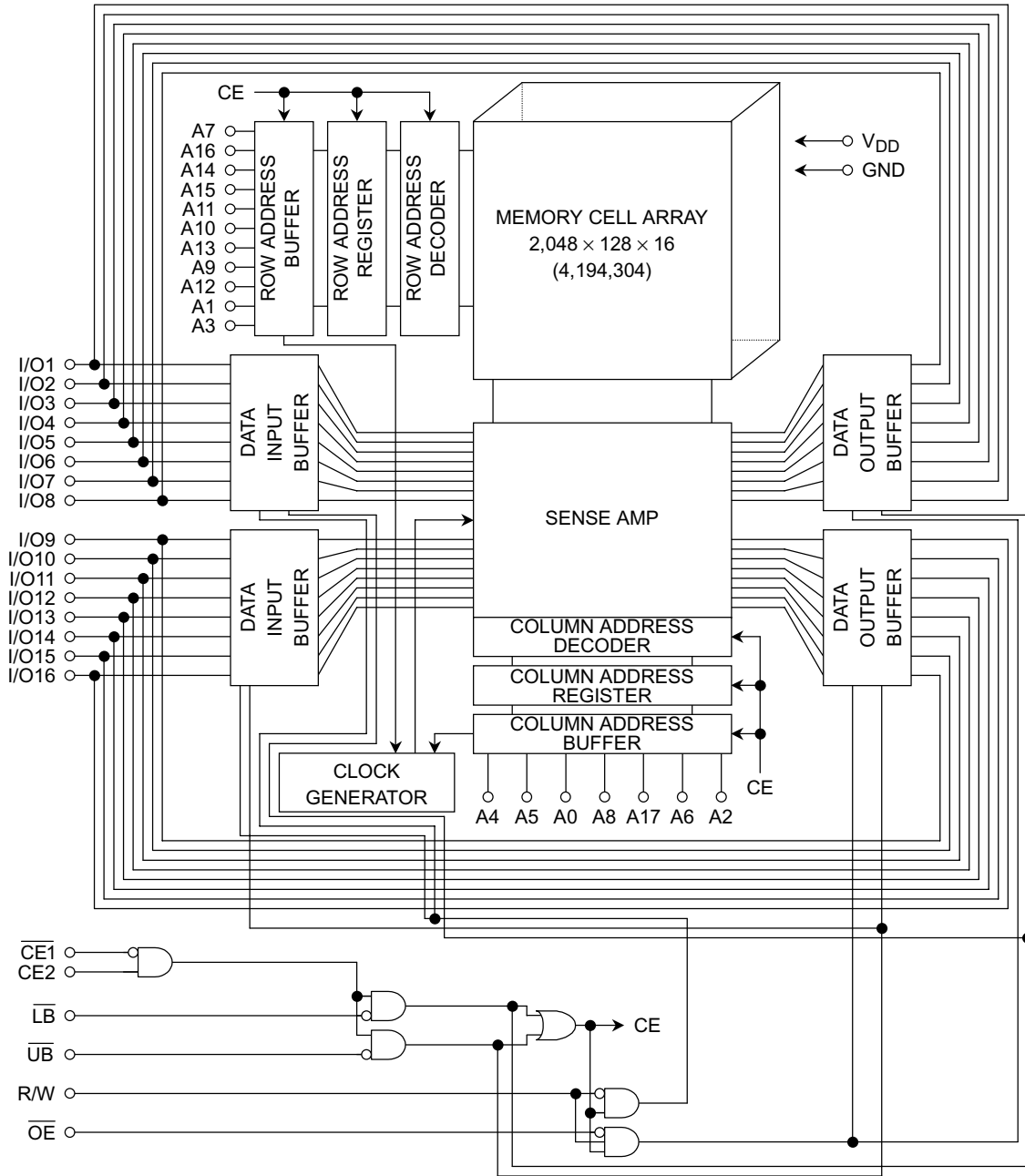
### 48 PIN BGA

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	$V_{SS}$	I/O12	A17	A7	I/O4	$V_{DD}$
E	$V_{DD}$	I/O13	NC	A16	I/O5	$V_{SS}$
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	R/W	I/O8
H	NC	A8	A9	A10	A11	NC

## PIN NAMES

A0~A17	Address Inputs
$\overline{CE1}$ , $\overline{CE2}$	Chip Enable Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$ , $\overline{UB}$	Data Byte Control Inputs
I/O1~I/O16	Data Inputs/Outputs
$V_{DD}$	Power
GND	Ground
NC	No Connection

**BLOCK DIAGRAM**



**OPERATING MODE**

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	H	L	H	L	L	Output	Output	$I_{DD0}$
	L	H	L	H	H	L	High-Z	Output	$I_{DD0}$
	L	H	L	H	L	H	Output	High-Z	$I_{DD0}$
Write	L	H	*	L	L	L	Input	Input	$I_{DD0}$
	L	H	*	L	H	L	High-Z	Input	$I_{DD0}$
	L	H	*	L	L	H	Input	High-Z	$I_{DD0}$
Output Deselect	L	H	H	H	*	*	High-Z	High-Z	$I_{DD0}$
Standby	H	*	*	*	*	*	High-Z	High-Z	$I_{DDs}$
	*	L	*	*	*	*	High-Z	High-Z	$I_{DDs}$
	*	*	*	*	H	H	High-Z	High-Z	$I_{DDs}$

\* = don't care  
 H = logic high  
 L = logic low

## MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~4.2	V
V <sub>IN</sub>	Input Voltage	-0.3*~4.2	V
V <sub>I/O</sub>	Input/Output Voltage	-0.5~V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.6	W
T <sub>solder</sub>	Soldering Temperature (10s)	260	°C
T <sub>stg</sub>	Storage Temperature	-55~125	°C
T <sub>opr</sub>	Operating Temperature	-40~85	°C

\*: -2.0 V when measured at a pulse width of 20 ns

## DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	
V <sub>DD</sub>	Power Supply Voltage	2.3	—	3.3	V	
V <sub>IH</sub>	Input High Voltage	V <sub>DD</sub> = 2.3 V~3.3 V	2.0	—	V <sub>DD</sub> + 0.3	V
		V <sub>DD</sub> = 2.7 V~3.3 V	2.2			
V <sub>IL</sub>	Input Low Voltage	-0.3*	—	V <sub>DD</sub> × 0.22	V	
V <sub>DH</sub>	Data Retention Supply Voltage	1.5	—	3.3	V	

\*: -2.0 V when measured at a pulse width of 20 ns

## DC CHARACTERISTICS (Ta = -40° to 85°C, VDD = 2.3 to 3.3 V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT		
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V~V <sub>DD</sub>	—	—	±1.0	μA		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5 V	-0.5	—	—	mA		
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	2.1	—	—	mA		
I <sub>LO</sub>	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{LB}$ and $\overline{UB} = V_{IH}$ or $R/W = V_{IL}$ or $OE = V_{IH}$ , V <sub>OUT</sub> = 0 V~V <sub>DD</sub>	—	—	±1.0	μA		
I <sub>DDO1</sub>	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $\overline{LB}$ and $\overline{UB} = V_{IL}$ and $R/W = V_{IH}$ and I <sub>OUT</sub> = 0 mA and Other Input = V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub>	min	—	—	45	mA
				1 μs	—	—	10	
I <sub>DDO2</sub>	Operating Current	$\overline{CE1} = 0.2$ V and $CE2 = V_{DD} - 0.2$ V and $\overline{LB}$ and $\overline{UB} = 0.2$ V, R/W = V <sub>DD</sub> - 0.2 V and I <sub>OUT</sub> = 0 mA, Other Input = V <sub>DD</sub> - 0.2 V/0.2 V	t <sub>cycle</sub>	min	—	—	45	mA
				1 μs	—	—	5	
I <sub>DDS1</sub>	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{LB}$ and $\overline{UB} = V_{IH}$		—	—	2	μA	
I <sub>DDS2</sub> (Note)		$\overline{CE1} = V_{DD} - 0.2$ V or $CE2 = 0.2$ V or $\overline{LB}$ and $\overline{UB} =$ V <sub>DD</sub> - 0.2 V, V <sub>DD</sub> = 1.5 V~3.3 V	V <sub>DD</sub> = 3.0 V ± 10%	Ta = 25°C	—	—		1
				Ta = -40~85°C	—	—		10
			V <sub>DD</sub> = 3.0 V	Ta = 25°C	—	0.05		0.5
	Ta = -40~40°C			—	—	1		
Ta = -40~85°C	—	—	5					

Note • In standby mode with  $\overline{CE1} \geq V_{DD} - 0.2$  V, these limits are assured for the condition  $CE2 \geq V_{DD} - 0.2$  V or  $CE2 \leq 0.2$  V.

• In standby mode with  $\overline{LB}$  and  $\overline{UB} \geq V_{DD} - 0.2$  V, these limits are assured for the condition  $\overline{CE1} \geq V_{DD} - 0.2$  V or  $\overline{CE1} \leq 0.2$  V and  $CE2 \geq V_{DD} - 0.2$  V or  $CE2 \leq 0.2$  V.

## CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

## AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = -40° to 85°C, V<sub>DD</sub> = 2.7 to 3.3 V)

### READ CYCLE

SYMBOL	PARAMETER	TC55W400XB				UNIT
		5		7		
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	ns
t <sub>ACC</sub>	Address Access Time	—	55	—	70	
t <sub>CO1</sub>	Chip Enable( $\overline{CE1}$ ) Access Time	—	55	—	70	
t <sub>CO2</sub>	Chip Enable(CE2) Access Time	—	55	—	70	
t <sub>OE</sub>	Output Enable Access Time	—	30	—	35	
t <sub>BA</sub>	Data Byte Control Access Time	—	55	—	70	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	—	5	—	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	—	0	—	
t <sub>BE</sub>	Data Byte Control Low to Output Active	0	—	0	—	
t <sub>OD</sub>	Chip Enable High to Output High-Z	—	25	—	30	
t <sub>ODO</sub>	Output Enable High to Output High-Z	—	25	—	30	
t <sub>BD</sub>	Data Byte Control High to Output High-Z	—	25	—	30	
t <sub>OH</sub>	Output Data Hold Time	10	—	10	—	

### WRITE CYCLE

SYMBOL	PARAMETER	TC55W400XB				UNIT
		5		7		
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	55	—	70	—	ns
t <sub>WP</sub>	Write Pulse Width	45	—	50	—	
t <sub>CW</sub>	Chip Enable to End of Write	50	—	60	—	
t <sub>BW</sub>	Data Byte Control to End of Write	50	—	60	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	R/W Low to Output High-Z	—	20	—	25	
t <sub>OEW</sub>	R/W High to Output Active	0	—	0	—	
t <sub>DS</sub>	Data Setup Time	25	—	30	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

### AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.4 V
Timing measurements	V <sub>DD</sub> × 0.5
Reference level	V <sub>DD</sub> × 0.5
t <sub>R</sub> , t <sub>F</sub>	5 ns

## AC CHARACTERISTICS AND OPERATING CONDITIONS

( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 2.3$  to  $3.3\text{ V}$ )

### READ CYCLE

SYMBOL	PARAMETER	TC55W400XB				UNIT
		5		7		
		MIN	MAX	MIN	MAX	
$t_{RC}$	Read Cycle Time	70	—	85	—	ns
$t_{ACC}$	Address Access Time	—	70	—	85	
$t_{CO1}$	Chip Enable( $\overline{CE1}$ ) Access Time	—	70	—	85	
$t_{CO2}$	Chip Enable(CE2) Access Time	—	70	—	85	
$t_{OE}$	Output Enable Access Time	—	35	—	45	
$t_{BA}$	Data Byte Control Access Time	—	70	—	85	
$t_{COE}$	Chip Enable Low to Output Active	5	—	5	—	
$t_{OEE}$	Output Enable Low to Output Active	0	—	0	—	
$t_{BE}$	Data Byte Control Low to Output Active	0	—	0	—	
$t_{OD}$	Chip Enable High to Output High-Z	—	30	—	35	
$t_{ODO}$	Output Enable High to Output High-Z	—	30	—	35	
$t_{BD}$	Data Byte Control High to Output High-Z	—	30	—	35	
$t_{OH}$	Output Data Hold Time	10	—	10	—	

### WRITE CYCLE

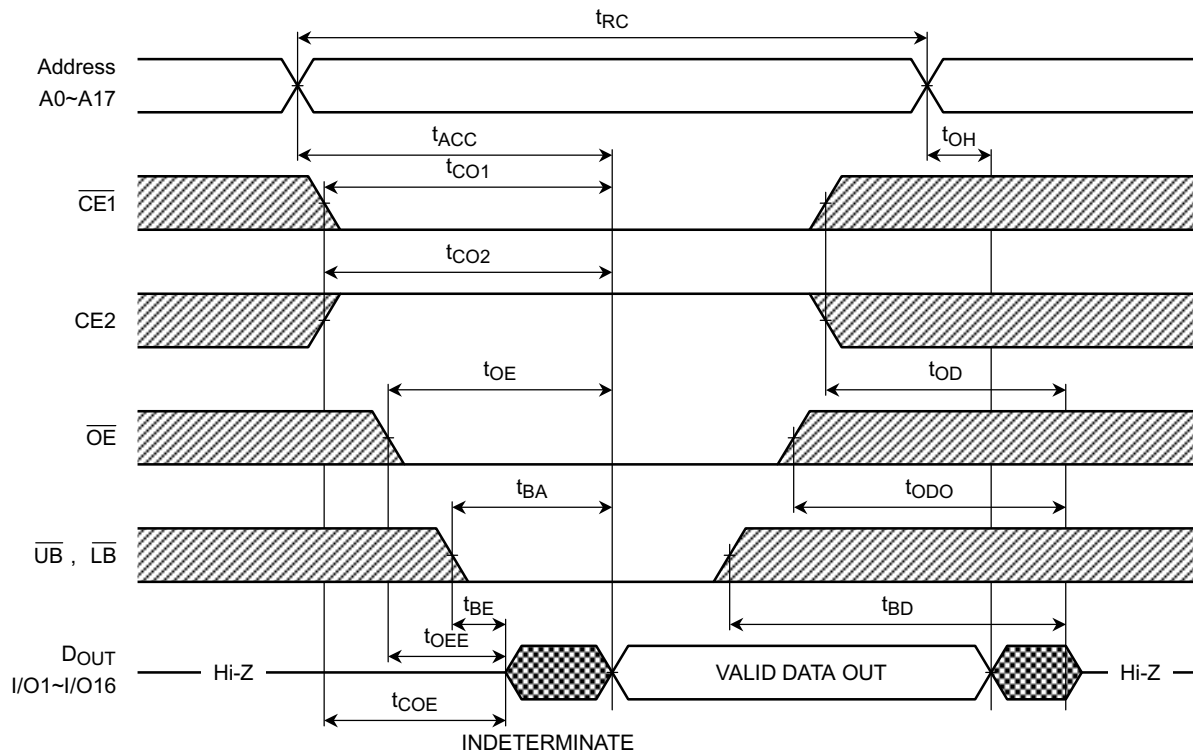
SYMBOL	PARAMETER	TC55W400XB				UNIT
		5		7		
		MIN	MAX	MIN	MAX	
$t_{WC}$	Write Cycle Time	70	—	85	—	ns
$t_{WP}$	Write Pulse Width	50	—	55	—	
$t_{CW}$	Chip Enable to End of Write	60	—	70	—	
$t_{BW}$	Data Byte Control to End of Write	60	—	70	—	
$t_{AS}$	Address Setup Time	0	—	0	—	
$t_{WR}$	Write Recovery Time	0	—	0	—	
$t_{ODW}$	R/W Low to Output High-Z	—	25	—	35	
$t_{OEW}$	R/W High to Output Active	0	—	0	—	
$t_{DS}$	Data Setup Time	30	—	35	—	
$t_{DH}$	Data Hold Time	0	—	0	—	

### AC TEST CONDITIONS

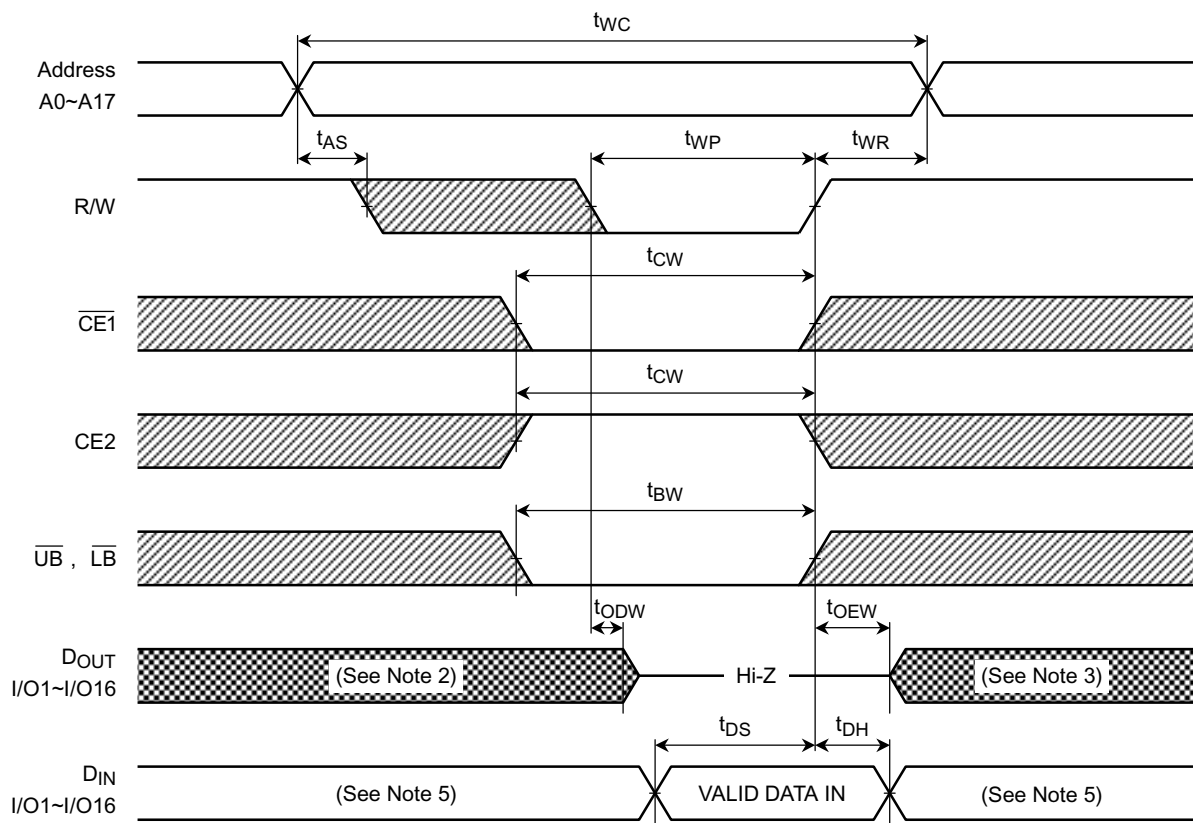
PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	$V_{DD} - 0.2\text{ V}$ , 0.2 V
Timing measurements	$V_{DD} \times 0.5$
Reference level	$V_{DD} \times 0.5$
$t_R$ , $t_F$	5 ns

## TIMING DIAGRAMS

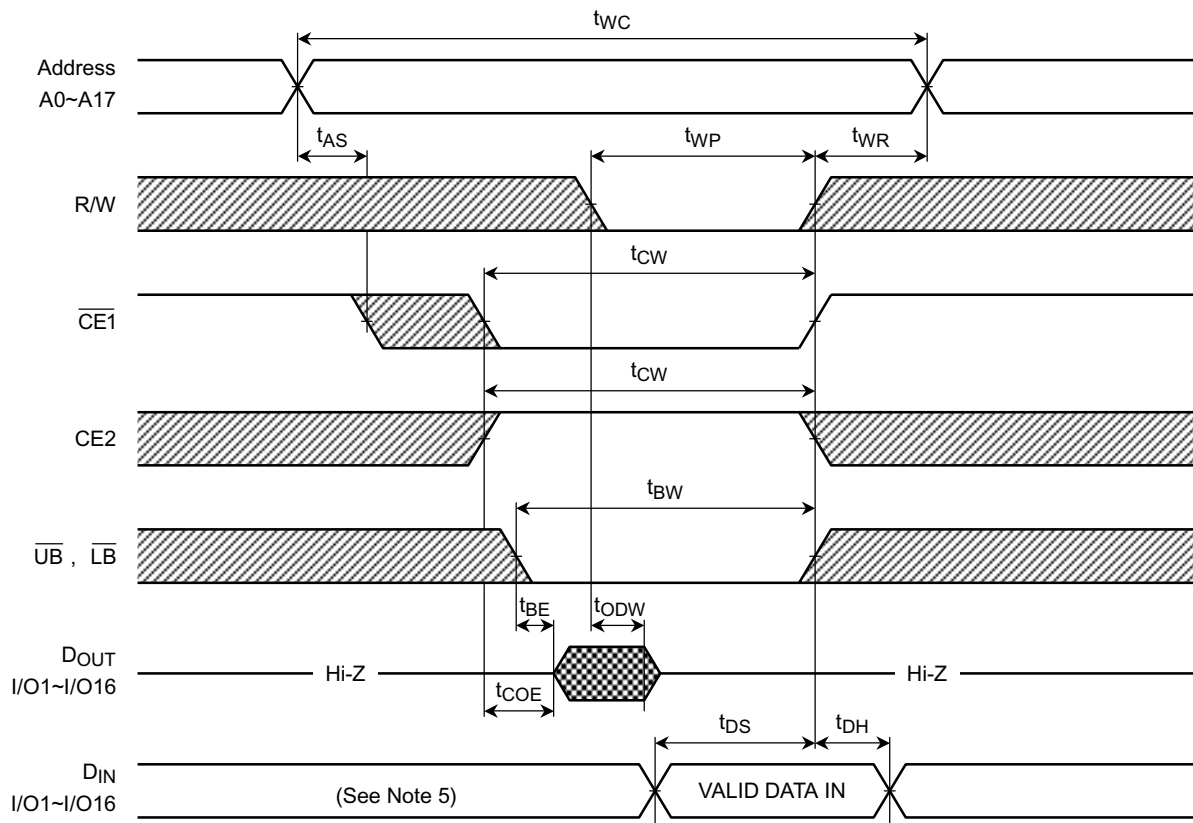
### READ CYCLE (See Note 1)



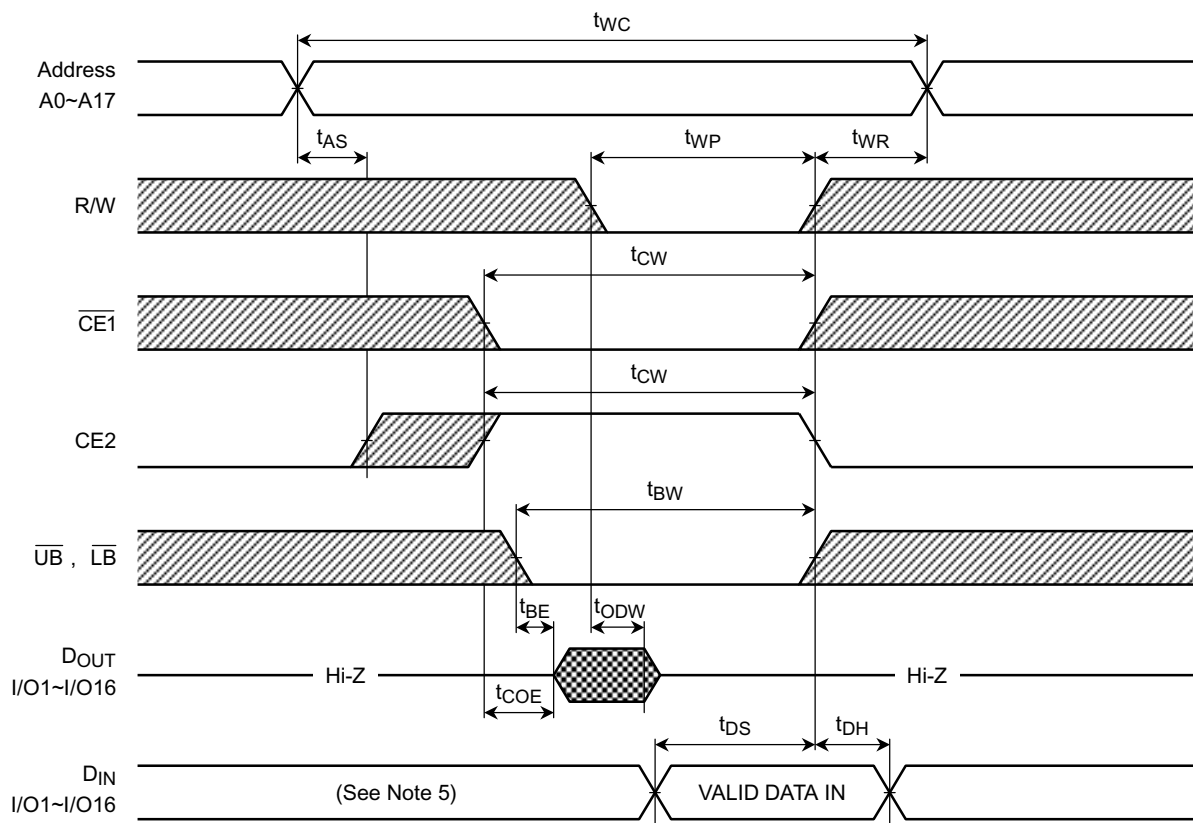
### WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ( $\overline{CE1}$  CONTROLLED) (See Note 4)

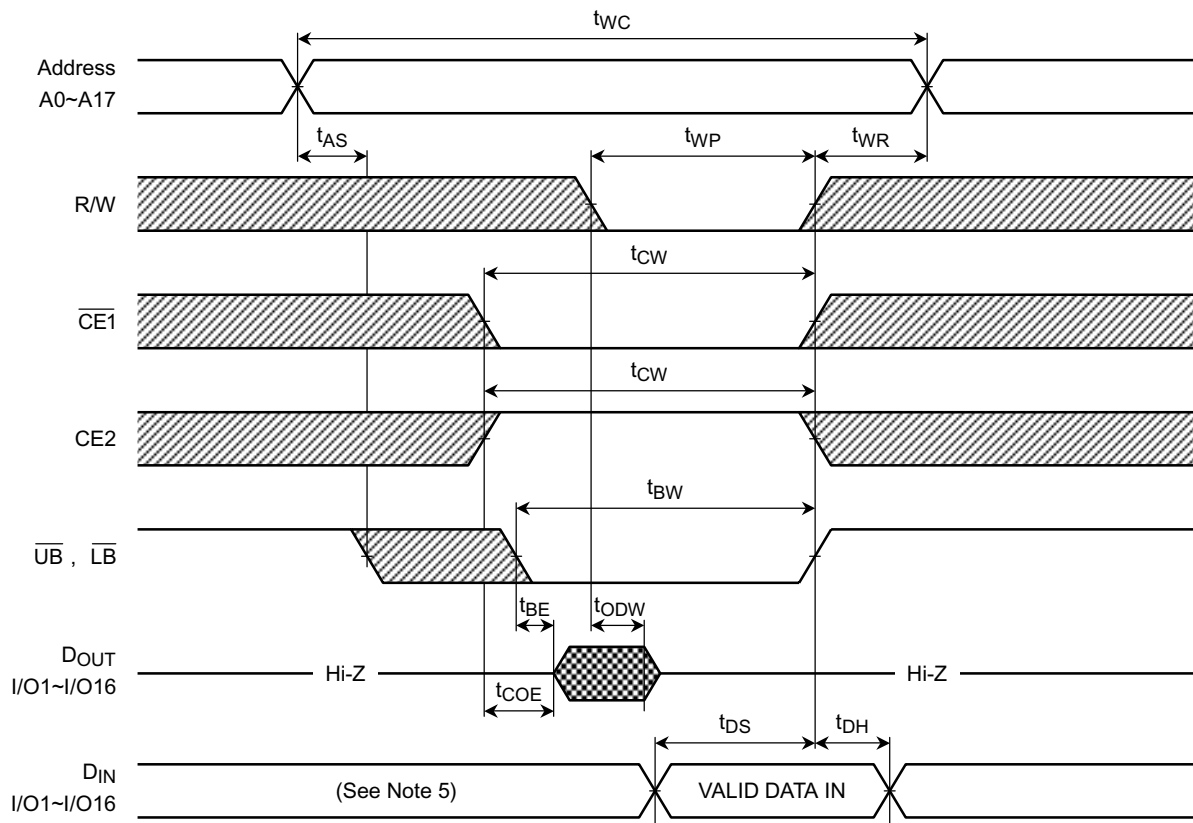


WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)





WRITE CYCLE 4 ( $\overline{UB}$ ,  $\overline{LB}$  CONTROLLED) (See Note 4)



Note:

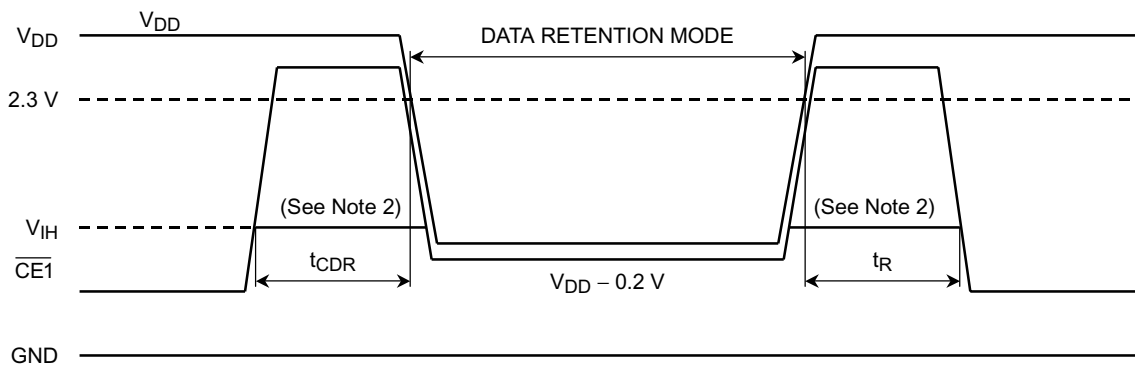
- (1) R/W remains HIGH for the read cycle.
- (2) If  $\overline{CE1}$  goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If  $\overline{CE1}$  goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

## DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

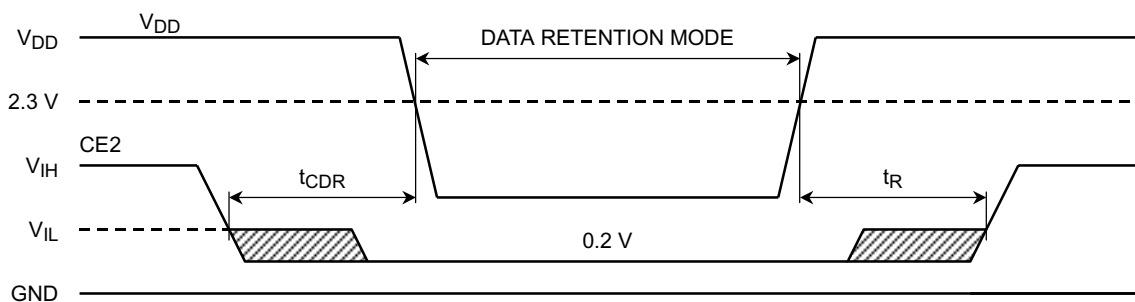
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage		1.5	—	3.3	V	
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.3 V	Ta = -40~85°C	—	—	10	μA
		V <sub>DH</sub> = 3.0 V	Ta = -40~40°C	—	—	1	
			Ta = -40~85°C	—	—	5	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time		0	—	—	ns	
t <sub>R</sub>	Recovery Time		t <sub>RC</sub> (See Note)	—	—	ns	

Note: Read cycle time

### CE1 CONTROLLED DATA RETENTION MODE (See Note 1)



### CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



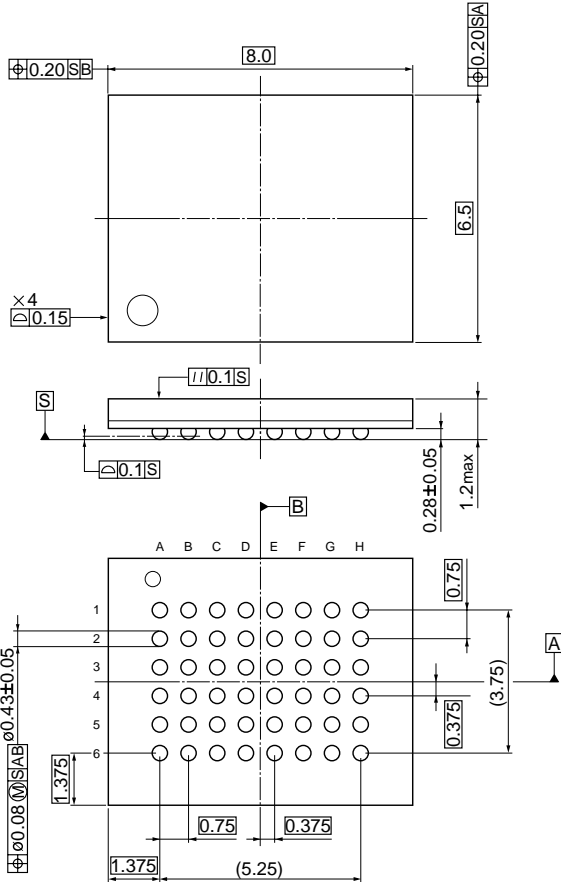
Note:

- (1) In  $\overline{CE1}$  controlled data retention mode, minimum standby current mode is entered when  $CE2 \leq 0.2$  V or  $CE2 \geq V_{DD} - 0.2$  V.
- (2) When  $\overline{CE1}$  is operating at the  $V_{IH}$  level, the operating current is given by  $I_{DDS1}$  during the transition of  $V_{DD}$  from 2.3 to 2.2V.
- (3) In CE2 controlled data retention mode, minimum standby current mode is entered when  $CE2 \leq 0.2$  V.

PACKAGE DIMENSIONS

P-TFBGA48-0608-0.75BZ

Unit:mm



Weight: 0.09 g (typ)

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000707EBA

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