

# TC74ACT164P, TC74ACT164F, TC74ACT164FN

## 8 - BIT SHIFT REGISTER (S - IN, P - OUT)

The TC74ACT164 is an advanced high speed CMOS 8 - BIT SERIAL - IN PARALLEL - OUT SHIFT REGISTER fabricated with silicon gate and double - layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. It consists of a serial - in, parallel - out 8 - bit shift register with a CLOCK input and an overriding CLEAR input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### FEATURES:

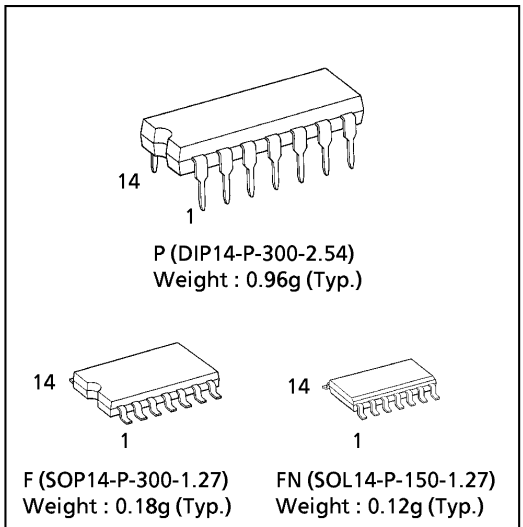
- High Speed..... $f_{MAX} = 200\text{MHz}$  (typ.) at  $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}$ (Max.) at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs.... $V_{IL} = 0.8\text{V}$ (Max.)  
 $V_{IH} = 2.0\text{V}$ (Min.)
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24\text{mA}$ (Min.)  
Capability of driving  $50\Omega$  transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F164

### TRUTH TABLE

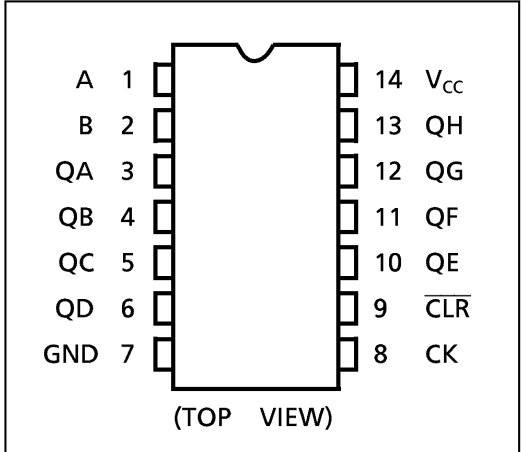
INPUTS				OUTPUTS			
CLR	CK	SERIAL IN		QA	QB	...	QH
		A	B				
L	X	X	X	L	L	...	L
H		X	X	NO CHANGE			
H		L	X	L	QA <sub>n</sub>	...	QG <sub>n</sub>
H		X	L	L	QA <sub>n</sub>	...	QG <sub>n</sub>
H		H	H	H	QA <sub>n</sub>	...	QG <sub>n</sub>

X : Don't Care  
 QA<sub>n</sub> ~ QG<sub>n</sub>: The level of QA ~ QG, respectively, before the most recent positive edge of the clock.

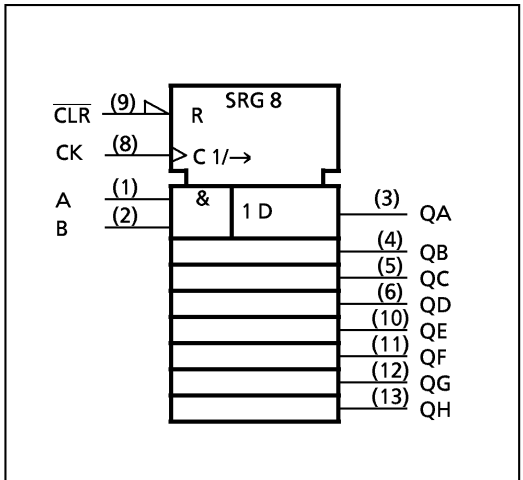
(Note) The JEDEC SOP (FN) is not available in Japan.



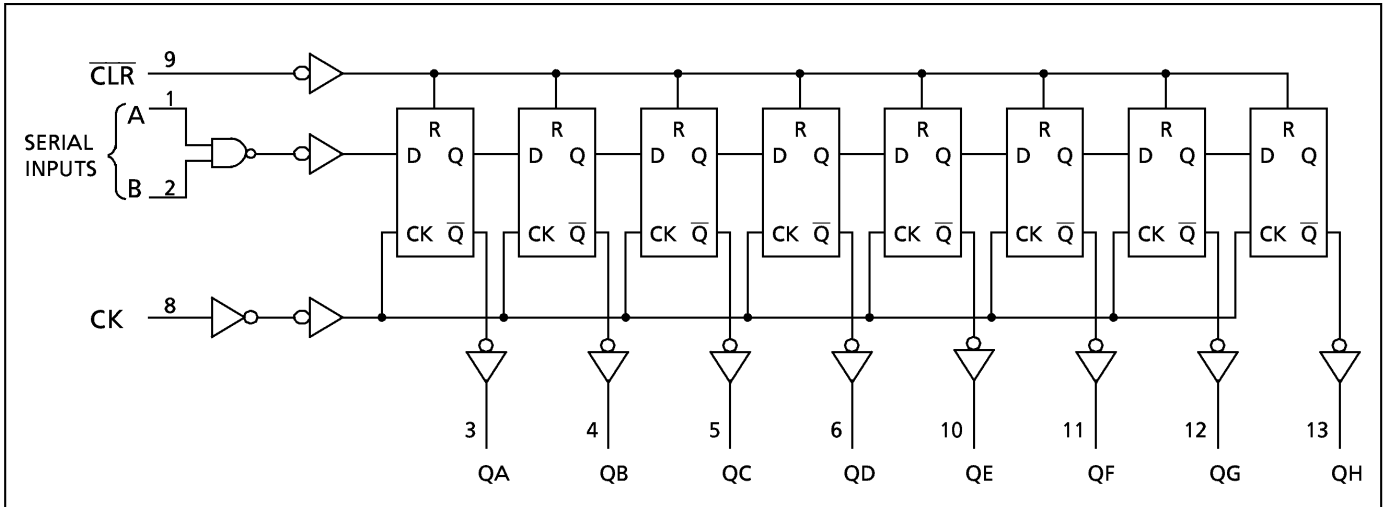
### PIN ASSIGNMENT



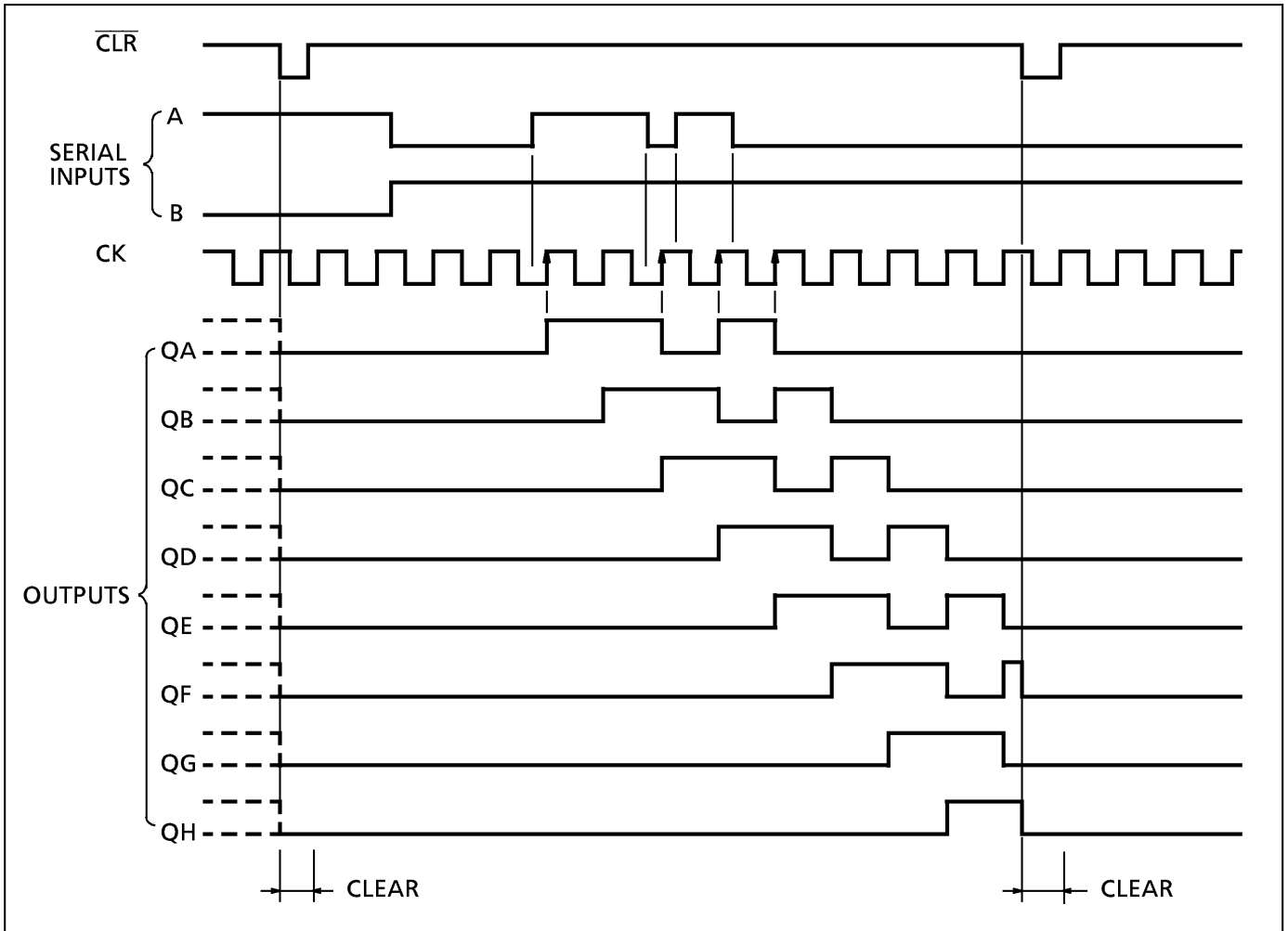
### IEC LOGIC SYMBOL



**SYSTEM DIAGRAM**



**TIMING CHART**



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	± 20	mA
Output Diode Current	$I_{OK}$	± 50	mA
DC Output Current	$I_{OUT}$	± 50	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	± 200	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  should be applied up to 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$dt/dV$	0~10	ns/V

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		4.5 } 5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	$V_{IL}$		4.5 } 5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -24\text{mA}$	4.5	3.94	—	—	3.80	—	
			$I_{OH} = -75\text{mA}^*$	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 24\text{mA}$	4.5	—	—	0.36	—	0.44	
			$I_{OL} = 75\text{mA}^*$	5.5	—	—	—	—	1.65	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	—	± 1.0	$\mu\text{A}$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0		
		$I_C$	PER INPUT : $V_{IN} = 3.4\text{V}$ OTHER INPUT : $V_{CC}$ or GND	5.5	—	—	1.35	—	1.5	mA

\* : This spec indicates the capability of driving  $50\Omega$  transmission lines.  
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t <sub>W(L)</sub> t <sub>W(H)</sub>		5.0 ± 0.5	5.0	5.0	5.0	ns
Minimum Pulse Width (CLR)	t <sub>W(L)</sub>		5.0 ± 0.5	5.0	5.0	5.0	
Minimum Set-up Time	t <sub>s</sub>		5.0 ± 0.5	3.0	3.0	3.0	
Minimum Hold Time	t <sub>h</sub>		5.0 ± 0.5	2.6	2.6	2.6	
Minimum Removal Time (CLR)	t <sub>rem</sub>		5.0 ± 0.5	2.0	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω, Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (CK-Q)	t <sub>pLH</sub> t <sub>pHL</sub>		5.0 ± 0.5	—	6.6	11.0	1.0	12.5	ns
Propagation Delay Time (CLR-Q)	t <sub>pHL</sub>		5.0 ± 0.5	—	6.9	11.0	1.0	12.5	
Maximum Clock Frequency	f <sub>MAX</sub>		5.0 ± 0.5	80	150	—	80	—	MHz
Input Capacitance	C <sub>IN</sub>			—	5	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub> (1)			—	101	—	—	—	

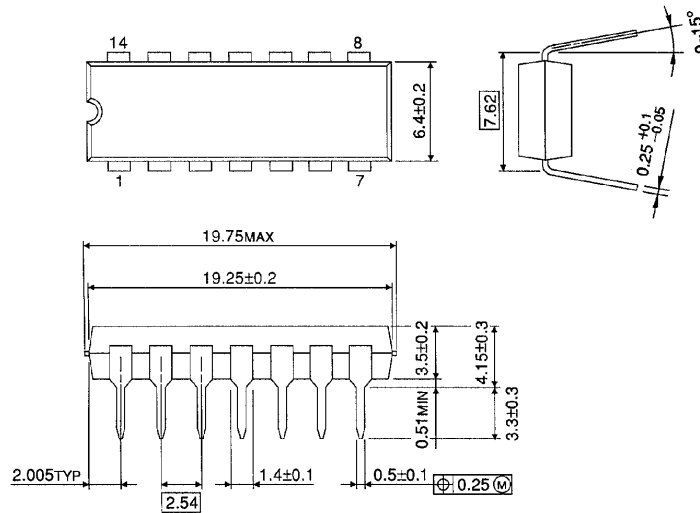
Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 14PIN PACKAGE DIMENSIONS (DIP14-P-300-2.54)

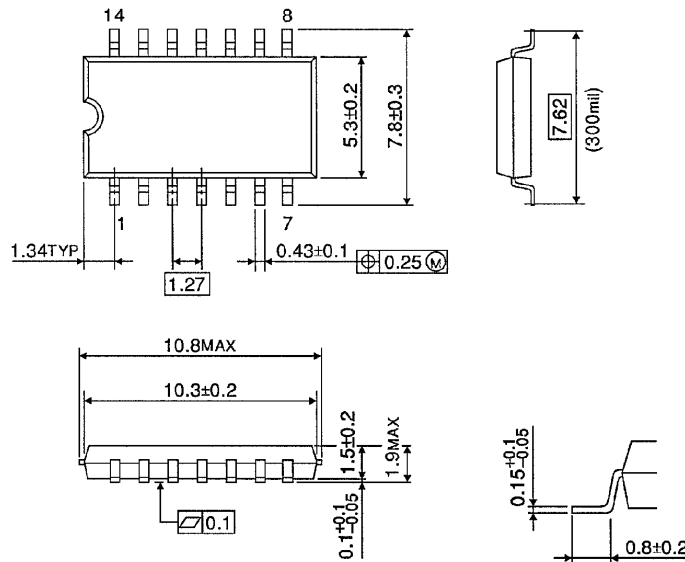
Unit in mm



Weight : 0.96g (Typ.)

SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm

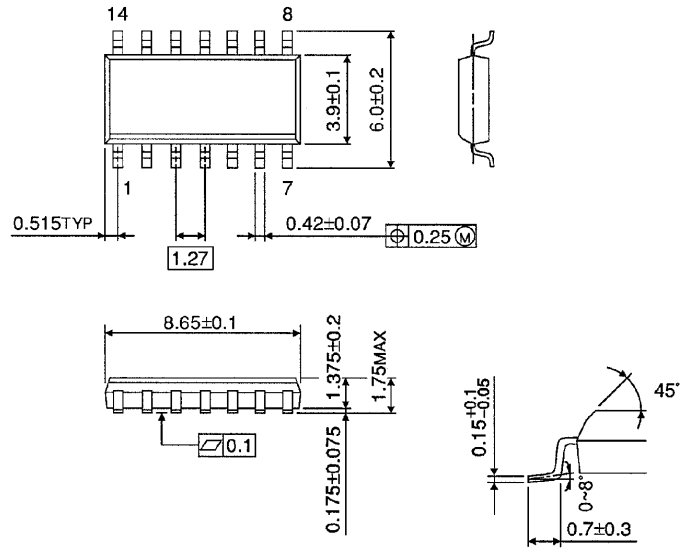


Weight : 0.18g (Typ.)

**SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOL14-P-150 -1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

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