

**TC74ACT299P, TC74ACT299F, TC74ACT299FW**

**8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR**

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74ACT299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

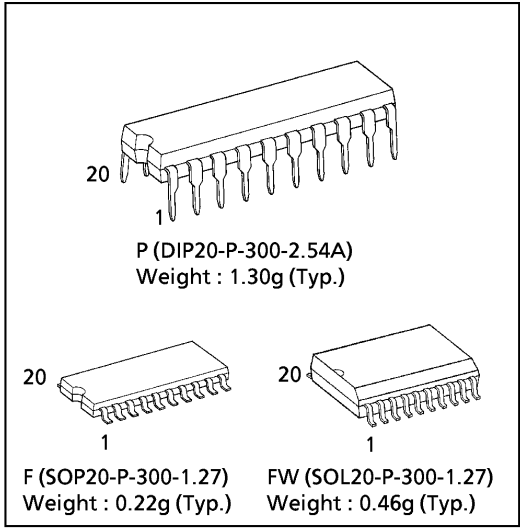
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

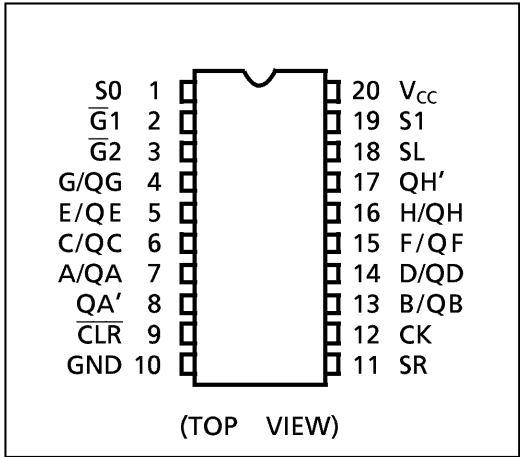
When one or both enable ( $\overline{G1}$ ,  $\overline{G2}$ ) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**FEATURES:**

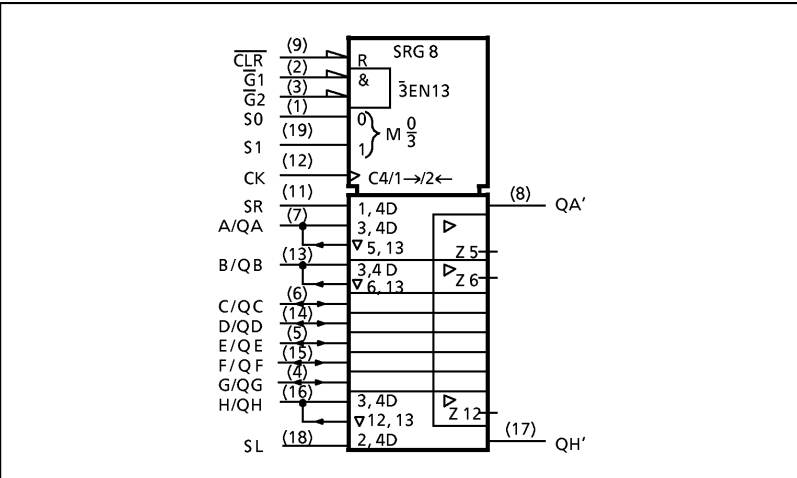
- High Speed..... $f_{MAX} = 130\text{MHz (typ.)}$   
at  $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A(Max.)}$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs ...  $V_{IL} = 0.8\text{V(Max.)}$   
 $V_{IH} = 2.0\text{V(Min.)}$
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 24\text{mA (Min.)}$   
Capability of driving  $50\Omega$  transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F299



**PIN ASSIGNMENT**



**IEC LOGIC SYMBOL**



**APPLICATION NOTES**

- 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

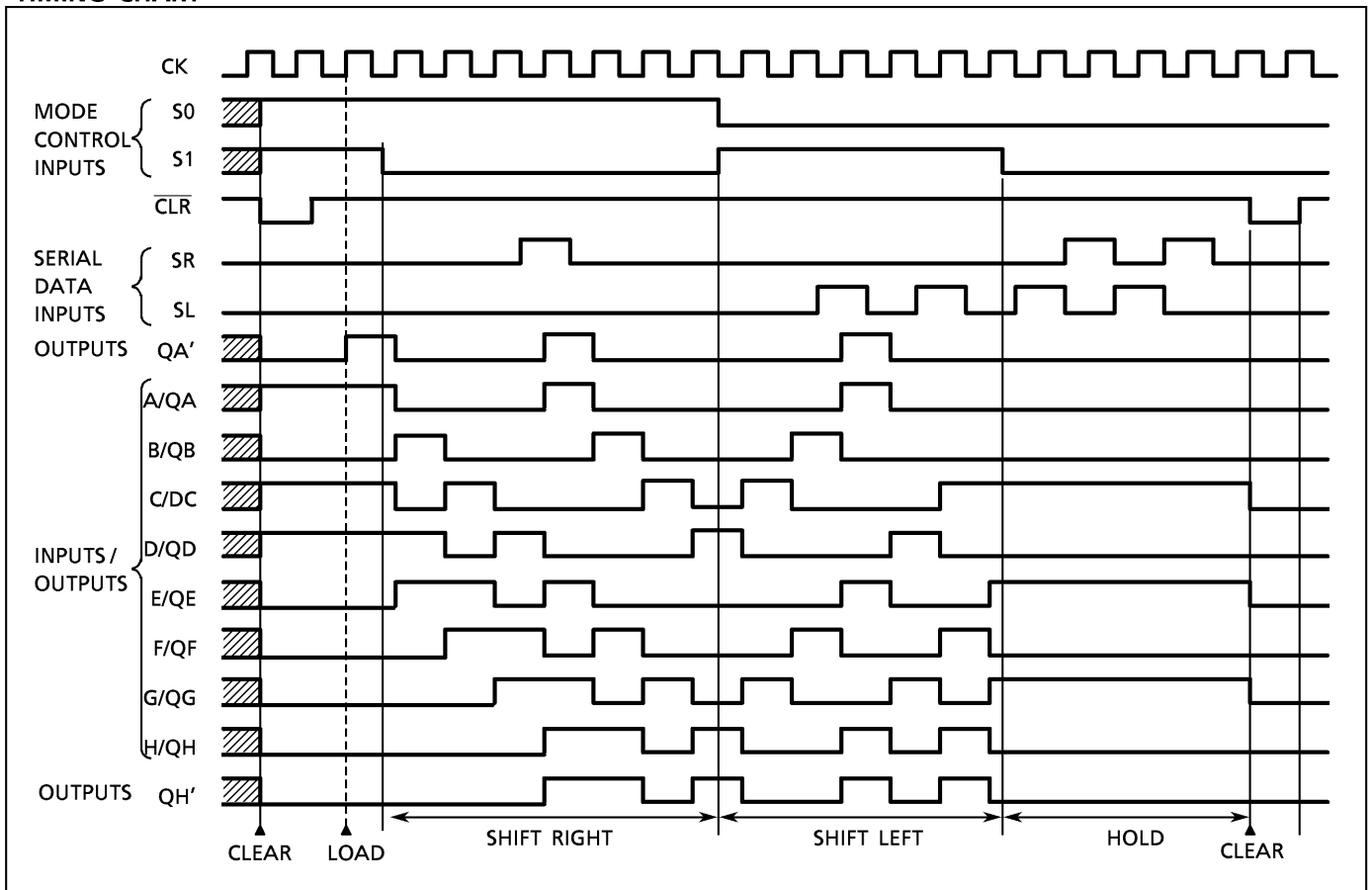
TRUTH TABLE

MODE	INPUTS								INPUTS/OUTPUTS		OUTPUTS	
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	G1*	G2*		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	$\uparrow$	X	H	H	QGn	H	QGn
SHIFT LEFT	H	H	L	L	L	$\uparrow$	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	$\uparrow$	X	X	a	h	a	h

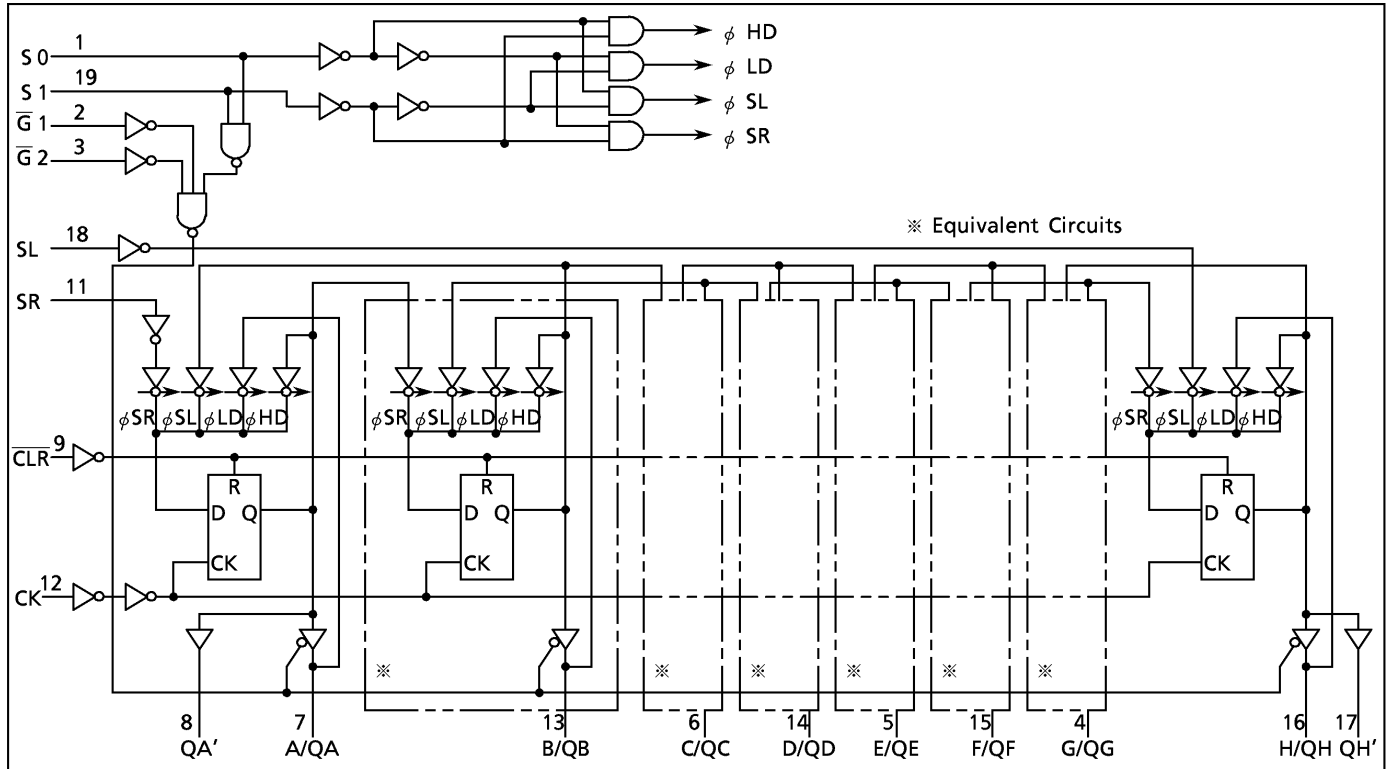
\* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

- Z : High Impedance
- Qn0 : The level of Qn before the indicated steady - state input conditions were established.
- Qnn : The level of Qn before the most recent active transition indicated by  $\uparrow$ .
- a, h : The level of the steady - state inputs A, H, respectively.
- X : Don't Care.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}$ + 0.5	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}$ + 0.5	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 50$	mA
DC Output Current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 250$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	$^{\circ}C$

\*500mW in the range of  $T_a = -40^{\circ}C \sim 65^{\circ}C$ . From  $T_a = 65^{\circ}C$  to  $85^{\circ}C$  a derating factor of  $-10mW/^{\circ}C$  should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	$^{\circ}C$
Input Rise and Fall Time	$dt/dV$	0~10	ns/V

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V <sub>IH</sub>			4.5 } 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V <sub>IL</sub>			4.5 } 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA I <sub>OH</sub> = -24mA I <sub>OH</sub> = -75mA*	4.5 4.5 5.5	4.4 3.94 —	4.5 — —	— — —	4.4 3.80 3.85	— — —	V
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA I <sub>OL</sub> = 24mA I <sub>OL</sub> = 75mA*	4.5 4.5 5.5	— — —	0.0 — —	0.1 0.36 —	— — —	0.1 0.44 1.65	V
3 - State Output Off - State Current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	8.0	—	80.0	
	I <sub>C</sub>	PER INPUT: V <sub>IN</sub> = 3.4V OTHER INPUT: V <sub>CC</sub> or GND		5.5	—	—	1.35	—	1.5	mA

\* : This spec indicates the capability of driving 50Ω transmission lines.  
One output should be tested at a time for a 10ms maximum duration.

**TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)**

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = -40~85°C	UNIT
			V <sub>CC</sub> (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t <sub>w</sub> (L) t <sub>w</sub> (H)		5.0 ± 0.5	5.0	5.0	ns
Minimum Pulse Width (CLR)	t <sub>w</sub> (L)		5.0 ± 0.5	5.0	5.0	
Minimum Set - up Time (SL, SR, A~H)	t <sub>s</sub>		5.0 ± 0.5	3.5	3.5	
Minimum Set - up Time (S0, S1)	t <sub>s</sub>		5.0 ± 0.5	6.0	6.5	
Minimum Hold Time (SL, SR, A~H)	t <sub>h</sub>		5.0 ± 0.5	2.0	2.0	
Minimum Hold Time (S0, S1)	t <sub>h</sub>		5.0 ± 0.5	0.0	0.0	
Minimum Removal Time (CLR)	t <sub>rem</sub>		5.0 ± 0.5	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ ,  $t_r = t_f = 3\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (CK-QA', QH')	t <sub>pLH</sub> t <sub>pHL</sub>		5.0 ± 0.5	—	7.2	10.5	1.0	12.0	ns
Propagation Delay Time ( $\overline{\text{CLR}}$ -QA', QH')	t <sub>pHL</sub>		5.0 ± 0.5	—	6.0	10.0	1.0	11.5	
Propagation Delay Time (CK-QA~QH)	t <sub>pLH</sub> t <sub>pHL</sub>		5.0 ± 0.5	—	7.4	11.4	1.0	13.0	
Propagation Delay Time ( $\overline{\text{CLR}}$ -QA~QH)	t <sub>pHL</sub>		5.0 ± 0.5	—	6.3	10.5	1.0	12.0	
Output Enable Time	t <sub>pZL</sub> t <sub>pZH</sub>		5.0 ± 0.5	—	7.4	11.4	1.0	13.0	
Output Disable Time	t <sub>pLZ</sub> t <sub>pHZ</sub>		5.0 ± 0.5	—	7.2	9.6	1.0	11.0	
Maximum Clock Frequency	f <sub>MAX</sub>		5.0 ± 0.5	80	120	—	80	—	MHz
Input Capacitance	C <sub>IN</sub>			—	5	10	—	10	pF
Bus Input Capacitance	C <sub>I/O</sub>			—	13	—	—	—	
Power Dissipation Capacitance	C <sub>PD</sub> (1)			—	160	—	—	—	

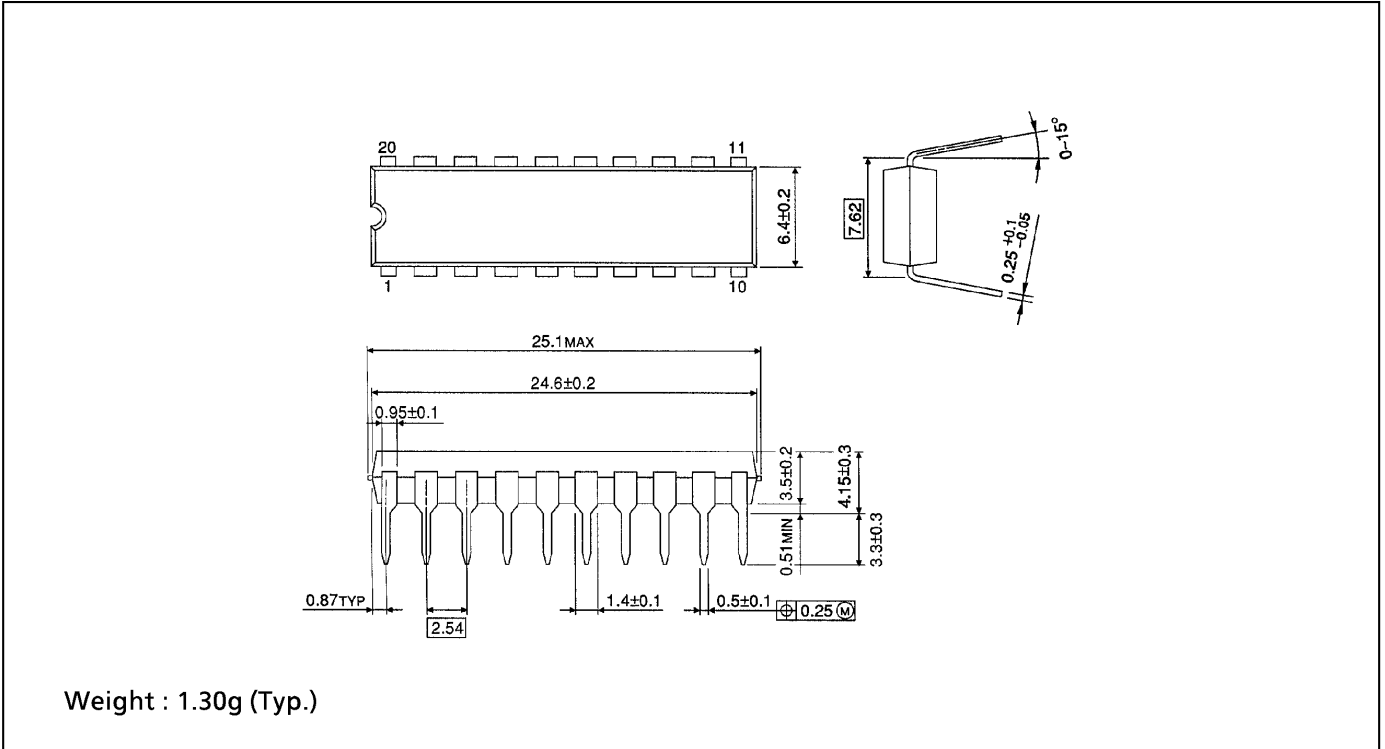
Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

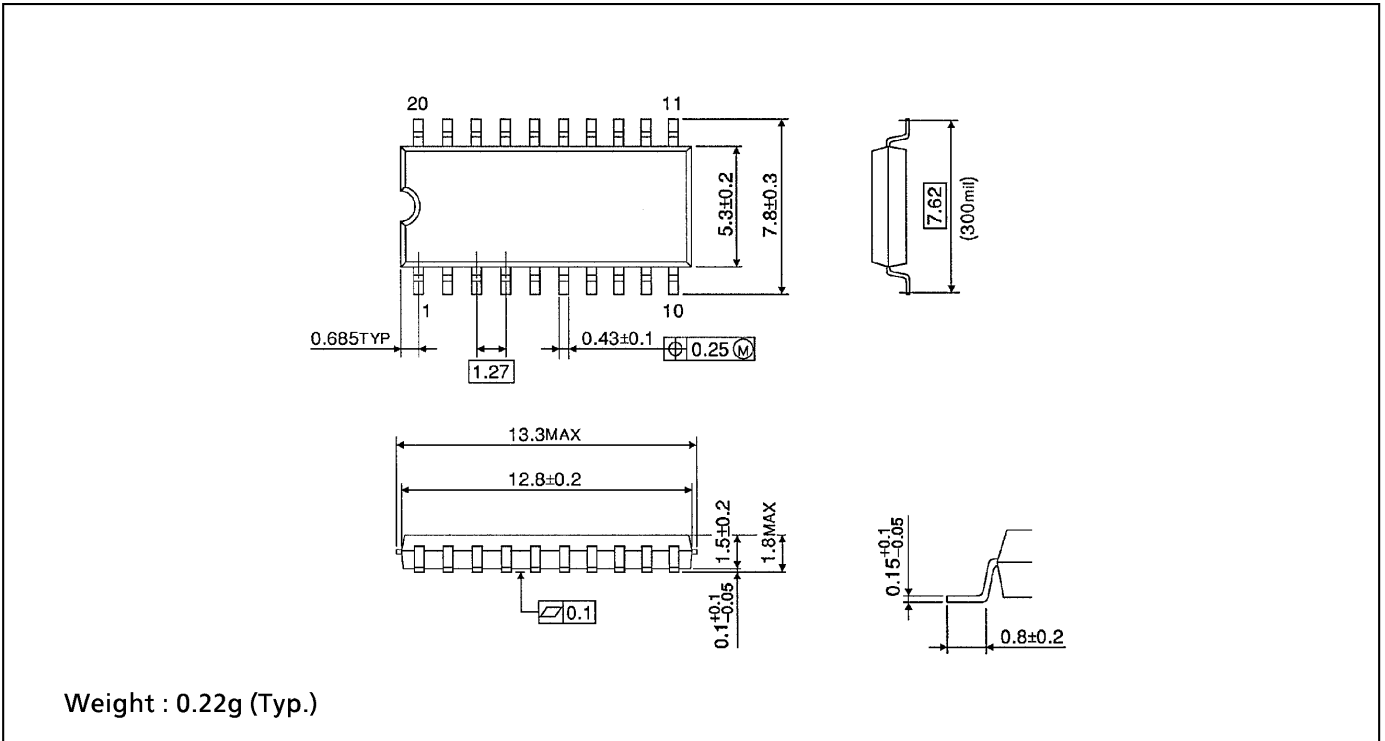
**DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)**

Unit in mm



**SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)**

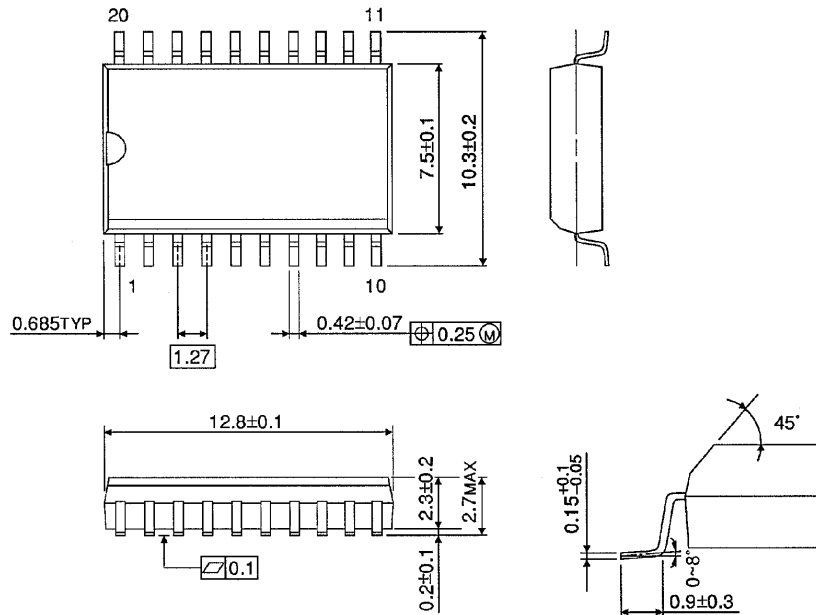
Unit in mm



**SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

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