

TC74ACT373P, TC74ACT373F, TC74ACT373FW, TC74ACT373FT

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74ACT373 is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

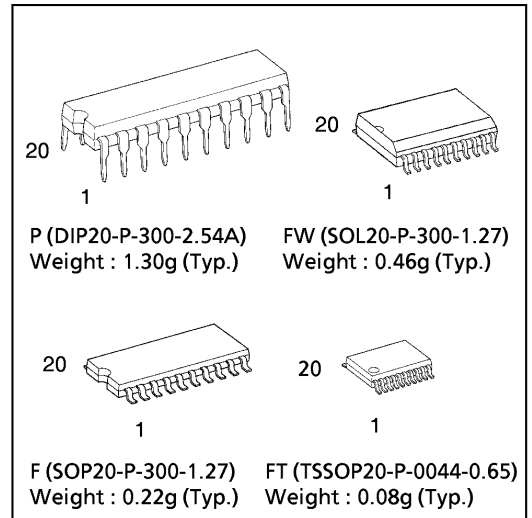
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. These 8-bit D-type latches are controlled by a latch enable (LE) and a output enable input (\overline{OE}).

When the (\overline{OE}) input is high, the eight outputs are in a high impedance state.

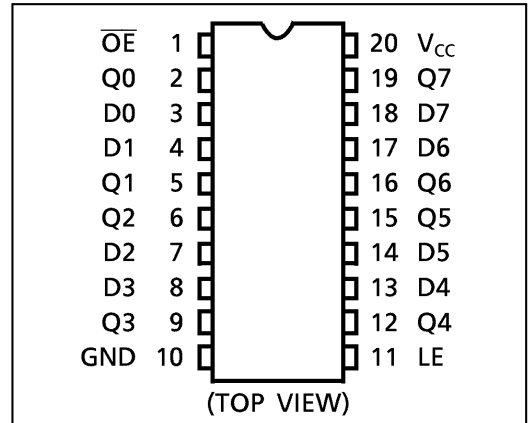
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed..... $t_{pd} = 5.2ns$ (typ.) at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 8\mu A$ (Max.) at $T_a = 25^\circ C$
- Compatible with TTL outputs..... $V_{IL} = 0.8V$ (Max.)
 $V_{IH} = 2.0V$ (Min.)
- Symmetrical Output Impedance..... $|I_{OH}| = I_{OL} = 24mA$ (Min.)
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F373



PIN ASSIGNMENT

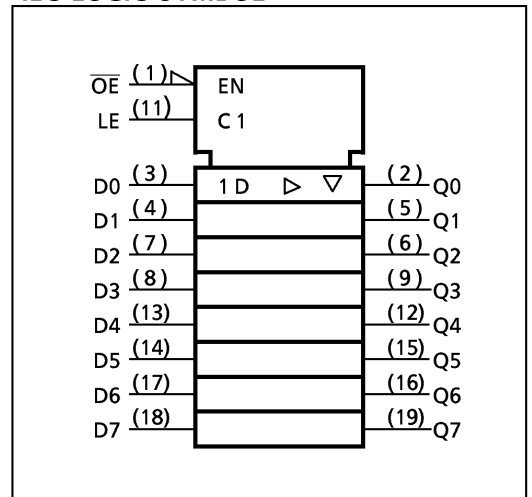


TRUTH TABLE

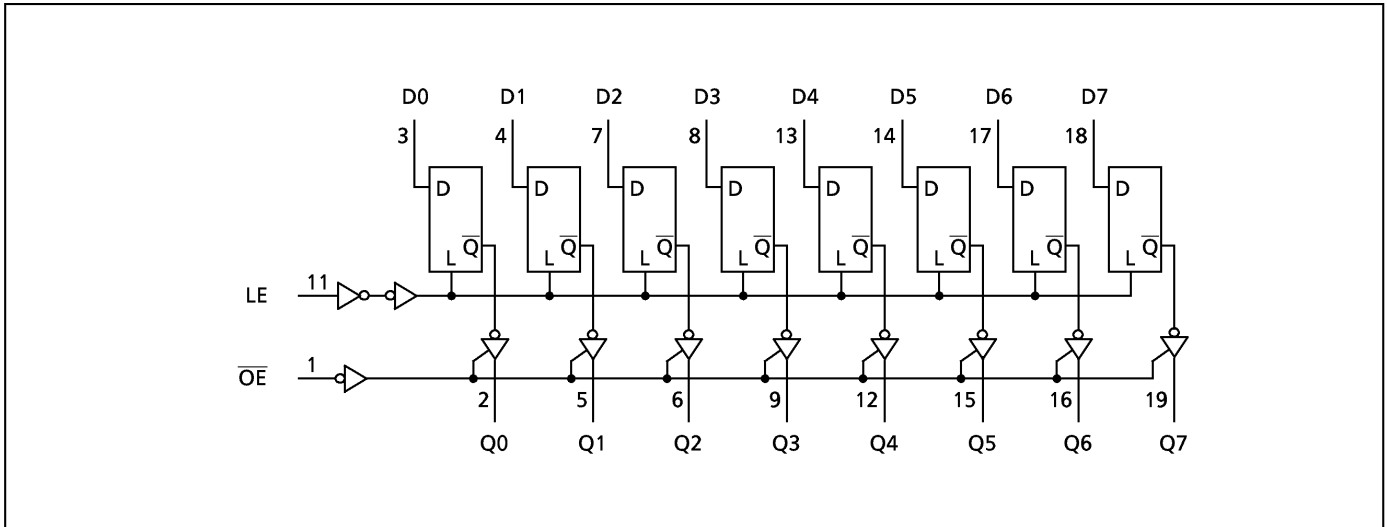
INPUTS			OUTPUTS
\overline{OE}	LE	D	Q
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
 Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	-65~150	$^{\circ}C$

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	$^{\circ}C$
Input Rise and Fall Time	dt/dV	0~10	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC}	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			4.5 } 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V _{IL}			4.5 } 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	4.5	4.4	4.5	—	4.4	—	V
			I _{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I _{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I _{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I _{OL} = 75mA*	5.5	—	—	—	—	1.65	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	8.0	—	80.0	
	I _C	PER INPUT : V _{IN} = 3.4V OTHER INPUT : V _{CC} or GND		5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = 25°C	Ta = -40~85°C	UNIT
			V _{CC}	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (LE)	t _W (H)		5.0 ± 0.5	—	5.0	5.0	ns
Minimum Set - up Time	t _s		5.0 ± 0.5	—	2.0	2.0	
Minimum Hold Time	t _h		5.0 ± 0.5	—	3.0	3.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC}	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (LE-Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	—	5.8	9.2	1.0	10.5	ns
Propagation Delay Time (D-Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	—	5.9	9.6	1.0	11.0	
Output Enable Time	t_{pZL} t_{pZH}		5.0 ± 0.5	—	6.5	10.5	1.0	12.0	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0 ± 0.5	—	5.5	7.8	1.0	9.0	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Output Capacitance	C _{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	C _{PD} (1)			—	32	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Latch)}$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 20 + 12 \cdot n$$

DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

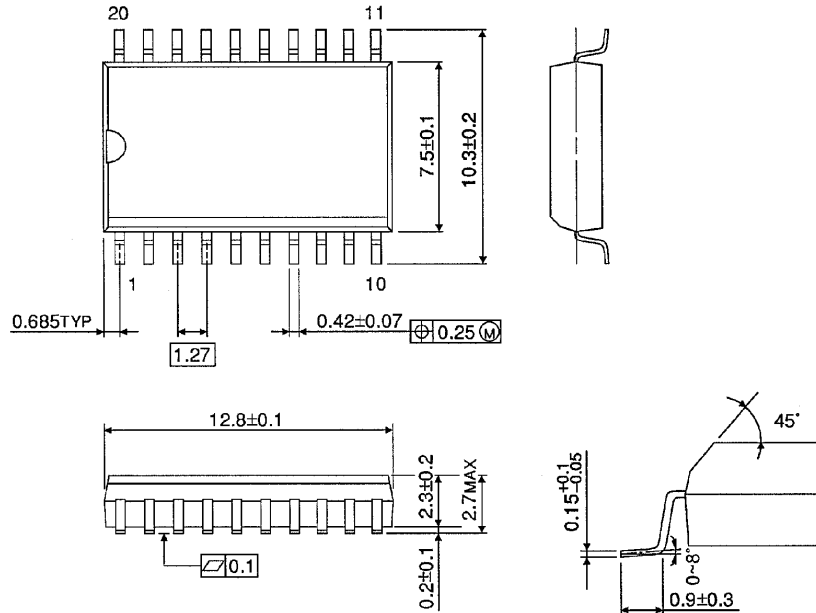
Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm

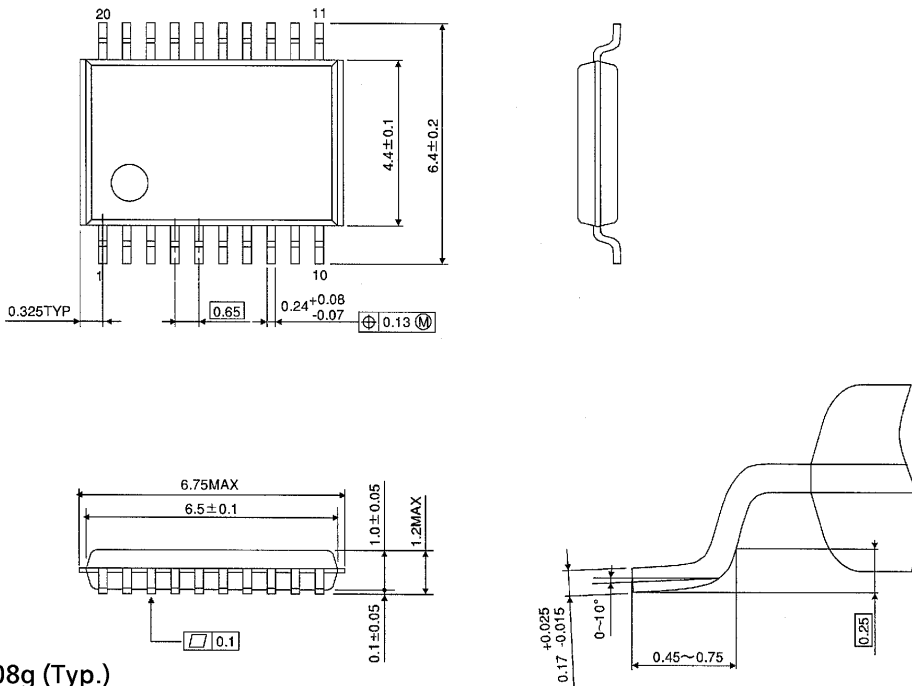
(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65)

Unit in mm



Weight : 0.08g (Typ.)

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000707EBA

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