

TC74HC374AP, TC74HC374AF, TC74HC374AFW

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The TC74HC374A is a high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input (\overline{OE}).

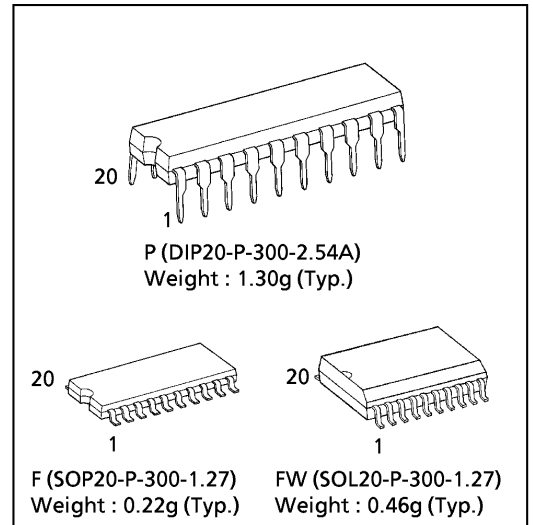
When the \overline{OE} input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

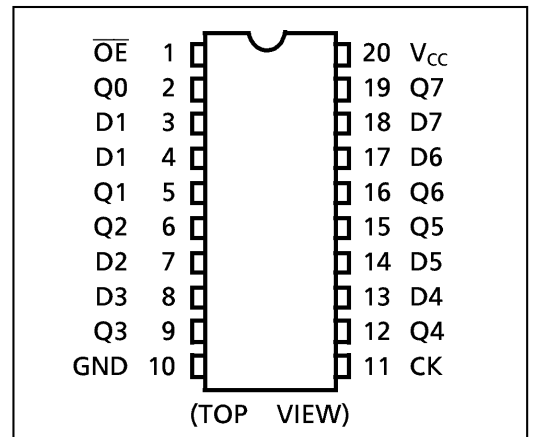
FEATURES:

- High Speed..... $f_{MAX} = 77\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability..... 15 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 6\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS374

(Note) The JEDEC SOP (FW) is not available in Japan.



PIN ASSIGNMENT

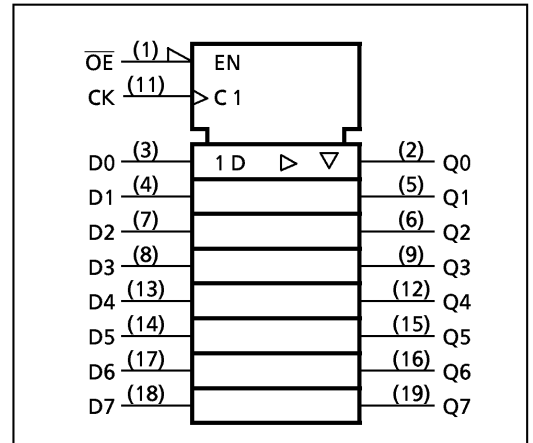


TRUTH TABLE

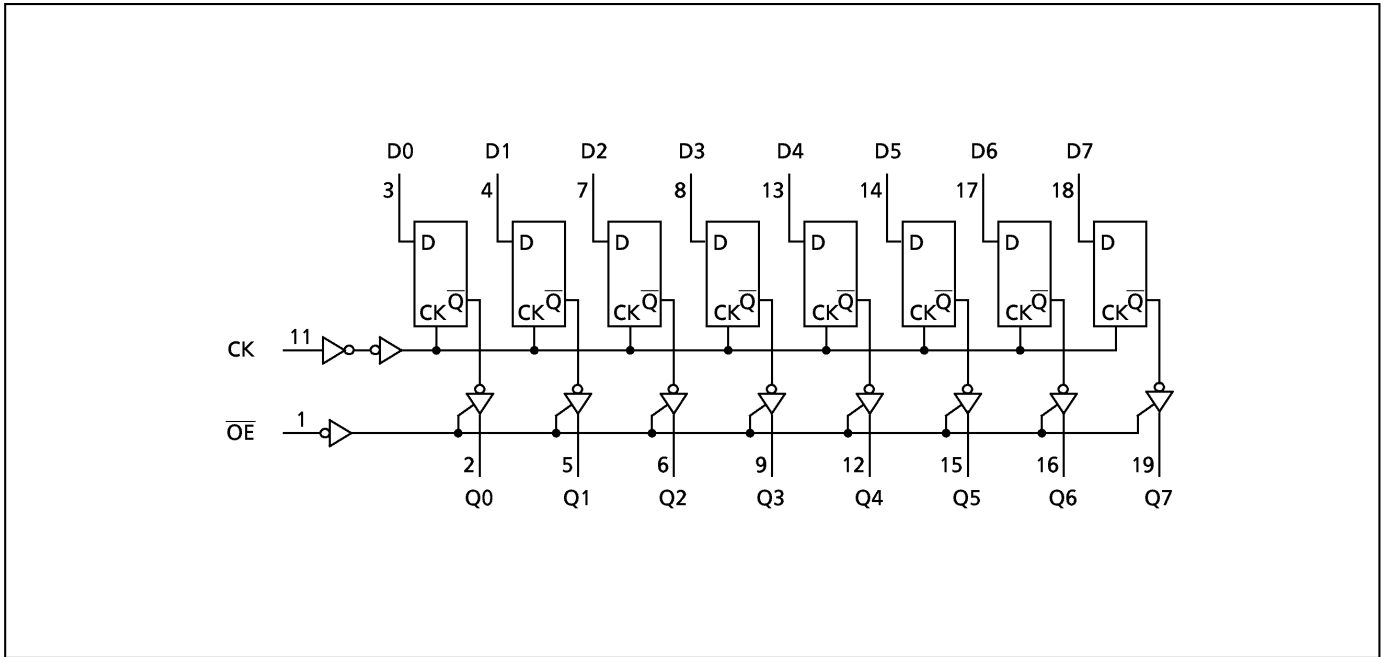
INPUTS			OUTPUTS
\overline{OE}	CK	D	Q
H	X	X	Z
L		X	Q_n
L		L	L
L		H	H

X : Don't Care
Z : High Impedance
 Q_n : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 ($V_{CC} = 2.0\text{V}$) 0~ 500 ($V_{CC} = 4.5\text{V}$) 0~ 400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V	
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	— — —	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -6\text{ mA}$ $I_{OH} = -7.8\text{mA}$	4.5	4.18	4.31	—	4.13	—	V
				6.0	5.68	5.80	—	5.63	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 6\text{ mA}$ $I_{OL} = 7.8\text{mA}$	4.5	—	0.17	0.26	—	0.33	V
				6.0	—	0.18	0.26	—	0.33	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0	—	—	± 0.5	—	± 5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0		

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C		Ta = -40-85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (Dn)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time (Dn)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40-85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		50	2.0	—	20	60	—	75	ns
				4.5	—	6	12	—	15	
				6.0	—	5	10	—	13	
Propagation Delay Time (CK-Q)	t_{pLH}		50	2.0	—	45	140	—	175	
				4.5	—	15	28	—	35	
				6.0	—	13	24	—	30	
	t_{pHL}		150	2.0	—	60	190	—	240	
				4.5	—	20	38	—	48	
				6.0	—	17	32	—	41	
Output Enable Time	t_{pZL}	$R_L = 1k\Omega$	50	2.0	—	39	135	—	170	
				4.5	—	13	27	—	34	
				6.0	—	11	23	—	29	
	t_{pZH}		150	2.0	—	54	185	—	230	
				4.5	—	18	37	—	46	
				6.0	—	15	31	—	39	
Output Enable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	2.0	—	30	135	—	170	
				4.5	—	13	27	—	34	
				6.0	—	12	23	—	29	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	18	—	5	—	MHz
				4.5	31	75	—	25	—	
				6.0	36	90	—	29	—	
Input Capacitance	C _{IN}				—	5	10	—	10	pF
Output Capacitance	C _{OUT}				—	10	—	—	—	
Power Dissipation Capacitance	C _{PD} (1)				—	47	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Flip Flop)}$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 30 + 17 \cdot n$$

DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

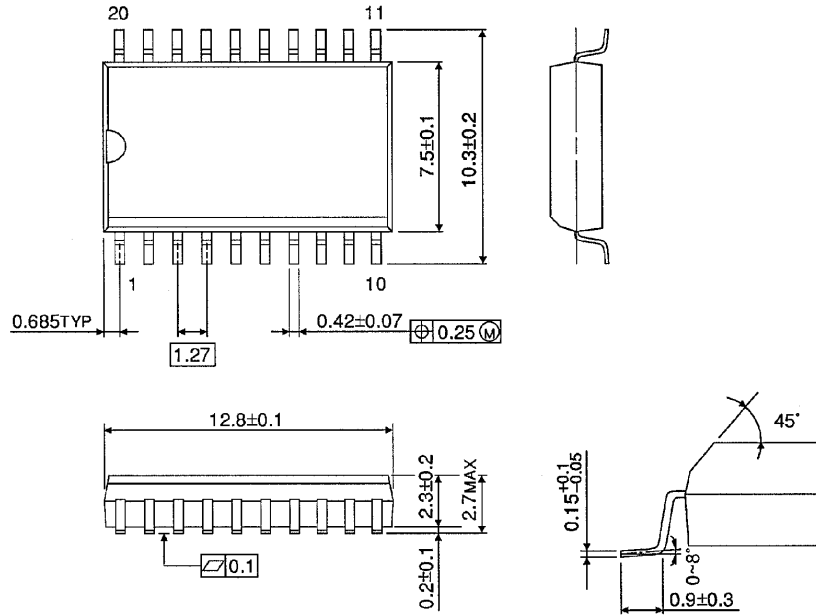
Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

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