

# TC74HC4520AP, TC74HC4520AF

## DUAL 4 - BIT BINARY COUNTER

The TC74HC4520A is high speed CMOS DUAL BCD / 4 - BIT BINARY COUNTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Since it contains two independent counter circuits in one package, counting or frequency division of eight binary bits can be achieved with one device. The counter is reset to "0" (Q0~Q3 low) by setting the CLR input high regardless of the other inputs.

Counting occurs on the positive going (rising edge) transition of CK if CE is high or the negative going (falling edge) transition of CK if CE is low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

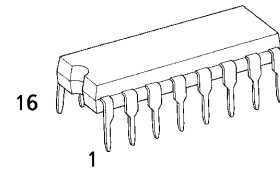
### FEATURES:

- High Speed..... $f_{MAX} = 55\text{MHz}(\text{typ.})$   
at  $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range...  $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with TC4520B

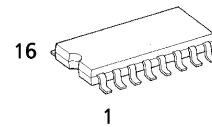
### TRUTH TABLE

INPUT			FUNCTION
CK	CE	CLR	
	H	L	INCREMENT COUNTER
L		L	INCREMENT COUNTER
	X	L	NO CHANGE
X		L	NO CHANGE
	L	L	NO CHANGE
H		L	NO CHANGE
X	X	H	Q0 THRU Q3 = L

X : Don't Care

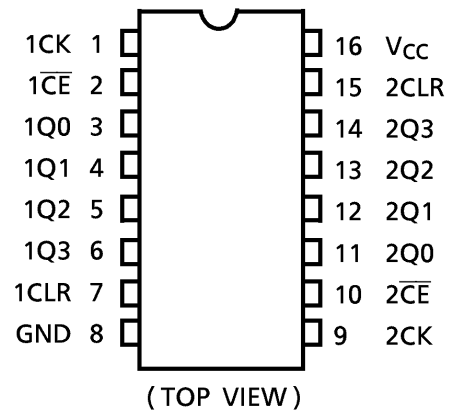


P (DIP16-P-300-2.54A)  
Weight : 1.00g (Typ.)

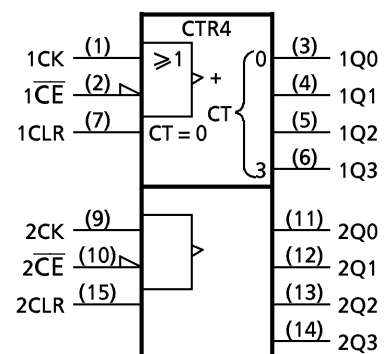


F (SOP16-P-300-1.27)  
Weight : 0.18g (Typ.)

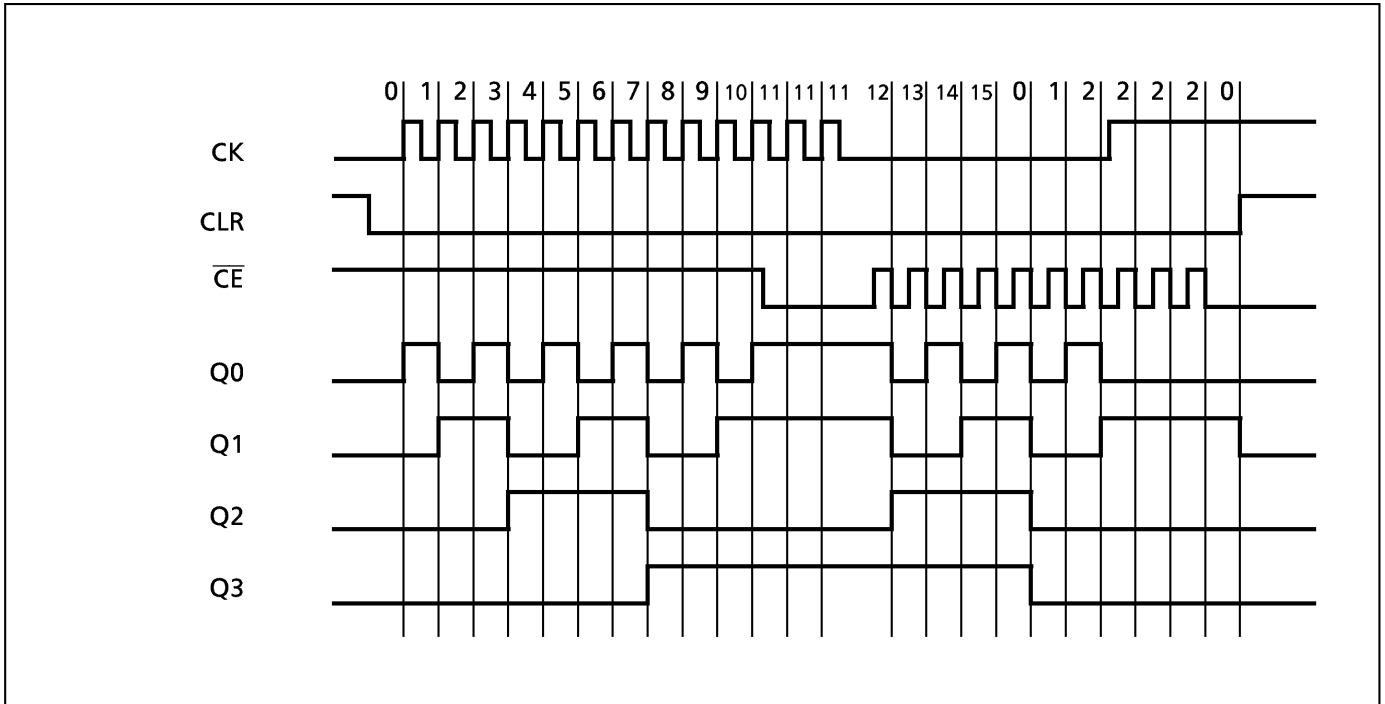
### PIN ASSIGNMENT



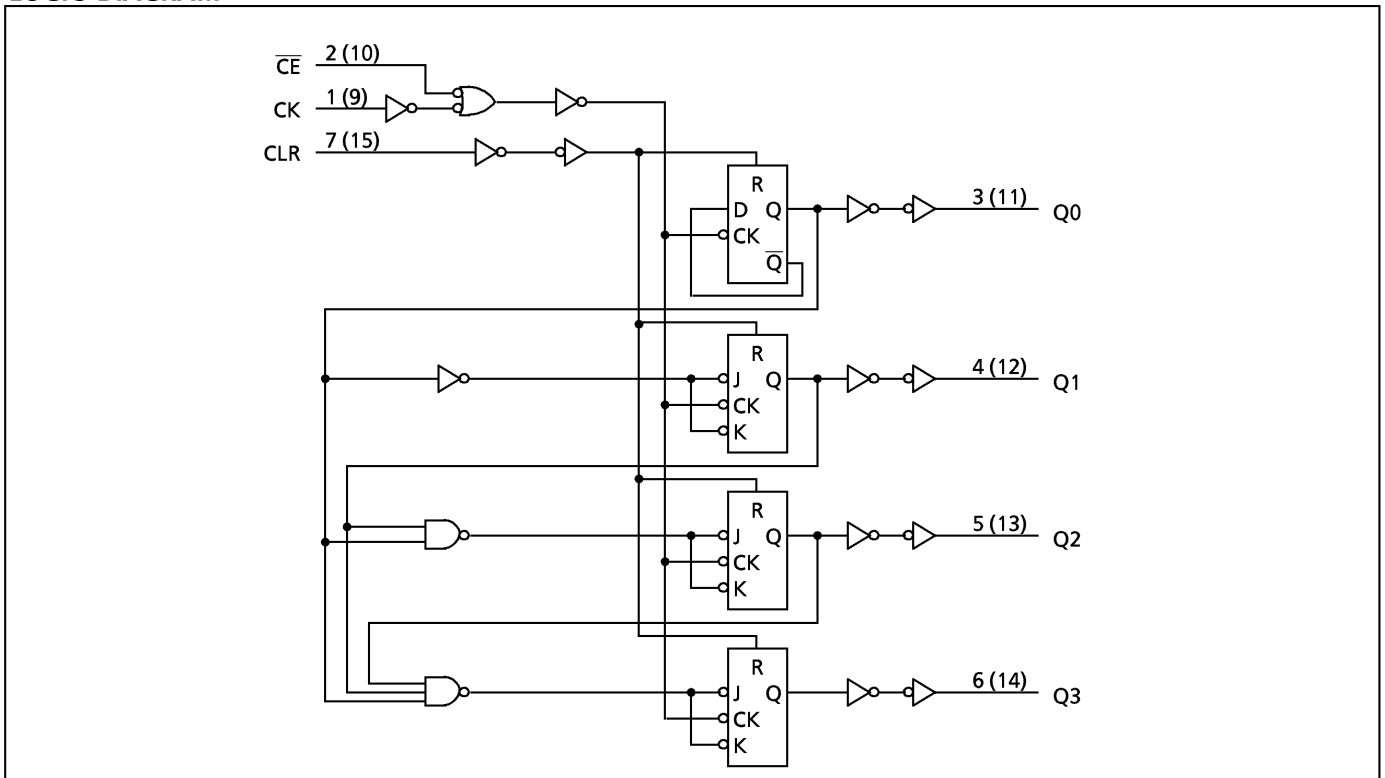
### IEC LOGIC SYMBOL



TIMING CHART



LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$ . From  $T_a = 65^\circ\text{C}$  to  $85^\circ\text{C}$  a derating factor of  $-10\text{mW}/^\circ\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT			
				MIN.	TYP.	MAX.	MIN.	MAX.				
High - Level Input Voltage	$V_{IH}$		2.0	1.50	—	—	1.50	—	V			
			4.5	3.15	—	—	3.15	—				
			6.0	4.20	—	—	4.20	—				
Low - Level Input Voltage	$V_{IL}$		2.0	—	—	0.50	—	0.50	V			
			4.5	—	—	1.35	—	1.35				
			6.0	—	—	1.80	—	1.80				
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V		
				4.5	4.4	4.5	—	4.4	—			
				6.0	5.9	6.0	—	5.9	—			
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V		
				4.5	—	0.0	0.1	—	0.1			
				6.0	—	0.0	0.1	—	0.1			
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$			
			Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—		4.0	—	40.0

TIMING REQUIREMENTS ( Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK, $\overline{CE}$ )	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLR)	$t_{W(H)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Removal Time	$t_{rem}$		2.0	—	50	60	
			4.5	—	10	12	
			6.0	—	9	11	
Clock Frequency	f		2.0	—	6	4	MHz
			4.5	—	30	24	
			6.0	—	35	28	

AC ELECTRICAL CHARACTERISTICS ( $C_L = 15\text{pF}$ ,  $V_{CC} = 5\text{V}$ , Ta = 25°C, Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$		—	4	8	ns
	$t_{THL}$		—	4	8	
Propagation Delay Time (CK, $\overline{CE}$ —Qn)	$t_{pLH}$		—	17	27	
	$t_{pHL}$		—	15	25	
Propagation Delay Time (CLR—Qn)	$t_{pHL}$		—	15	25	
Maximum Clock Frequency	$f_{MAX}$		33	55	—	MHz

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$ $t_{THL}$		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (CK, $\overline{CE}$ —Qn)	$t_{pLH}$ $t_{pHL}$		2.0	—	72	160	—	200	
			4.5	—	22	32	—	40	
			6.0	—	18	27	—	34	
Propagation Delay Time (CLR—Qn)	$t_{pHL}$		2.0	—	65	150	—	190	
			4.5	—	20	30	—	38	
			6.0	—	16	26	—	33	
Maximum Clock Frequency	$f_{MAX}$		2.0	6	23	—	4	—	MHz
			4.5	30	51	—	24	—	
			6.0	35	60	—	28	—	
Input Capacitance	$C_{IN}$			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}$	Note (1)		—	32	—	—	—	

Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per circuit)}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)

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