

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCX162843FT

Low-Voltage 18-Bit D-Type Latch with 3.6-V Tolerant Inputs and Outputs

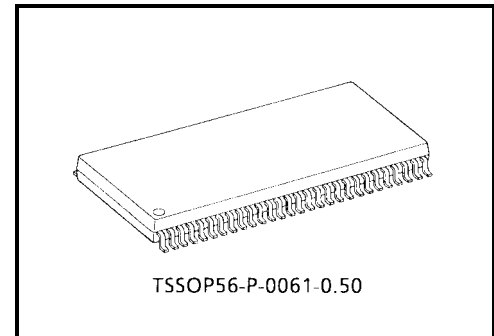
The TC74VCX162843FT is a high-performance CMOS 18-bit D-type latch. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

The TC74VCX162843FT can be used as two 9-bit latches or one 18-bit latch. The 18 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 9-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs. CLR and PR are independent of the CK and are accomplished by setting the appropriate input low. When the OE input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The 26- Ω series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.

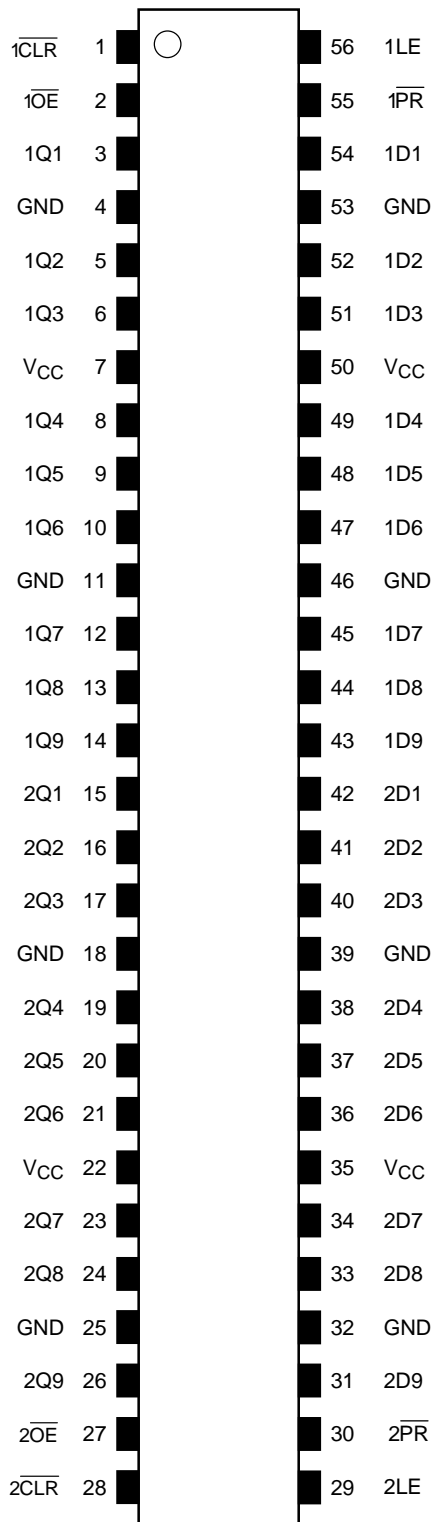


Weight: 0.25 g (typ.)

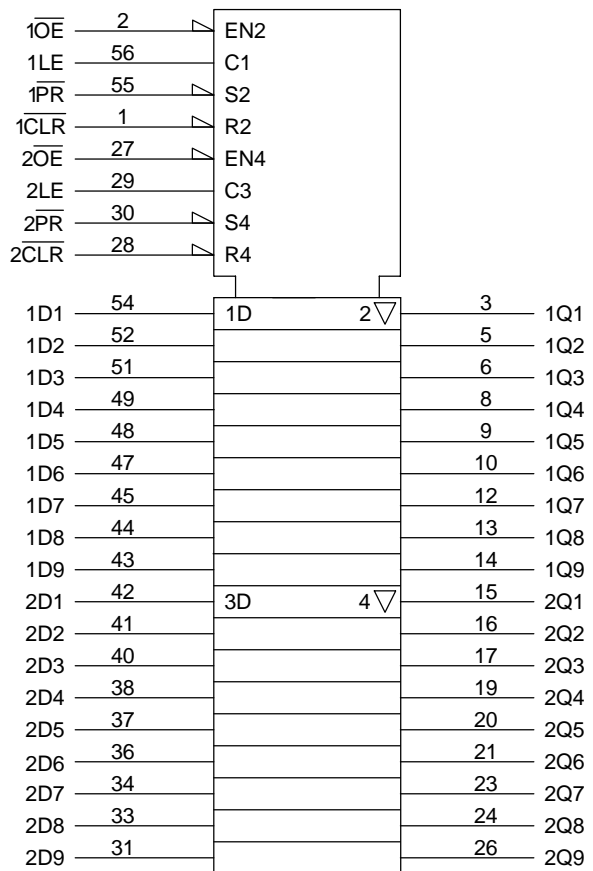
Features

- 26- Ω series resistors on outputs
- Low-voltage operation: $V_{CC} = 1.8$ to 3.6 V
- High-speed operation: $t_{pd} = 3.9$ ns (max) ($V_{CC} = 3.0$ to 3.6 V)
 : $t_{pd} = 5.1$ ns (max) ($V_{CC} = 2.3$ to 2.7 V)
 : $t_{pd} = 9.8$ ns (max) ($V_{CC} = 1.8$ V)
- Output current: $I_{OH}/I_{OL} = \pm 12$ mA (min) ($V_{CC} = 3.0$ V)
 : $I_{OH}/I_{OL} = \pm 8$ mA (min) ($V_{CC} = 2.3$ V)
 : $I_{OH}/I_{OL} = \pm 4$ mA (min) ($V_{CC} = 1.8$ V)
- Latch-up performance: ± 300 mA
- ESD performance: Machine model $> \pm 200$ V
 : Human body model $> \pm 2000$ V
- Package: TSSOP (thin shrink small outline package)
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

Pin Assignment (top view)



IEC Logic Symbol



Truth Table (each 9-bit latch)

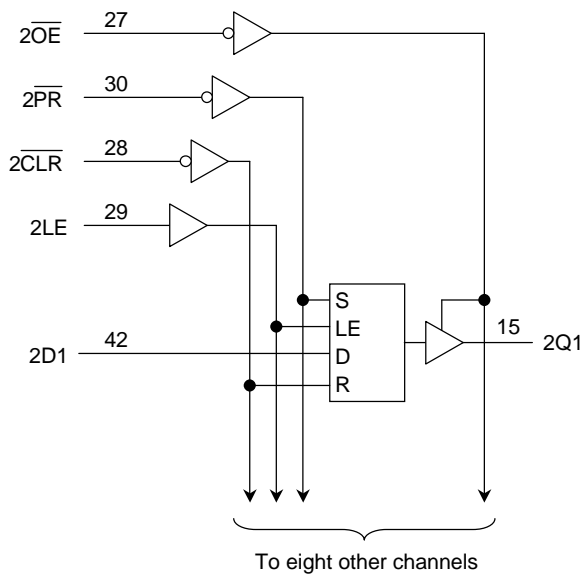
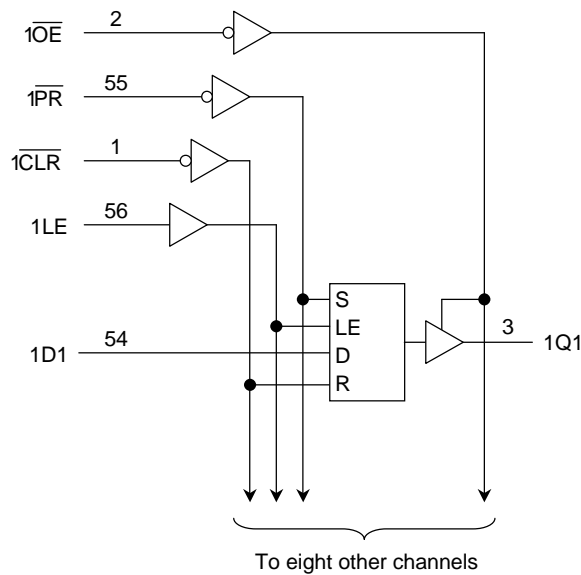
Inputs					Outputs Q
$\overline{\text{PR}}$	$\overline{\text{CLR}}$	$\overline{\text{OE}}$	LE	D	
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Qn
X	X	H	X	X	Z

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to 4.6	V
DC input voltage	V_{IN}	-0.5 to 4.6	V
DC output voltage	V_{OUT}	-0.5 to 4.6 (Note 1)	V
		-0.5 to $V_{CC} + 0.5$ (Note 2)	
Input diode current	I_{IK}	-50	mA
Output diode current	I_{OK}	± 50 (Note 3)	mA
DC output current	I_{OUT}	± 50	mA
Power dissipation	P_D	400	mW
DC V_{CC} /ground current per supply pin	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: OFF state

Note 2: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Range

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 3.6	V
		1.2 to 3.6 (Note 4)	
Input voltage	V_{IN}	-0.3 to 3.6	V
Output voltage	V_{OUT}	0 to 3.6 (Note 5)	V
		0 to V_{CC} (Note 6)	
Output current	I_{OH}/I_{OL}	± 12 (Note 7)	mA
		± 8 (Note 8)	
		± 4 (Note 9)	
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 10)	ns/V

Note 4: Data retention only

Note 5: OFF state

Note 6: High or low state

Note 7: $V_{CC} = 3.0$ to 3.6 V

Note 8: $V_{CC} = 2.3$ to 2.7 V

Note 9: $V_{CC} = 1.8$ V

Note 10: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C, 2.7 V < VCC ≤ 3.6 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V _{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.7 to 3.6	V _{CC} - 0.2	—	V
				I _{OH} = -6 mA	2.7	2.2	—	
				I _{OH} = -8 mA	3.0	2.4	—	
				I _{OH} = -12 mA	3.0	2.2	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I _{OL} = 6 mA	2.7	—	0.4	
				I _{OL} = 8 mA	3.0	—	0.55	
				I _{OL} = 12 mA	3.0	—	0.8	
Input leakage current		I _{IN}	V _{IN} = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA
Power-off leakage current		I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.7 to 3.6	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.7 to 3.6	—	±20.0	
Increase in I _{CC} per input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V		2.7 to 3.6	—	750	

DC Characteristics (Ta = -40 to 85°C, 2.3 V ≤ VCC ≤ 2.7 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V _{IL}	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.3 to 2.7	V _{CC} - 0.2	—	V
				I _{OH} = -4 mA	2.3	2.0	—	
				I _{OH} = -6 mA	2.3	1.8	—	
				I _{OH} = -8 mA	2.3	1.7	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3 to 2.7	—	0.2	
				I _{OL} = 6 mA	2.3	—	0.4	
				I _{OL} = 8 mA	2.3	—	0.6	
Input leakage current		I _{IN}	V _{IN} = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA
Power-off leakage current		I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.3 to 2.7	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.3 to 2.7	—	±20.0	

DC Characteristics (Ta = -40 to 85°C, 1.8 V ≤ VCC < 2.3 V)

Characteristics		Symbol	Test Circuit	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—	—		1.8 to 2.3	0.7 × V _{CC}	—	V
	L-level	V _{IL}	—	—		1.8 to 2.3	—	0.2 × V _{CC}	
Output voltage	H-level	V _{OH}	—	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	1.8	V _{CC} - 0.2	—	V
					I _{OH} = -4 mA	1.8	1.4	—	
	L-level	V _{OL}	—	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.8	—	0.2	
					I _{OL} = 4 mA	1.8	—	0.3	
Input leakage current		I _{IN}	—	V _{IN} = 0 to 3.6 V		1.8	—	±5.0	μA
3-state output OFF state current		I _{OZ}	—	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V		1.8	—	±10.0	μA
Power-off leakage current		I _{OFF}	—	V _{IN} , V _{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I _{CC}	—	V _{IN} = V _{CC} or GND		1.8	—	20.0	μA
				V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		1.8	—	±20.0	

AC Characteristics (Ta = -40 to 85°C, input: tr = tf = 2.0 ns, CL = 30 pF, RL = 500 Ω)

Characteristics	Symbol	Test Condition	VCC (V)	Min	Max	Unit
Propagation delay time (D-Q)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.1	
			3.3 ± 0.3	0.6	3.9	
Propagation delay time (LE-Q)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.8	
			3.3 ± 0.3	0.6	4.4	
Propagation delay time ($\overline{\text{PR}}$ -Q)	t _{pLH}	Figure 1, Figure 3	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	7.0	
			3.3 ± 0.3	0.6	4.9	
Propagation delay time ($\overline{\text{CLR}}$ -Q)	t _{pHL}	Figure 1, Figure 3	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	6.0	
			3.3 ± 0.3	0.6	4.6	
3-state output enable time	t _{pZL} t _{pZH}	Figure 1, Figure 4	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.9	
			3.3 ± 0.3	0.6	4.3	
3-state output disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 4	1.8	1.5	8.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	4.3	
Minimum pulse width (LE, $\overline{\text{PR}}$, $\overline{\text{CLR}}$)	t _W (H) t _W (L)	Figure 1, Figure 2, Figure 3	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time	t _s	Figure 1, Figure 2	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t _h	Figure 1, Figure 2	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Minimum removal time	t _{rem}	Figure 1, Figure 5	1.8	4.0	—	ns
			2.5 ± 0.2	3.0	—	
			3.3 ± 0.3	2.0	—	
Output to output skew	t _{osLH} t _{osHL}	(Note 11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 11: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic Switching Characteristics

($T_a = 25^\circ\text{C}$, input: $t_r = t_f = 2.0 \text{ ns}$, $C_L = 30 \text{ pF}$, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	0.15	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	0.25	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	0.35	
Quiet output minimum dynamic V _{OL}	V _{OLV}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	-0.15	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	-0.25	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	-0.35	
Quiet output minimum dynamic V _{OH}	V _{OHV}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	1.55	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	2.05	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	2.65	

Note 12: Parameter guaranteed by design.

Capacitive Characteristics ($T_a = 25^\circ\text{C}$)

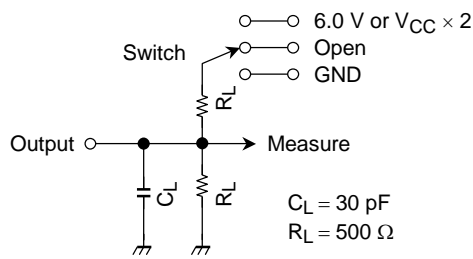
Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Input capacitance	C _{IN}	—	1.8, 2.5, 3.3	6	pF
Output capacitance	C _O	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz (Note 13)	1.8, 2.5, 3.3	20	pF

Note 13: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/18 \text{ (per bit)}$$

AC Test Circuit



Parameter	Switch
t_{pLH} , t_{pHL}	Open
t_{pLZ} , t_{pZL}	6.0 V $V_{CC} \times 2$
t_{pHZ} , t_{pZH}	GND

@ $V_{CC} = 3.3 \pm 0.3 \text{ V}$
 @ $V_{CC} = 2.5 \pm 0.2 \text{ V}$
 @ $V_{CC} = 1.8 \text{ V}$

Figure 1

AC Waveform

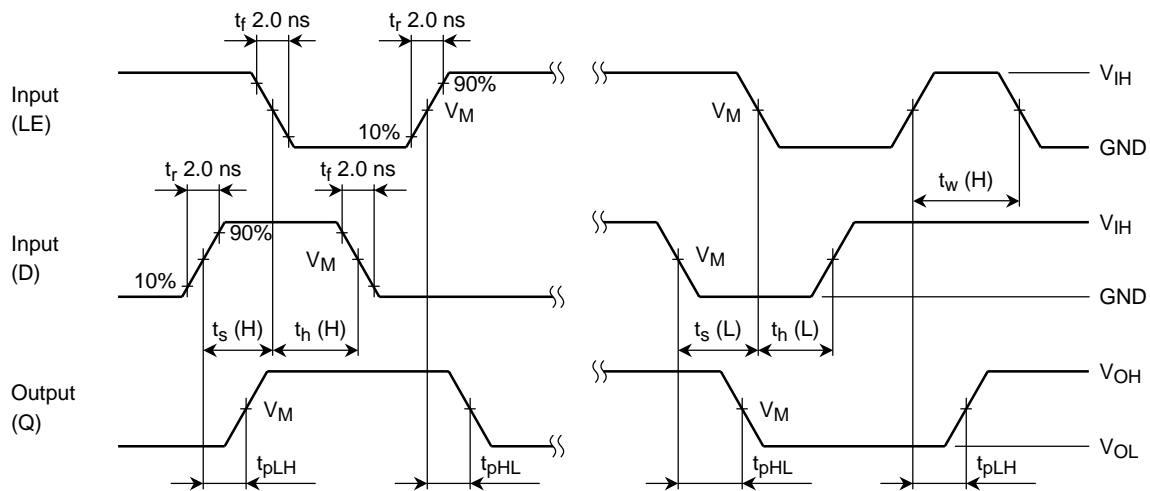


Figure 2 t_{pLH} , t_{pHL} , t_w , t_s , t_h

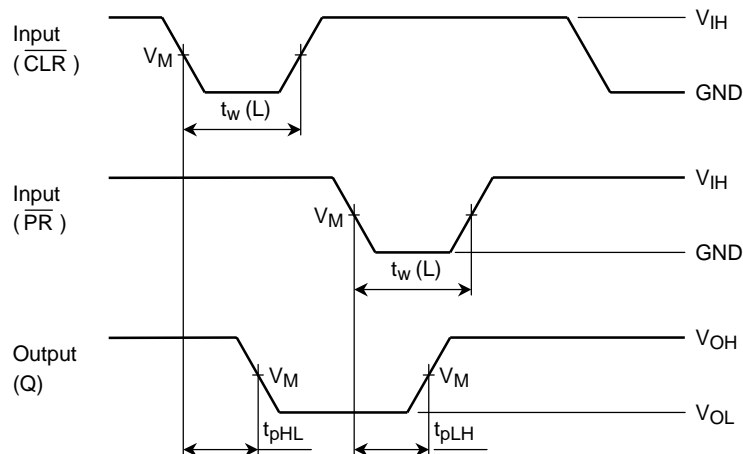


Figure 3 t_{pLH} , t_{pHL} , t_w

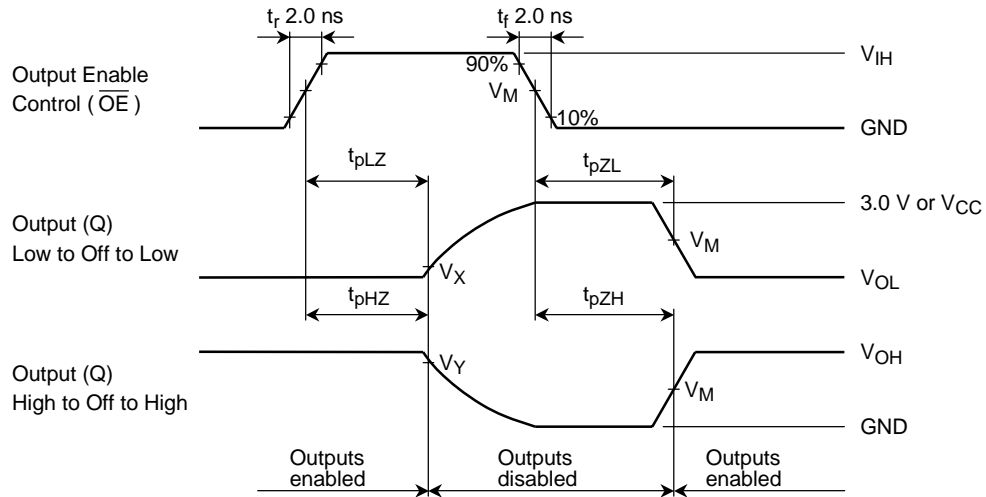


Figure 4 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

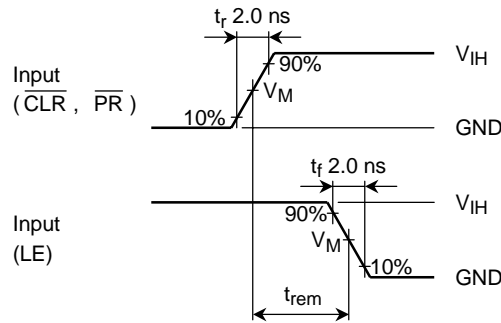


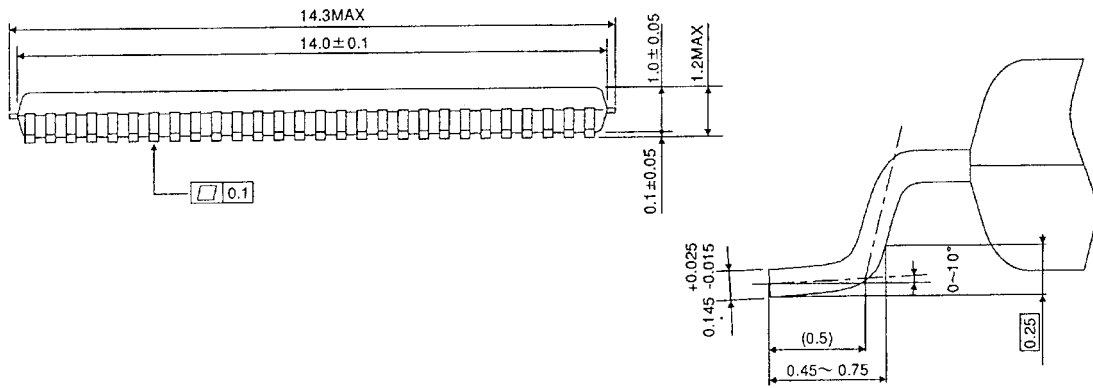
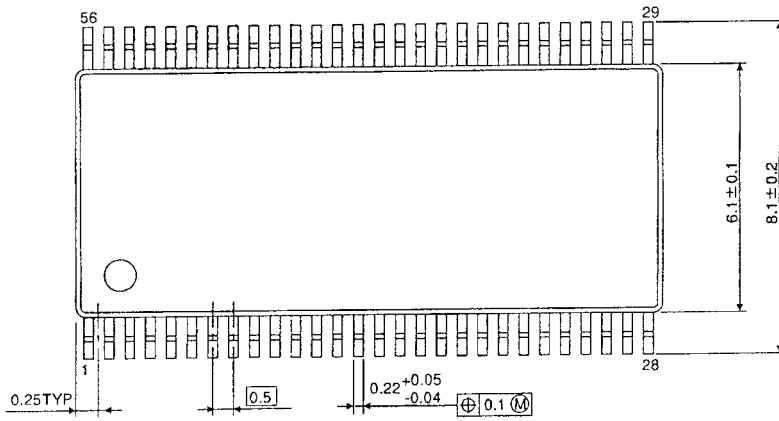
Figure 5 t_{rem}

Symbol	V_{CC}		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
V_Y	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

Package Dimensions

TSSOP56-P-0061-0.50

Unit : mm



Weight: 0.25 g (typ.)

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000707EBA

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