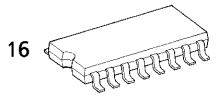
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

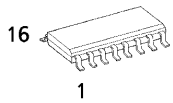
TC74VHC123AF, TC74VHC123AFN, TC74VHC123AFT
TC74VHC221AF, TC74VHC221AFN, TC74VHC221AFT

DUAL MONOSTABLE MULTIVIBRATOR
TC74VHC123AF / AFN / AFT RETRIGGERBLE
TC74VHC221AF / AFN / AFT NON - RETRIGGERBLE

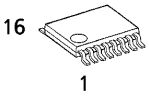
(Note) : The JEDEC SOP (FN) is not available in Japan.



F (SOP16-P-300-1.27)
Weight : 0.18 g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13 g (Typ.)



FT (TSSOP16-P-0044-0.65)
Weight : 0.06 g (Typ.)

The TC74VHC123A / 221A are high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C2MOS technology.

There are two trigger inputs, $\overline{A}$ input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal (tr = tf = 1 s) as they are schmitt trigger inputs. This device may also be triggered by using $\overline{CLR}$ input (Positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (Rx, Cx). A low level at the $\overline{CLR}$ input breaks this state.

Limits for Cx and Rx are:

External capacitor, Cx ····· No limit

External resistor, Rx ····· V_{CC} = 2.0 V more than 5 kΩ

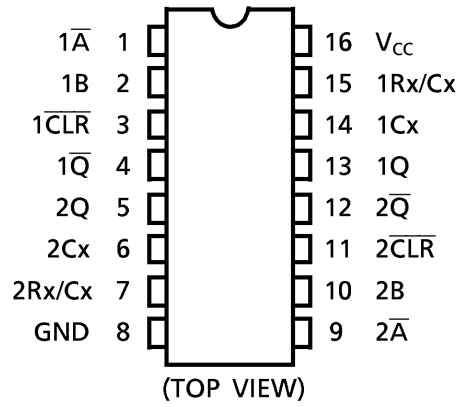
$V_{CC} \geqq$ 3.0 V more than 1 kΩ

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed····· t_{pd} = 8.1 ns (typ.) at V_{CC} = 5 V
- Low Power Dissipation
  - Standby State····· 4 μA (Max.) at Ta = 25°C
  - Active State····· 600 μA (Max.) at Ta = 25°C
- High Noise Immunity····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is equipped with all inputs.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range···· V_{CC} (opr) = 2 V~5.5 V
- Pin and Function Compatible with 74HC123A / 221A

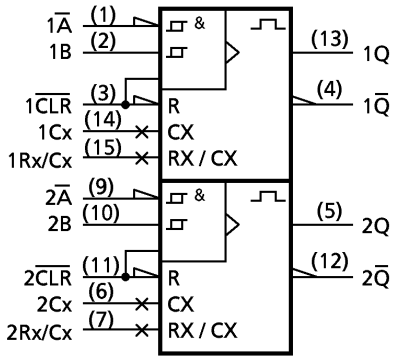
PIN ASSIGNMENT



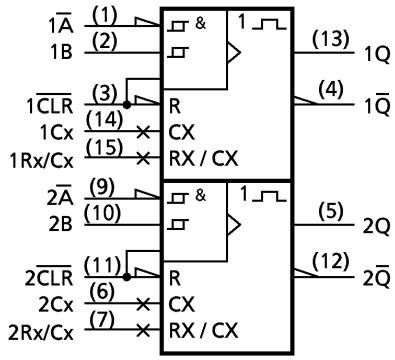
(TOP VIEW)

IEC LOGIC SYMBOL

TC74VHC123A



TC74VHC221A

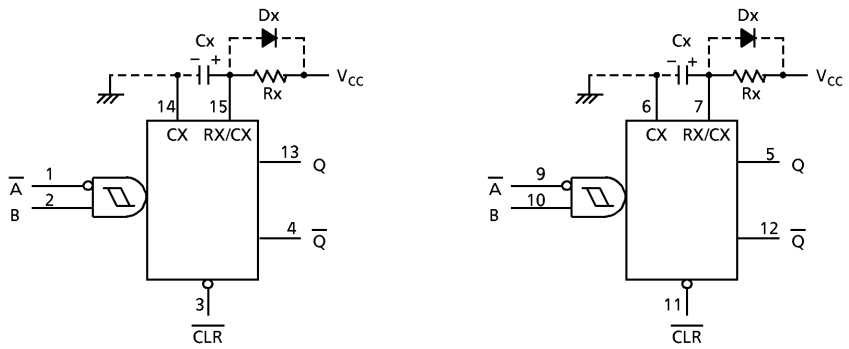


TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎍	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H	⎍	⎍	OUTPUT ENABLE
L	H	↑	⎍	⎍	OUTPUT ENABLE
X	X	L	L	H	RESET

X : Don't Care

BLOCK DIAGRAM



Notes : (1) Cx, Rx, Dx are external
Capacitor, Resistor, and Diode, respectively.

(2) External clamping diode, Dx ;

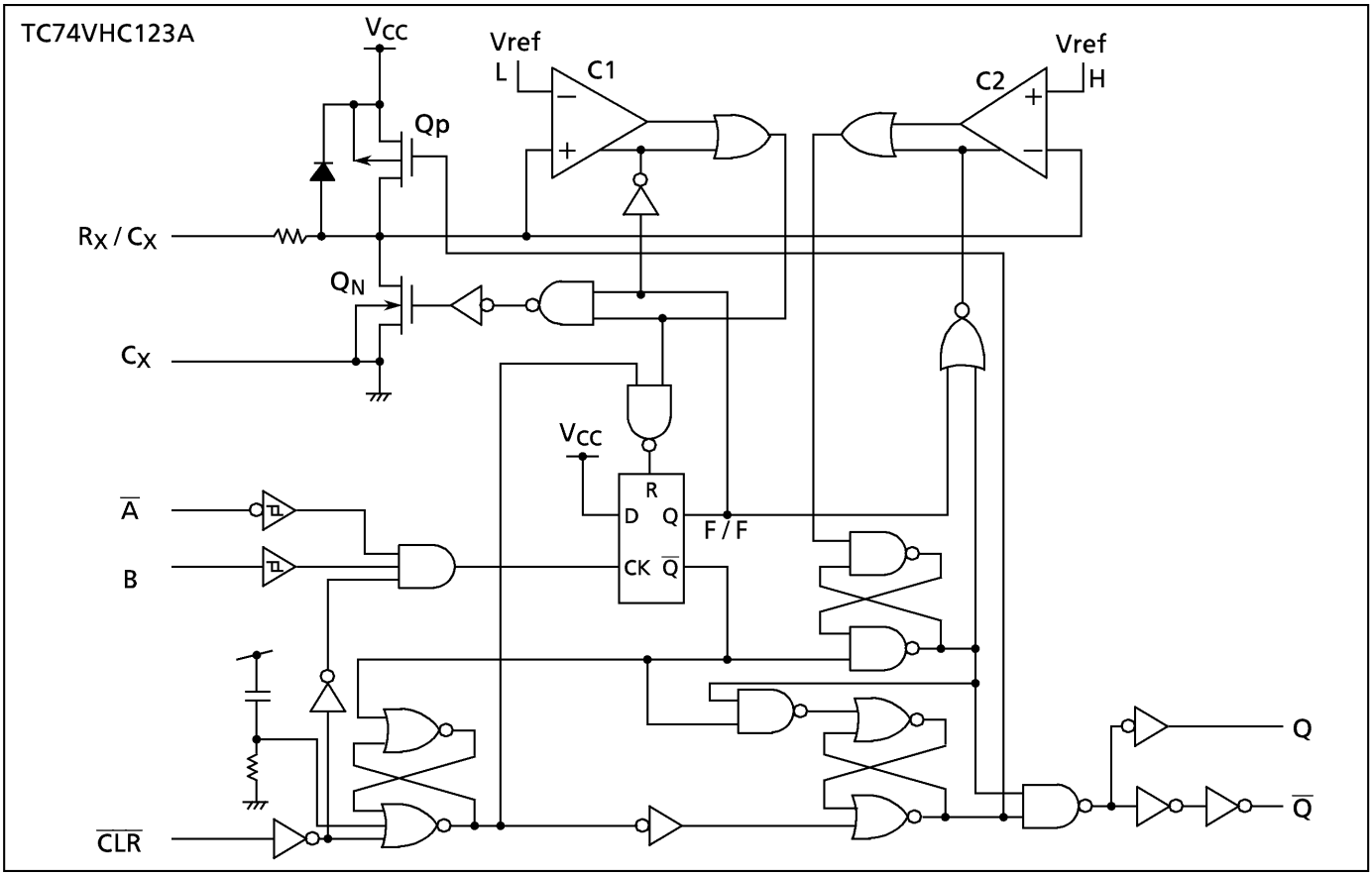
The external capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied.
If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.
The maximum value of forward current through the parasitic diode is ± 20 mA.
In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_f \geqq (V_{CC} - 0.7) \cdot Cx / 20\ mA$$

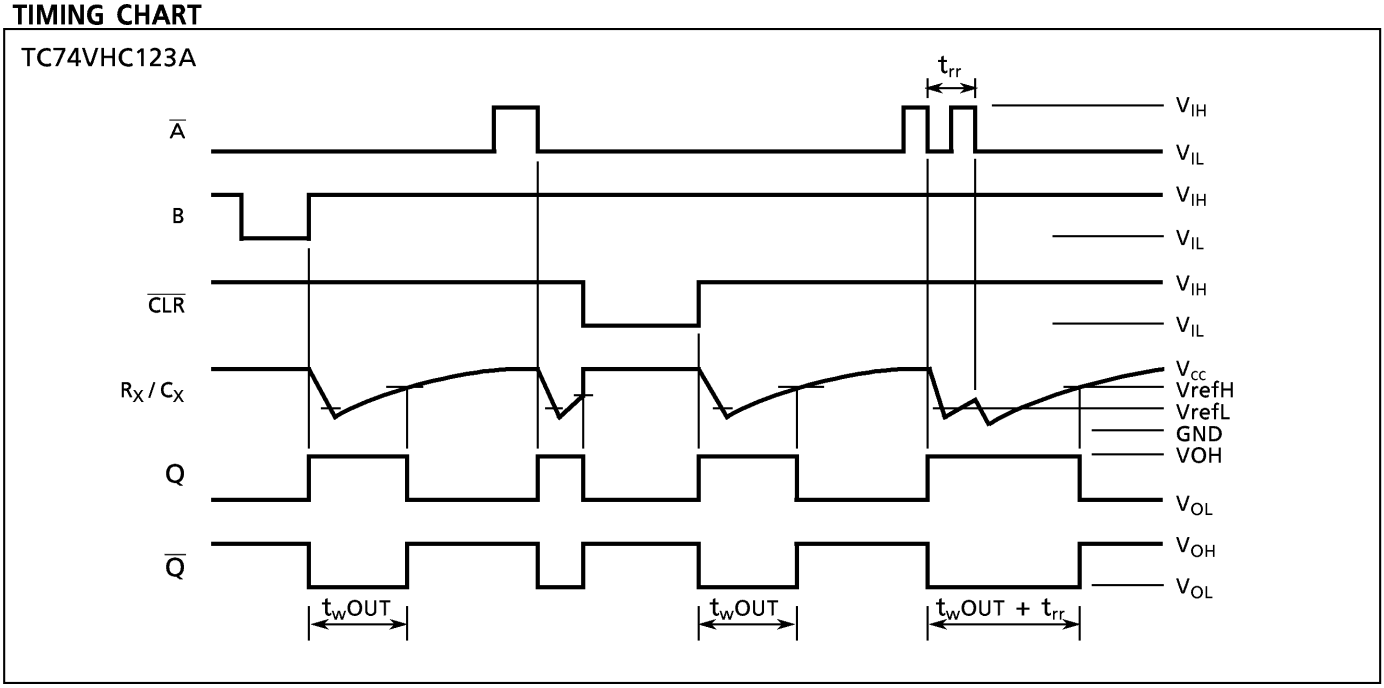
(tf is the time between the supply voltage turn off
and the supply voltage reaching 0.4 V_{CC}.)

In the even a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from rush current.

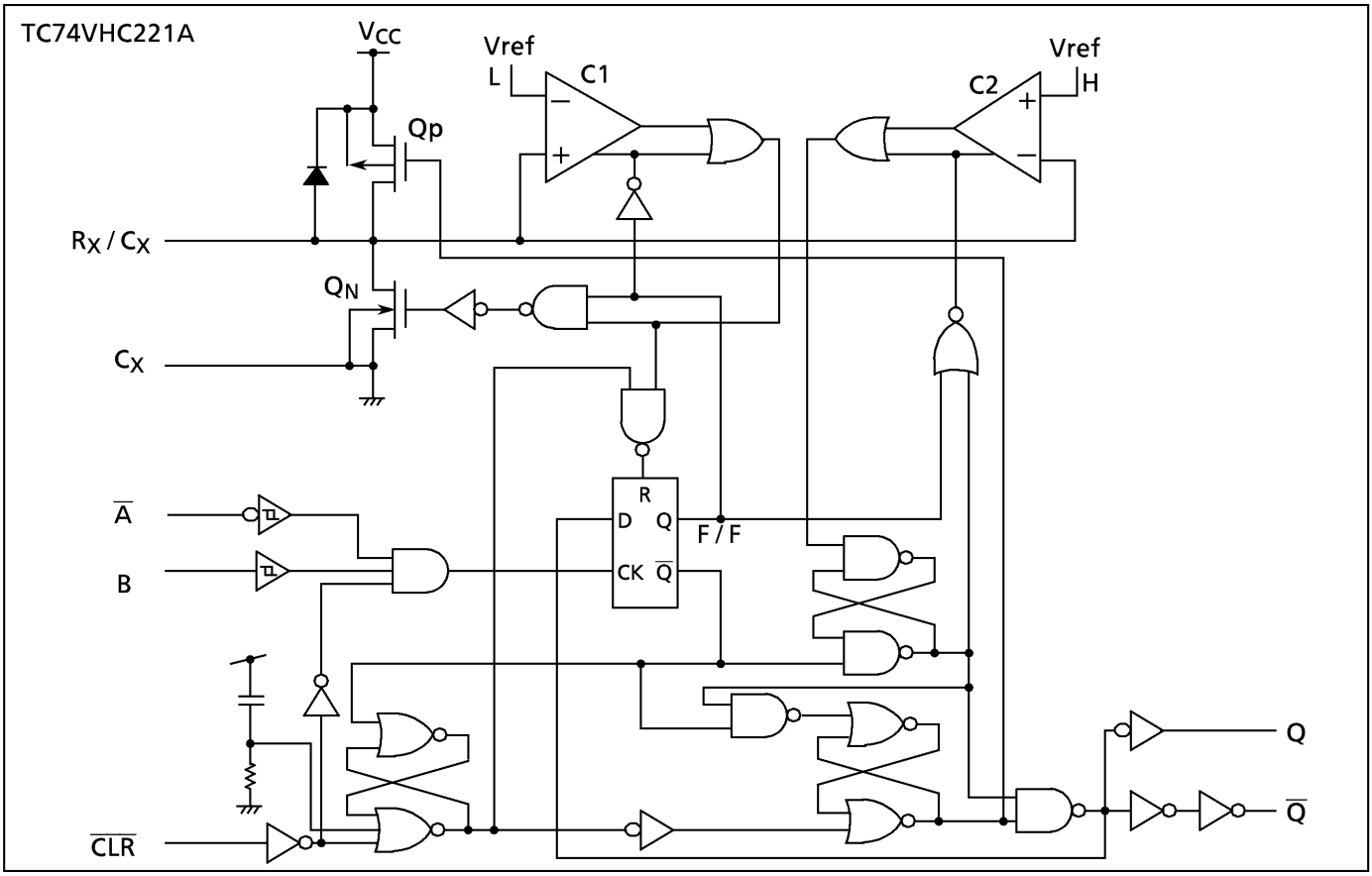
SYSTEM DIAGRAM



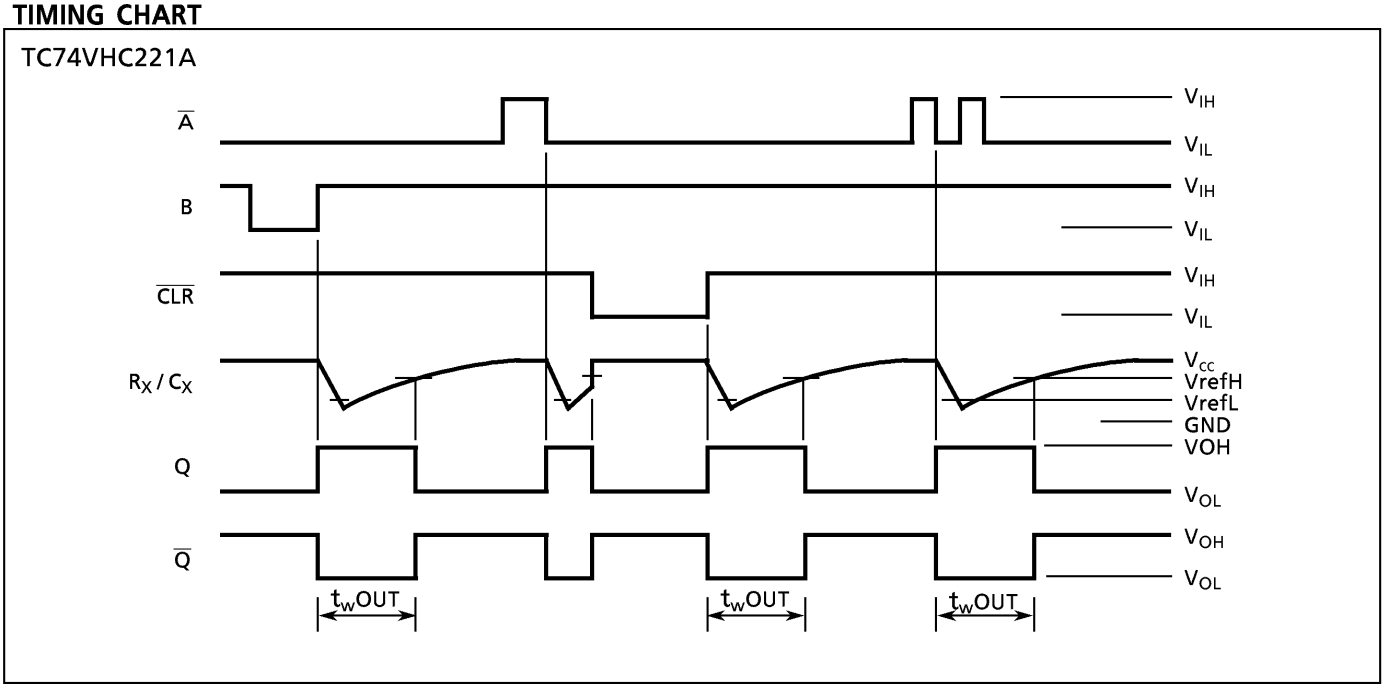
TIMING CHART



SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1)Stand-by State

The external capacitor (Cx) is fully charged to V_{CC} in the stand-by state. That means, before triggering, the Q_P and Q_N transistors which are connected to the Rx / Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2)Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal ; second, where the B input is high, and the $\overline{A}$ input has a falling signal ; and third, where the $\overline{A}$ input is low and the B input is high, and the $\overline{CLR}$ input has a rising signal.
After a trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the Rx / Cx node drops. If the Rx / Cx voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.
After Q_N turns off, the voltage at the Rx / Cx node starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.
Upon triggering, output Q becomes high, following some delay time of the internal F / F and gates. It stays high even if the voltage of Rx / Cx changes from falling to rising. When Rx / Cx reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx / Cx node reaches Vref H, the IC returns to its MONOSTABLE state.
With large values of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, tw (OUT), is as follows :

$$tw(OUT) = 1.0\,Cx\,Rx$$

(3)Retrigger operation (TC74VHC123A)

When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging Cx. The voltage level of the Rx / Cx node then falls to Vref L level again. Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx.
If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.
The minimum time for a trigger to be effective 2nd trigger, trr (Min.), depends on V_{CC} and Cx.

(4)Reset operation
In normal operation, the $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, Q_P turns on and Cx is charged rapidly to V_{CC}.
This means if $\overline{CLR}$ is set low, the IC goes into a wait state.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V_{CC} = 3.3 ± 0.3 V) 0~20 (V_{CC} = 5 ± 0.5 V)	ns / V
External Capacitor	Cx	No Limitation *	F
External Resistor	Rx	≧ 5 K * (VCC = 2.0 V) ≧ 1 K * (VCC ≧ 3.0 V)	Ω

* The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74VHC123A / 221A, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for Rx > 1 MΩ.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0	1.50	—	—	1.50	—	V
				3.0~5.5	V_{CC} × 0.7	—	—	V_{CC} × 0.7	—	
Low - Level Input Voltage	V_{IL}			2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	V_{CC} × 0.3	—	V_{CC} × 0.3	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5 V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Rx / Cx Terminal Off - State Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.5	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	
Active - State * Supply Current	I_{CC}	V_{IN} = V_{CC} or GND Rx / Cx = 0.5 V_{CC}		3.0	—	160	250	—	280	μA
				4.5	—	380	500	—	650	
				5.5	—	560	750	—	975	

* : Per circiut

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width	$t_{W(L)}$			3.3 ± 0.3	—	5.0	5.0	ns
	$t_{W(H)}$			5.0 ± 0.5	—	5.0	5.0	
Minimum Clear Width ($\overline{CLR}$)	$t_{W(L)}$			3.3 ± 0.3	—	5.0	5.0	
				5.0 ± 0.5	—	5.0	5.0	
Minimum Retrigger Time **	t_{rr}	Rx = 1 kΩ Cx = 100 pF		3.3 ± 0.3	60	—	—	
				5.0 ± 0.5	39	—	—	
		Rx = 1 kΩ Cx = 0.01 μF		3.3 ± 0.3	1.5	—	—	μs
				5.0 ± 0.5	1.2	—	—	

** : for TC74VHC123A only

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

PARAMETER	SYM-BOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A , B – Q , $\overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	–	13.4	20.6	1.0	24.0	ns
				50	–	15.9	24.1	1.0	27.5	
			5.0 ± 0.5	15	–	8.1	12.0	1.0	14.0	
				50	–	9.6	14.0	1.0	16.0	
Propagation Delay Time ($\overline{CLR}$ trigger – Q , $\overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	–	14.5	22.4	1.0	26.0	
				50	–	17.0	25.9	1.0	29.5	
			5.0 ± 0.5	15	–	8.7	12.9	1.0	15.0	
				50	–	10.2	14.9	1.0	17.0	
Propagation Delay Time ($\overline{CLR}$ – Q , $\overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	–	10.3	15.8	1.0	18.5	
				50	–	12.8	19.3	1.0	22.0	
			5.0 ± 0.5	15	–	6.3	9.4	1.0	11.0	
				50	–	7.8	11.4	1.0	13.0	
Output Pulse Width	t_{wOUT}	Cx = 28 pF	3.3 ± 0.3	50	–	160	240	–	300	
		Rx = 2 kΩ	5.0 ± 0.5		–	133	200	–	240	
		Cx = 0.01 μF	3.3 ± 0.3	50	90	100	110	90	110	μs
		Rx = 10 kΩ	5.0 ± 0.5		90	100	110	90	110	
		Cx = 0.1 μF	3.3 ± 0.3	50	0.9	1.0	1.1	0.9	1.1	ms
		Rx = 10 kΩ	5.0 ± 0.5		0.9	1.0	1.1	0.9	1.1	
Output Pulse Width Error Between Circuits (In same Package)	$\triangle t_{wOUT}$				–	± 1	–	–	–	%
Input Capacitance	C_{IN}					4	10	–	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			–	73	–	–	–	

(Note 1) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

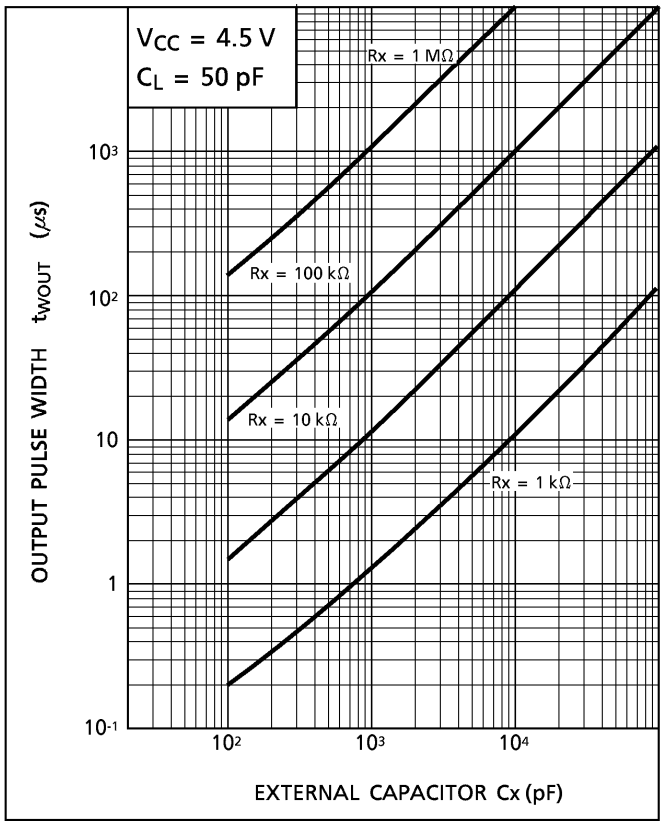
Average operating current can be obtained by the equation :

I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot$ Duty / 100 + I_{CC} / 2 (per circuit)

(I_{CC}' : Active Supply Current)

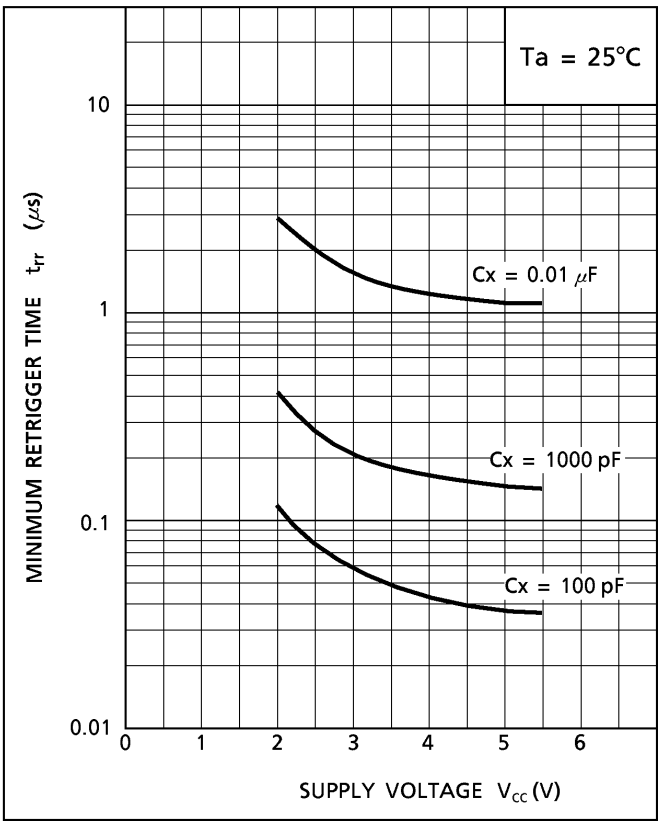
(Duty : %)

t_{WOUT}-C_X CHARACTERISTICS (typ.)

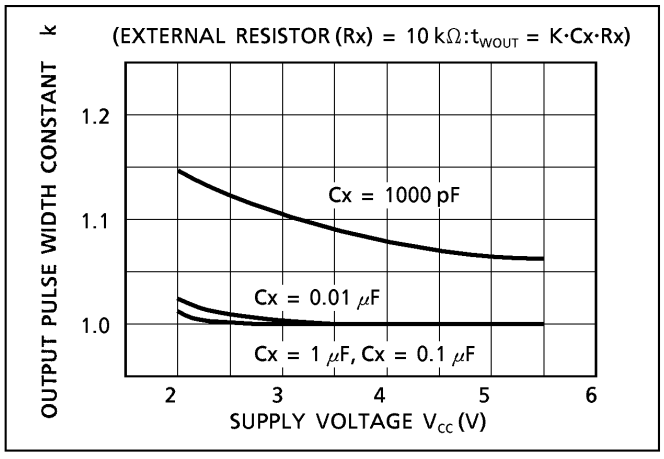


t_{rr}-V_{CC} CHARACTERISTICS (TYP.)

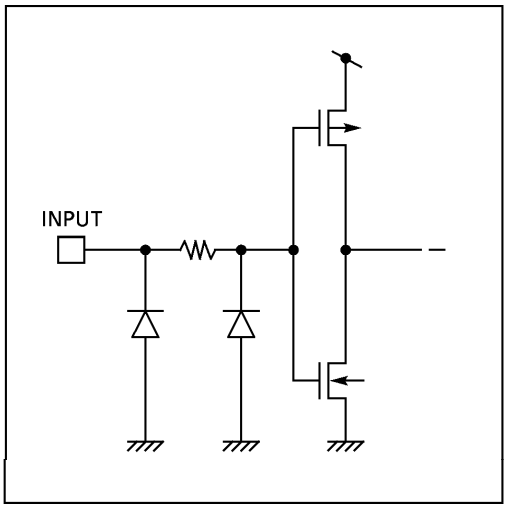
(TC74VHC123A)



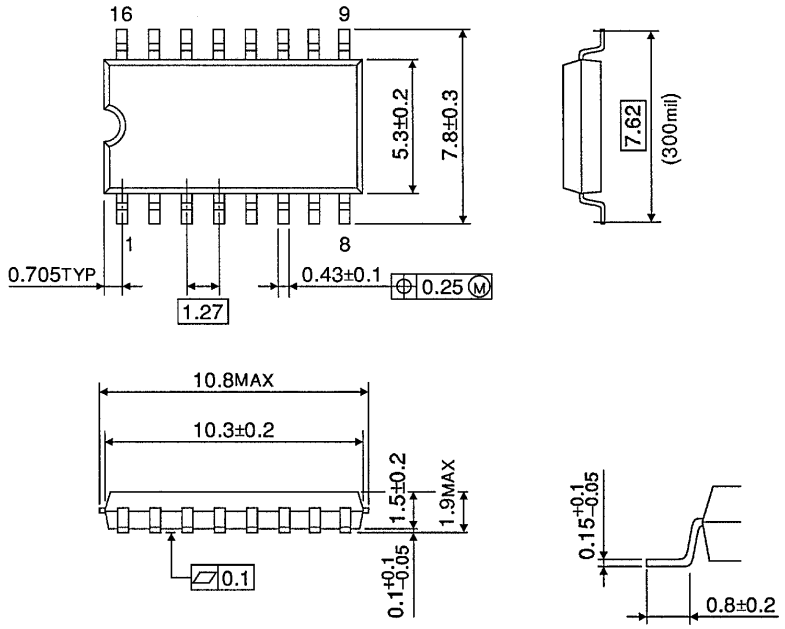
OUTPUT PULSE WIDTH CONSTANT K-SUPPLY VOLTAGE (TYPICAL)



INPUT EQUIVALENT CIRCUIT



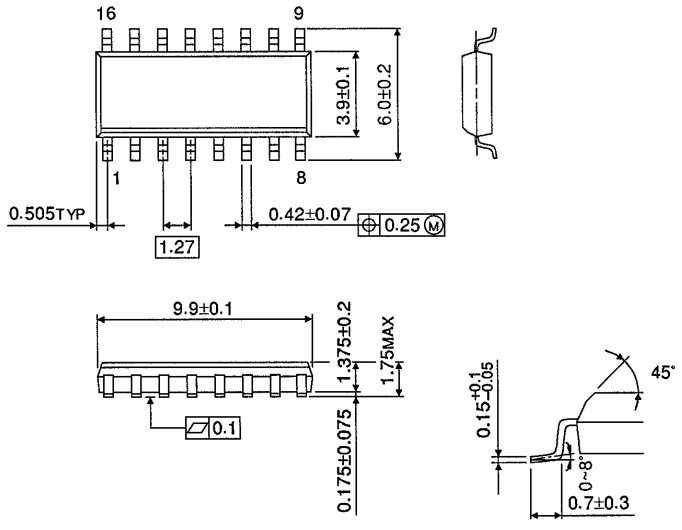
SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27) Unit in mm



Weight : 0.18 g (Typ.)

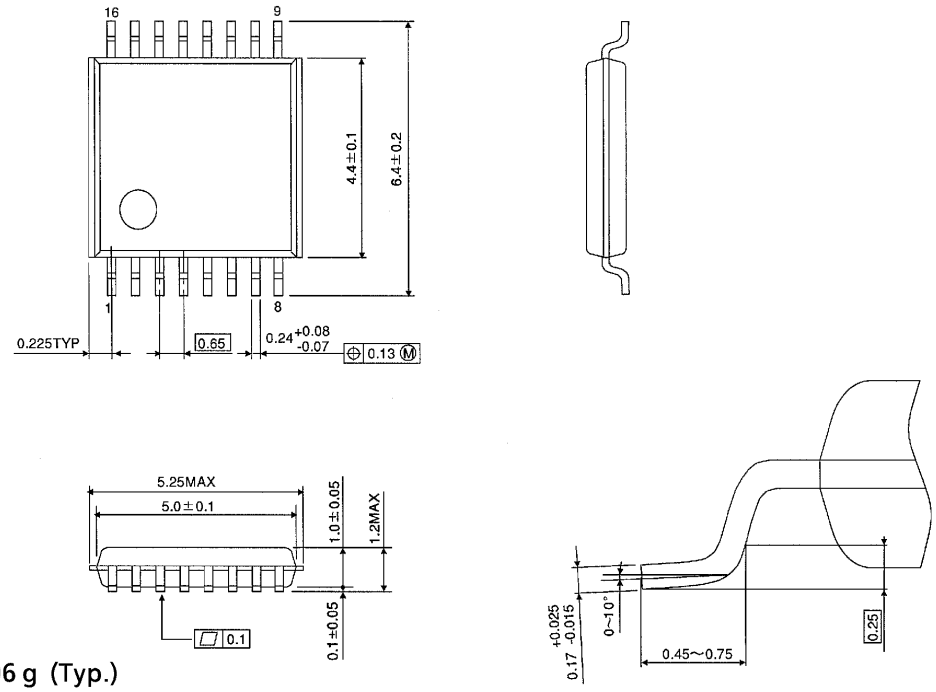
SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150-1.27) Unit in mm

(Note) : This package is not available in Japan.



Weight : 0.13 g (Typ.)

TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65) Unit in mm



Weight : 0.06 g (Typ.)

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000707EBA

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