TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT   SILICON MONOLITHIC

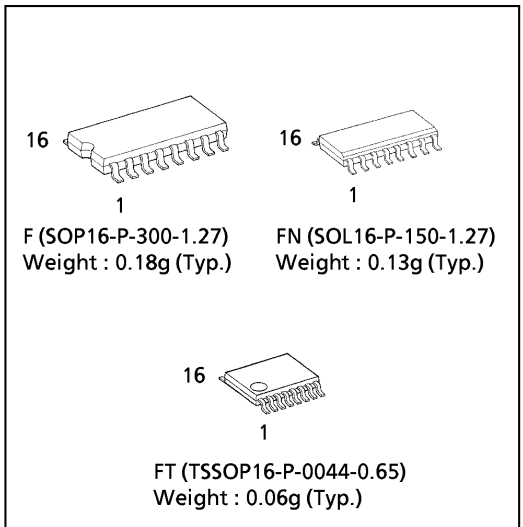# TC74VHC138F, TC74VHC138FN, TC74VHC138FT

3 - TO - 8 LINE DECODER

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74VHC138 is an advanced high speed CMOS 3 - to - 8 DECODER fabricated with silicon gate C^{2}MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ($\overline{Y}0$ - $\overline{Y}7$) will go low.

When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high. G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems. An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.
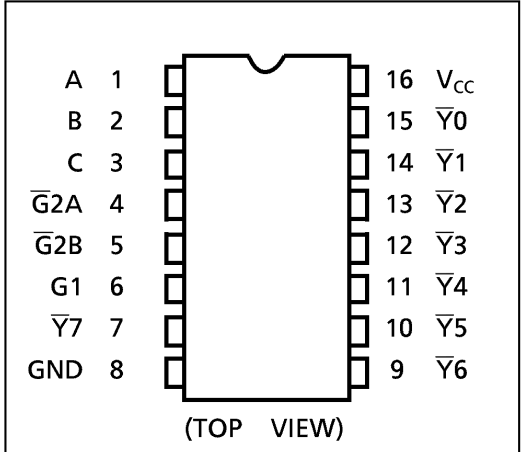
FEATURES :
- High Speed⋯⋯⋯⋯⋯⋯⋯⋯⋯$t_{pd} = 5.7$ns(typ.) at $V_{CC} = 5$V
- Low Power Dissipation⋯⋯⋯⋯⋯$I_{CC} = 4\mu$A(Max.) at Ta = 25°C
- High Noise Immunity⋯⋯⋯⋯⋯⋯$V_{NIH} = V_{NIL} = 28\%$ V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays⋯⋯$t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range⋯⋯V_{CC} (opr) = 2V ~ 5.5V
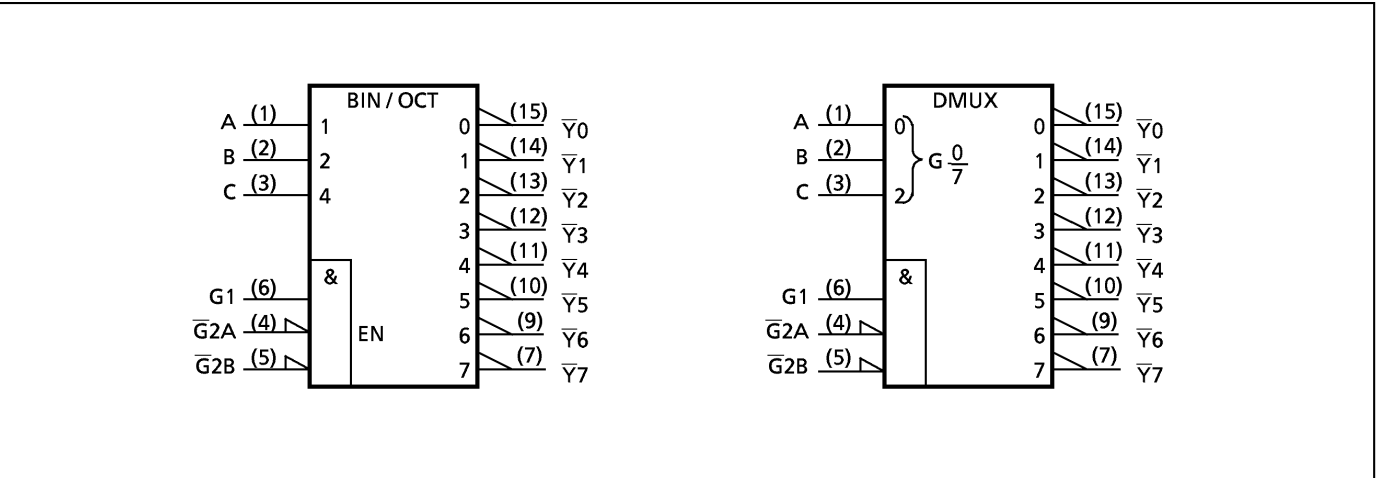- Pin and Function Compatible with 74ALS138

F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

FT (TSSOP16-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT

A	1	16	V_{CC}
B	2	15	$\overline{Y}0$
C	3	14	$\overline{Y}1$
$\overline{G}2A$	4	13	$\overline{Y}2$
$\overline{G}2B$	5	12	$\overline{Y}3$
G1	6	11	$\overline{Y}4$
$\overline{Y}7$	7	10	$\overline{Y}5$
GND	8	9	$\overline{Y}6$

(TOP   VIEW)

IEC LOGIC SYMBOL

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT			$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : Don't Care

LOGIC DIAGRAM
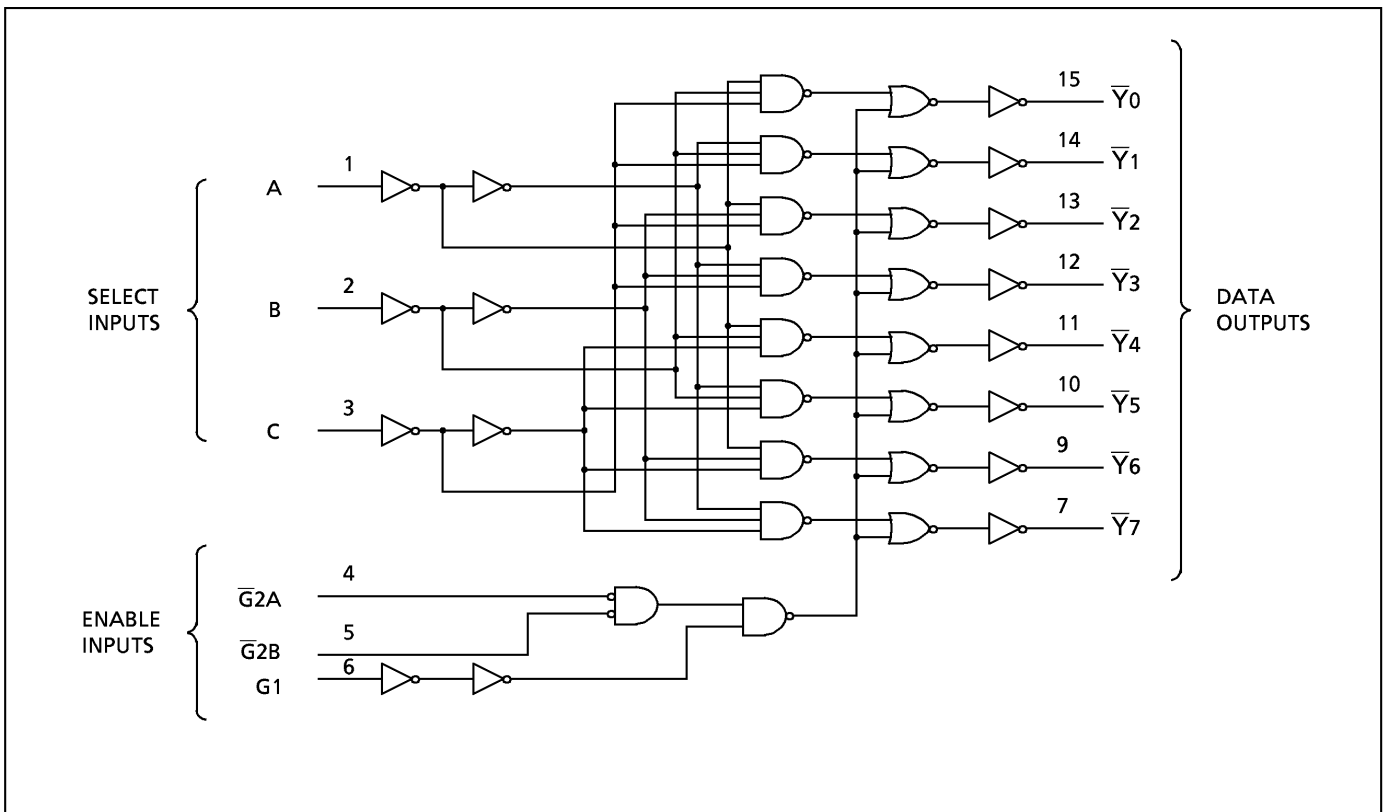
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim 5.5$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	dt / dv	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3$V) $0 \sim 20$ ($V_{CC} = 5 \pm 0.5$V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = $-40 \sim 85$°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0	1.50	—	—	1.50	—	V
				3.0~5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—	
Low - Level Input Voltage	V_{IL}			2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$	
High - Level Output Voltage	V_{OH}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OH} = -50\mu A$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4mA$	3.0	2.58	—	—	2.48	—	
			$I_{OH} = -8mA$	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OL} = 50\mu A$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 4mA$	3.0	—	—	0.36	—	0.44	
			$I_{OL} = 8mA$	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	$V_{IN} = 5.5$V or GND		0~5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

| PARAMETER | SYMBOL | TEST CONDITION | | Ta = 25°C | | | Ta = −40~85°C | | UNIT |
		V_{CC}(V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B, C - $\overline{Y}$)	t_{pLH} t_{pHL}	3.3 ± 0.3	15	—	8.2	11.4	1.0	13.5	ns
			50	—	10.0	15.8	1.0	18.0	
		5.0 ± 0.5	15	—	5.7	8.1	1.0	9.5	
			50	—	7.2	10.1	1.0	11.5	
Propagation Delay Time (G 1 - $\overline{Y}$)	t_{pLH} t_{pHL}	3.3 ± 0.3	15	—	8.1	12.8	1.0	15.0	
			50	—	10.6	16.3	1.0	18.5	
		5.0 ± 0.5	15	—	5.6	8.1	1.0	9.5	
			50	—	7.1	10.1	1.0	11.5	
Propagation Delay Time ($\overline{G}$ 2 - $\overline{Y}$)	t_{pLH} t_{pHL}	3.3 ± 0.3	15	—	8.2	11.4	1.0	13.5	
			50	—	10.7	14.9	1.0	17.0	
		5.0 ± 0.5	15	—	5.8	8.1	1.0	9.5	
			50	—	7.3	10.1	1.0	11.5	
Input Capacitance	C_{IN}			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)		—	34	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
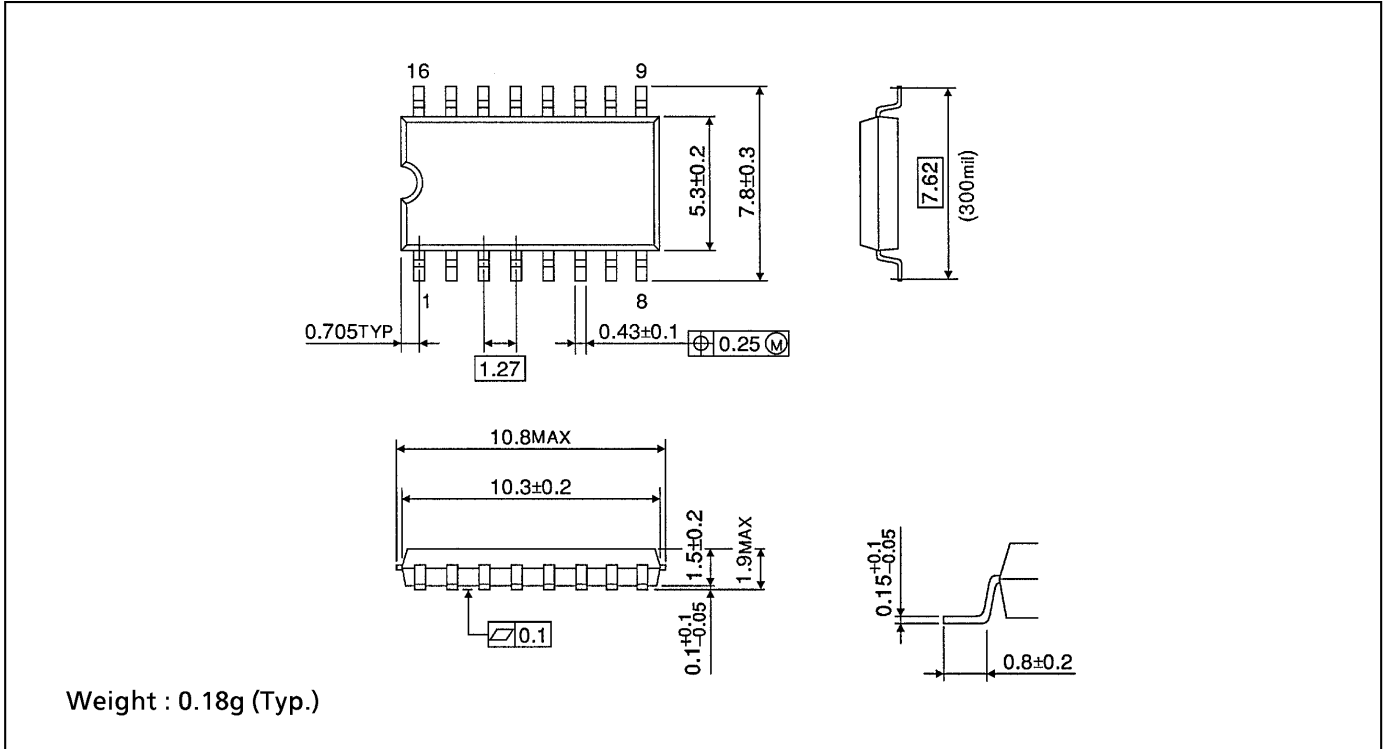Average operating current can be obtained by the equation :

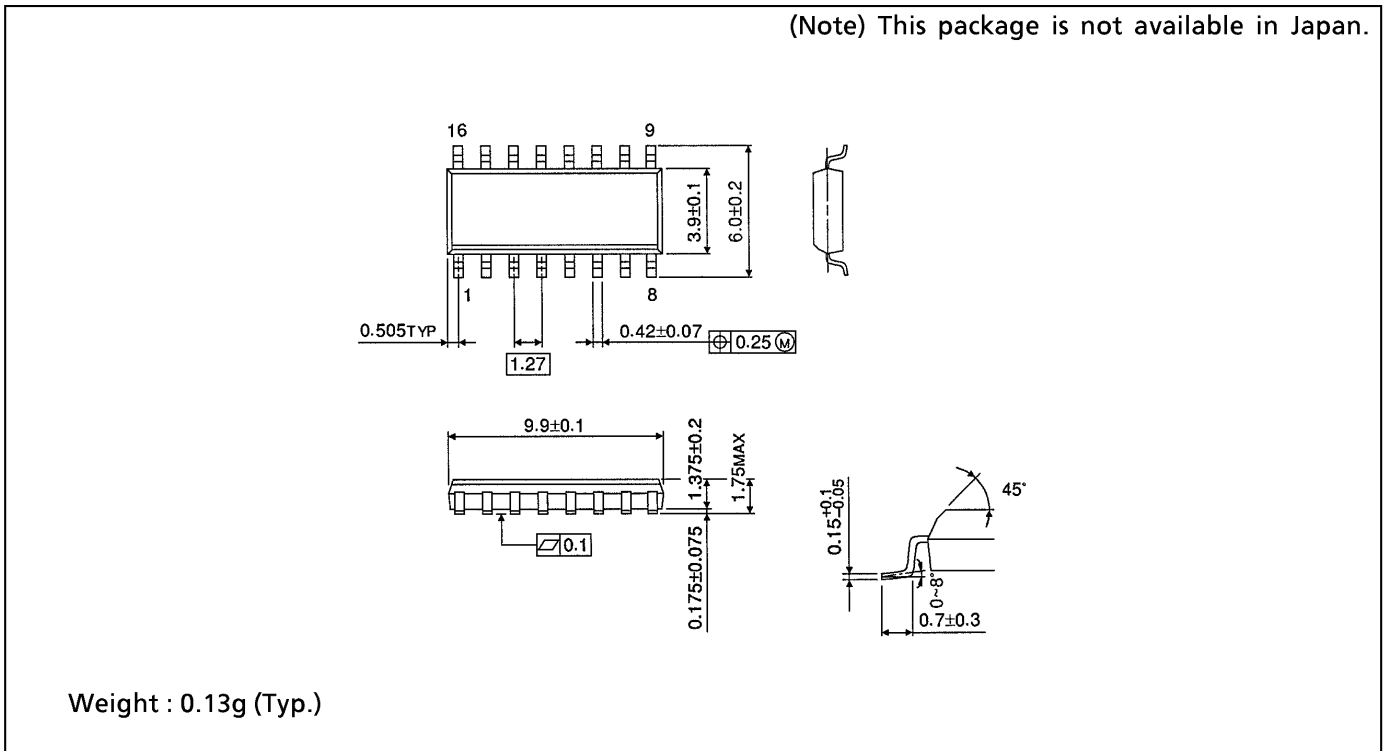$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

INPUT EQUIVALENT CIRCUIT
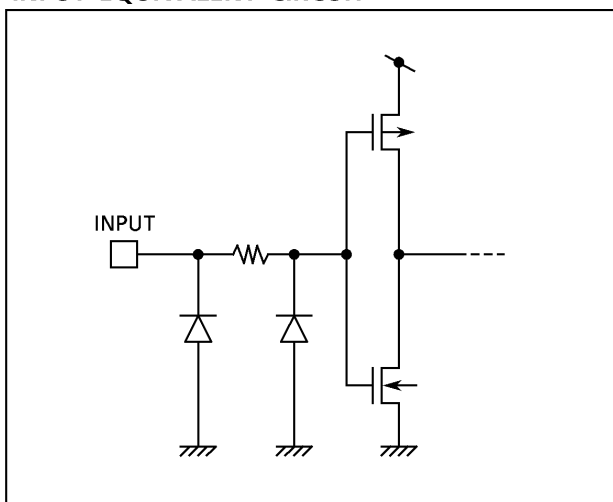
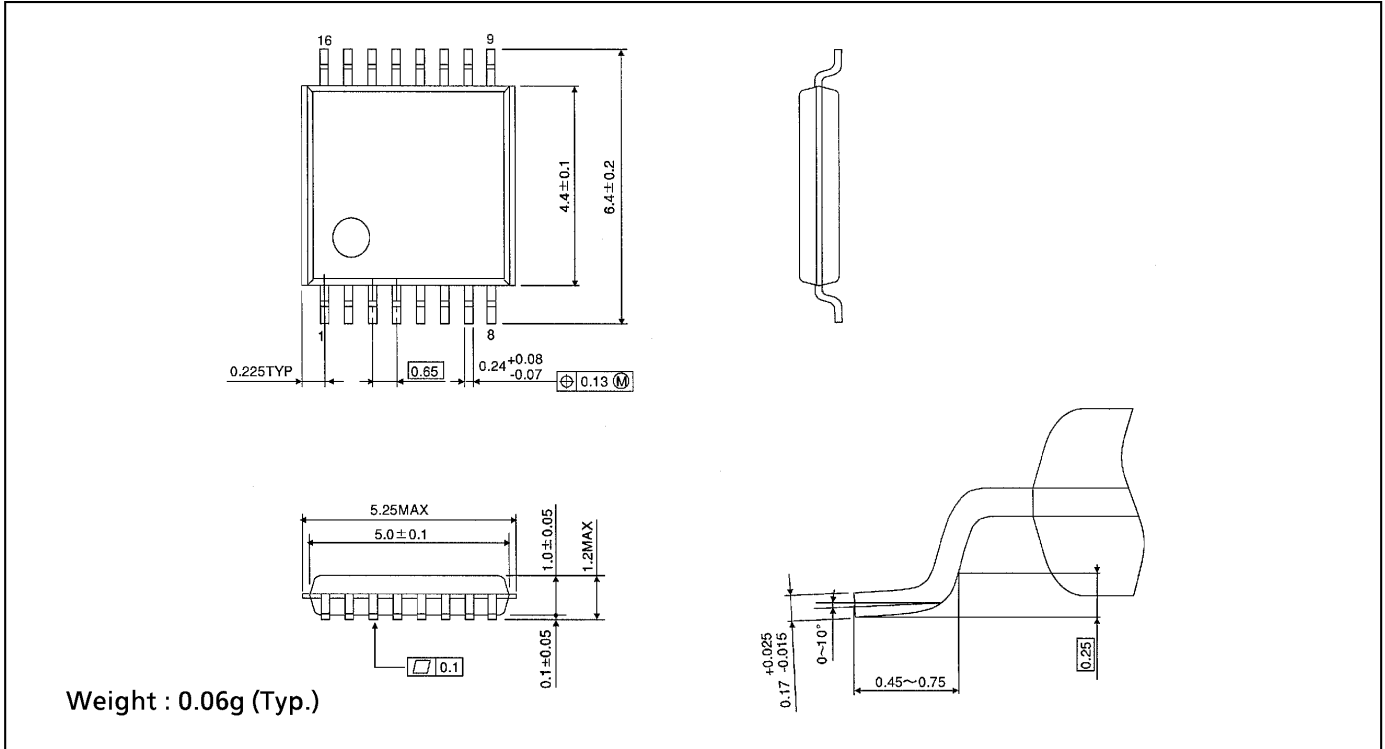**SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)**   Unit in mm

Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150-1.27)   Unit in mm

(Note) This package is not available in Japan.

Weight : 0.13g (Typ.)

TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65) Unit in mm

Weight : 0.06g (Typ.)

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000707EBA

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