

TC74VHC245F, TC74VHC245FW, TC74VHC245FT

OCTAL BUS TRANSCEIVER

The TC74VHC245 is an advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two - way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

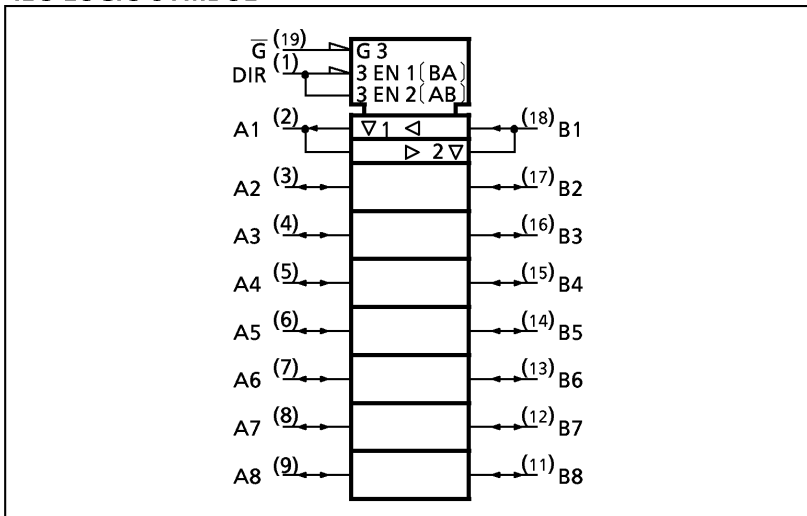
The enable input (\bar{G}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

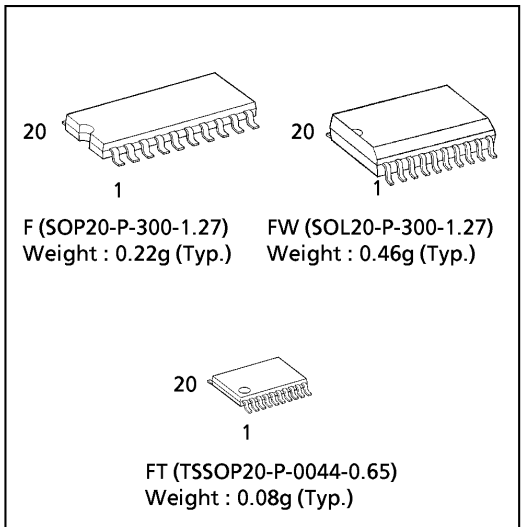
FEATURES:

- High Speed..... $t_{pd} = 4.0ns(typ.)$ at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A(Max.)$ at $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (Min.)$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (opr) = 2V \sim 5.5V$
- Low Noise $V_{OLP} = 1.2V (Max.)$
- Pin and Function Compatible with 74ALS245

IEC LOGIC SYMBOL



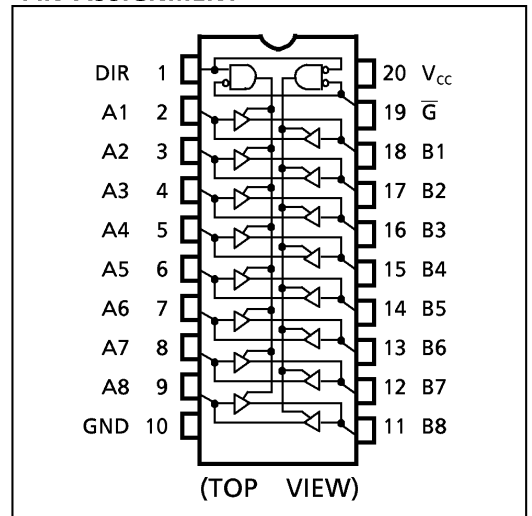
(Note) The JEDEC SOP (FW) is not available in Japan.



APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.
- 3) A parasitic diode is formed between the bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

PIN ASSIGNMENT



TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
\bar{G}	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

X : Don't Care

Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage (DIR, \bar{G})	V_{IN}	-0.5~7.0	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage (DIR, \bar{G})	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/O}$	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt / dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		2.0 3.0~ 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	—	V	
Low - Level Input Voltage	V _{IL}		2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V	
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			I _{OH} = -4mA I _{OH} = -8mA	4.5	4.4	4.5	—	4.4	—	
				3.0	2.58	—	—	2.48	—	
			I _{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			I _{OL} = 4mA I _{OL} = 8mA	4.5	—	0.0	0.1	—	0.1	
				3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	± 0.25	—	± 2.50	μA	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND	0~5.5	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0		

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	CL (pF)	Ta = 25°C			Ta = -40~85°C		UNIT	
					MIN.	TYP.	MAX.	MIN.	MAX.		
Propagation Delay Time	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	5.8	8.4	1.0	10.0	ns	
				50	—	8.3	11.9	1.0	13.5		
				5.0 ± 0.5	15	—	4.0	5.5	1.0		6.5
					50	—	5.5	7.5	1.0		8.5
3-State Output Enable Time	t _{pZL} t _{pZH}	RL = 1kΩ	3.3 ± 0.3	15	—	8.5	13.2	1.0	15.5	ns	
				50	—	11.0	16.7	1.0	19.0		
				5.0 ± 0.5	15	—	5.8	8.5	1.0		10.0
					50	—	7.3	10.6	1.0		12.0
3-State Output Disable Time	t _{pLZ} t _{pHZ}	RL = 1kΩ	3.3 ± 0.3	50	—	11.5	15.8	1.0	18.0	ns	
				5.0 ± 0.5	50	—	7.0	9.7	1.0		11.0
Output to Output Skew	t _{osLH} t _{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns	
				5.0 ± 0.5	50	—	—	1.0	—		1.0
Input Capacitance	C _{IN}	DIR, \bar{G}			—	4	10	—	10	pF	
Bus Input Capacitance	C _{I/O}	An, Bn			—	8	—	—	—		
Power Dissipation Capacitance	C _{PD}	(Note 2)			—	21	—	—	—		

Note (1) Parameter guaranteed by design. t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

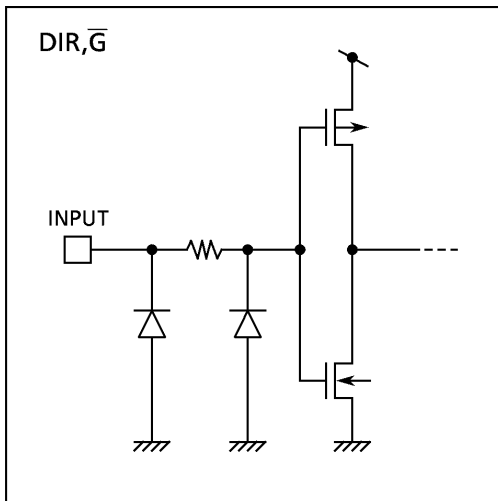
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

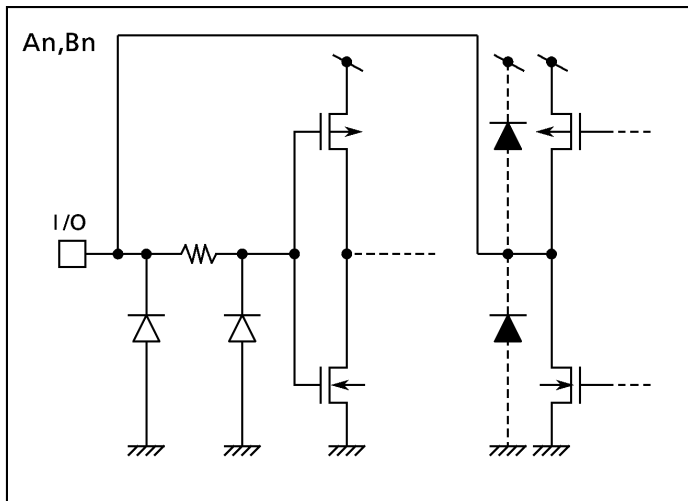
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT	
			V _{CC} (V)	TYP.		MAX.
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.7 (0.9)	1.0 (1.2)	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.7 (-0.9)	-1.0 (-1.2)	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	-	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	-	1.5	V

(Note) The value in () only applies to JEDEC SOP (FW) devices.

INPUT EQUIVALENT CIRCUIT

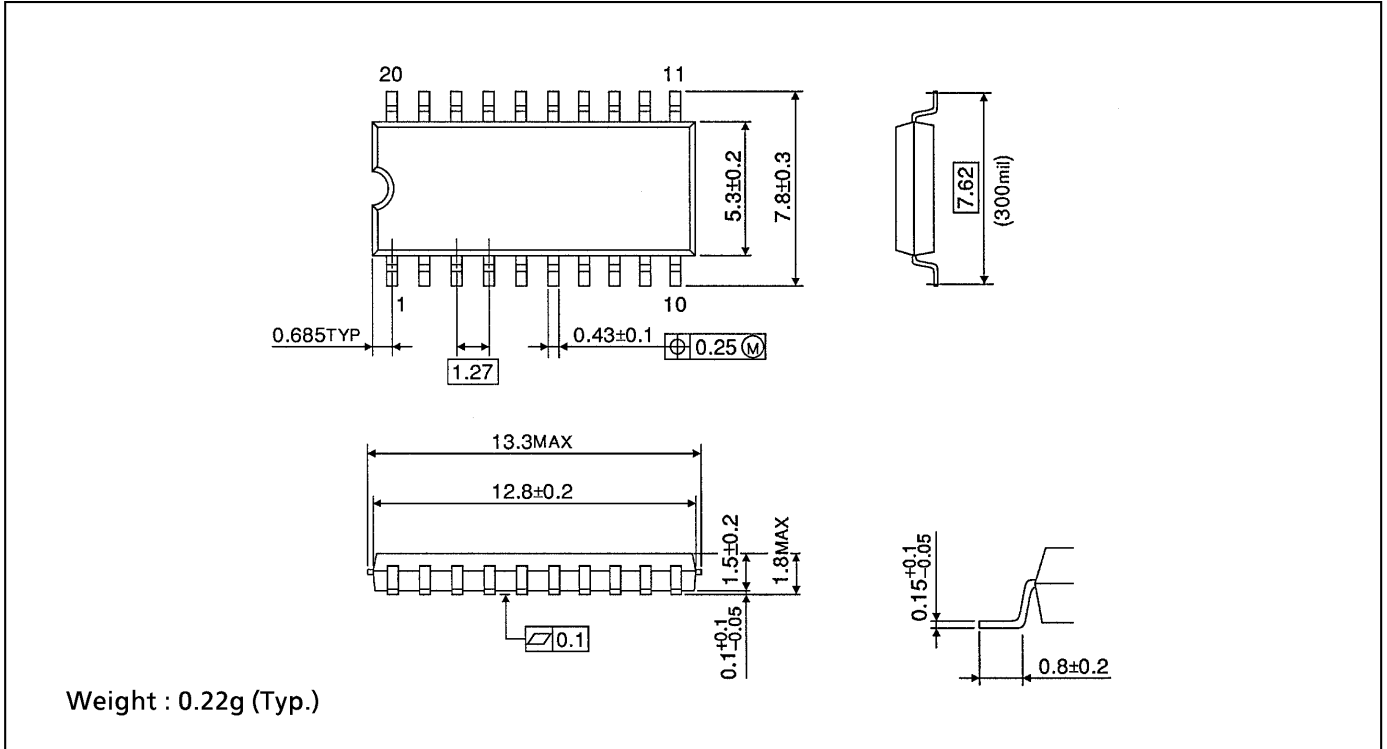


BUS TERMINAL EQUIVALENT CIRCUIT



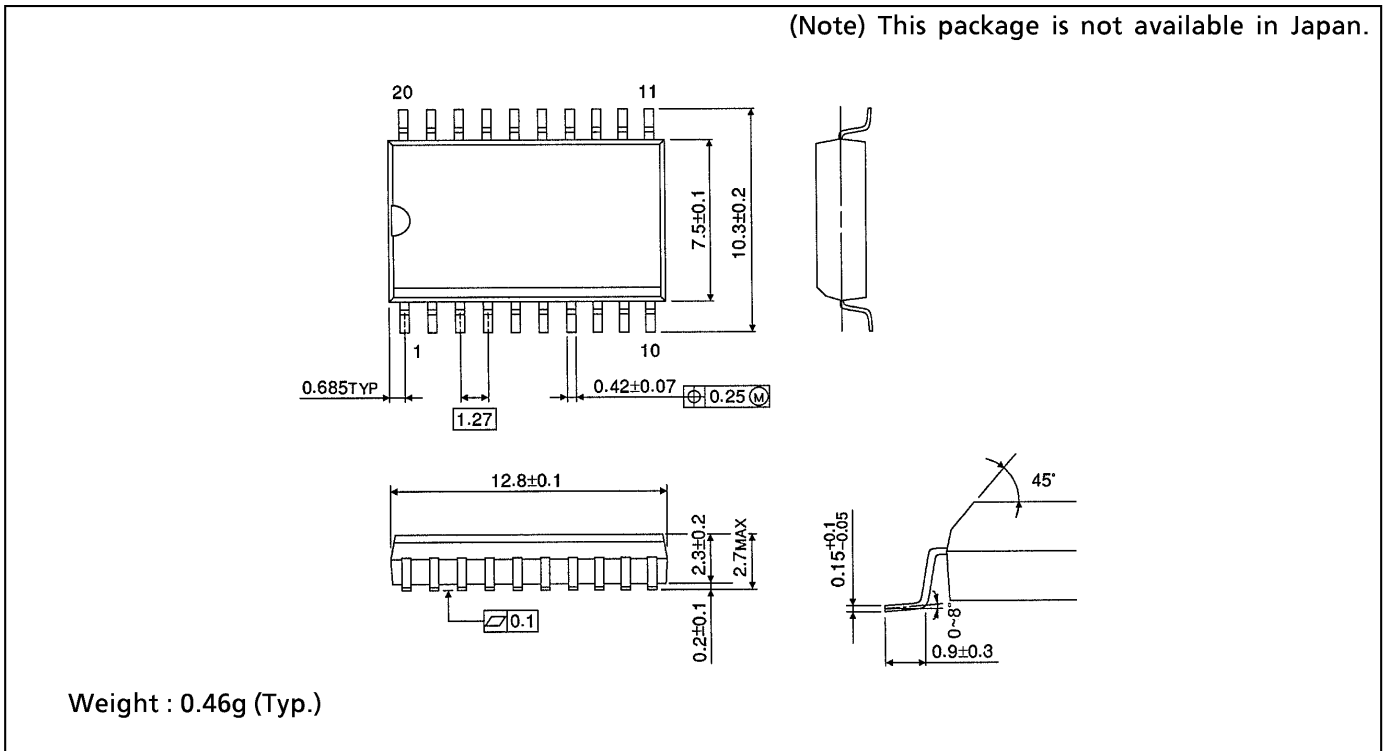
SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

Unit in mm



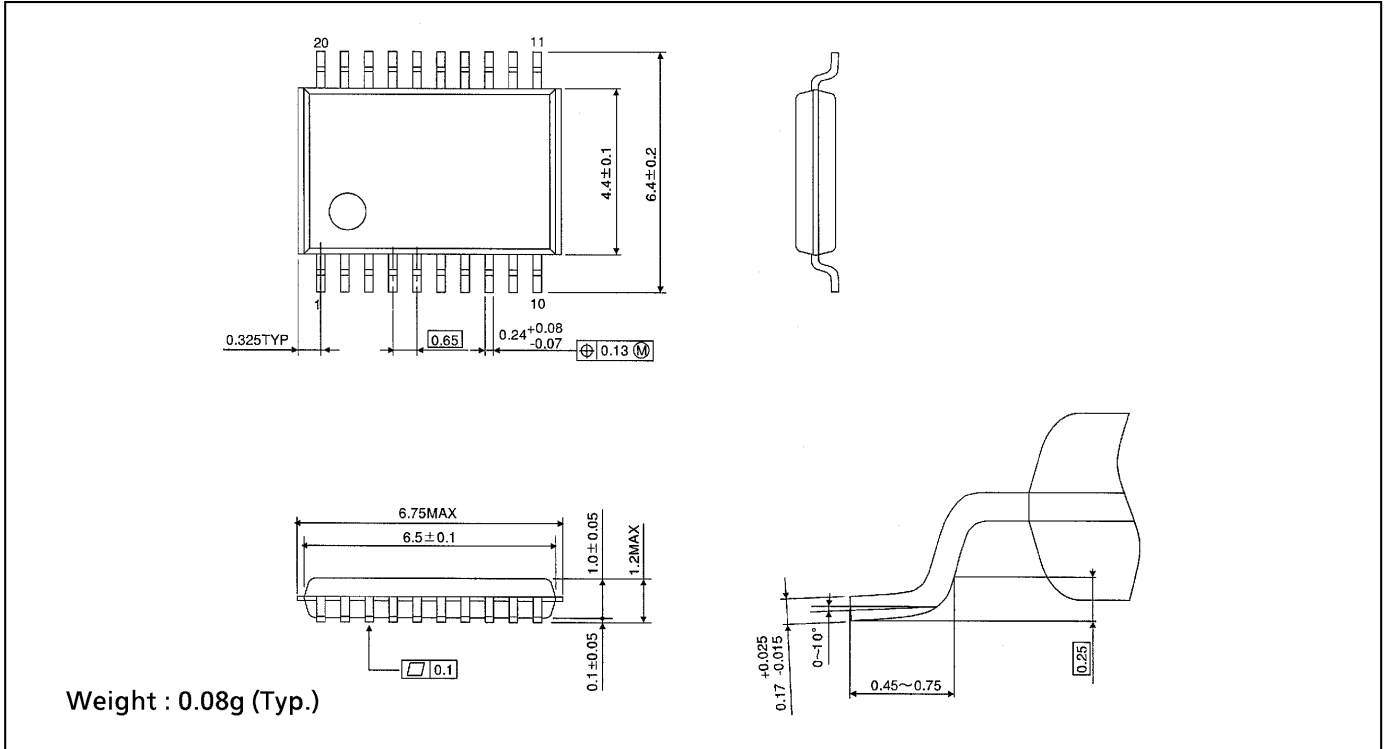
SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

Unit in mm



TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65)

Unit in mm



RESTRICTIONS ON PRODUCT USE

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