TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC299F, TC74VHC299FW, TC74VHC299FT

8 - BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74VHC299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate C^{2}MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

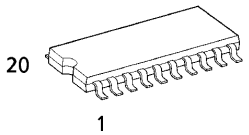
It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G}1$, $\overline{G}2$) are high, the eight I / O are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

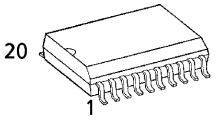
All inputs are equipped with protection circuits against static discharge.

FEATURES :

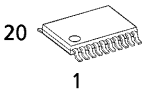
- High Speed ····· f_{MAX} = 160MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC} (opr) = 2V ~ 5.5V
- Low Noise ····· V_{OLP} = 1.4V (Max.)
- Pin and Function Compatible with 74ALS299



F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)



FW (SOL20-P-300-1.27)
Weight : 0.46g (Typ.)



FT (TSSOP20-P-0044-0.65)
Weight : 0.08g (Typ.)

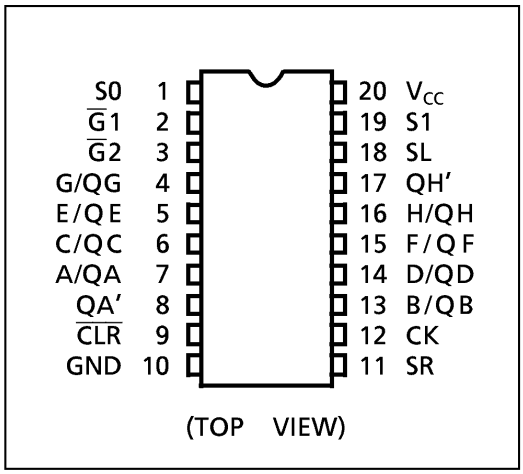
APPLICATION NOTE

1) Do not apply a signal to A / QA~H / QH bus terminal when it is in the output mode. Damage may result.

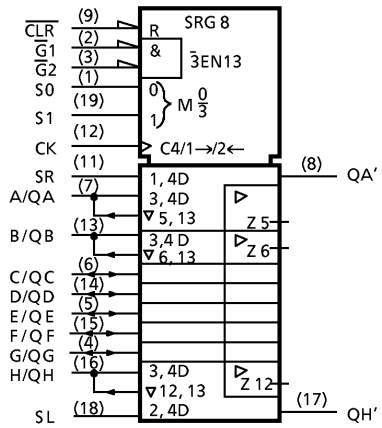
2) All floating (high impedance) A / QA~H / QH bus terminals must have their input levels fixed by means of pull up or pull down resistors.

3) A parasitic diode is formed between A / QA~H / QH bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

MODE	INPUTS								INPUTS/ OUTPUTS		OUTPUTS	
	$\overline{CLR}$	FUNCTION SELECT		OUTPUT CONTROL		CK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G}$1*	$\overline{G}$2*		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↑	X	H	H	QGn	H	QGn
	H	L	H	L	L	↑	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↑	H	X	QBn	H	QBn	H
	H	H	L	L	L	↑	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	↑	X	X	a	h	a	h

* When one or both output controls are high, the eight input / output terminals are in the high-impedance state ; however sequential or clearing of the register is not affected.

Z : High impedance

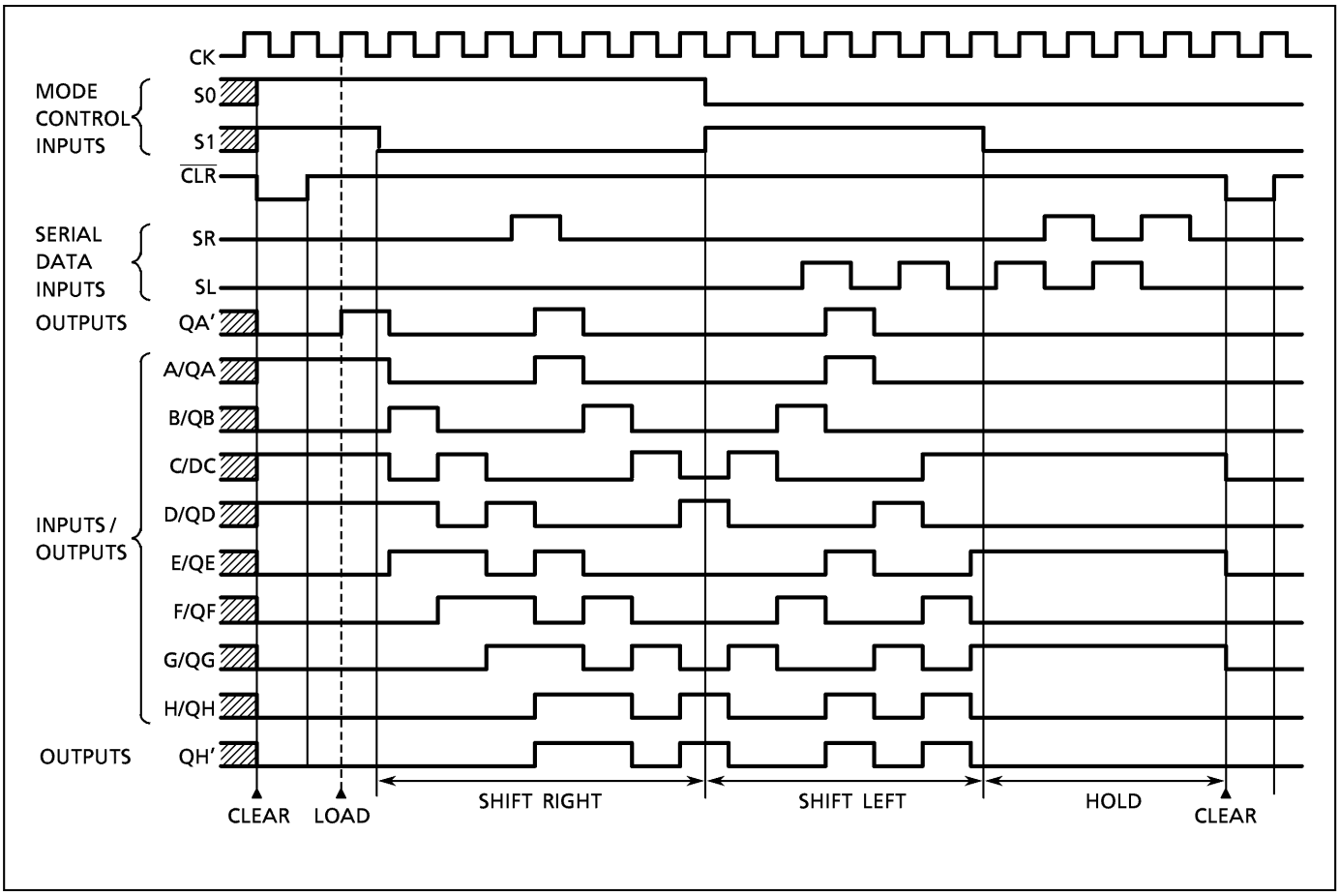
Qn0 : The level of Qn before the indicated steady-state input conditions were established.

Qnn : The level of Qn before the most recent active transition indicated by ↓ or ↑.

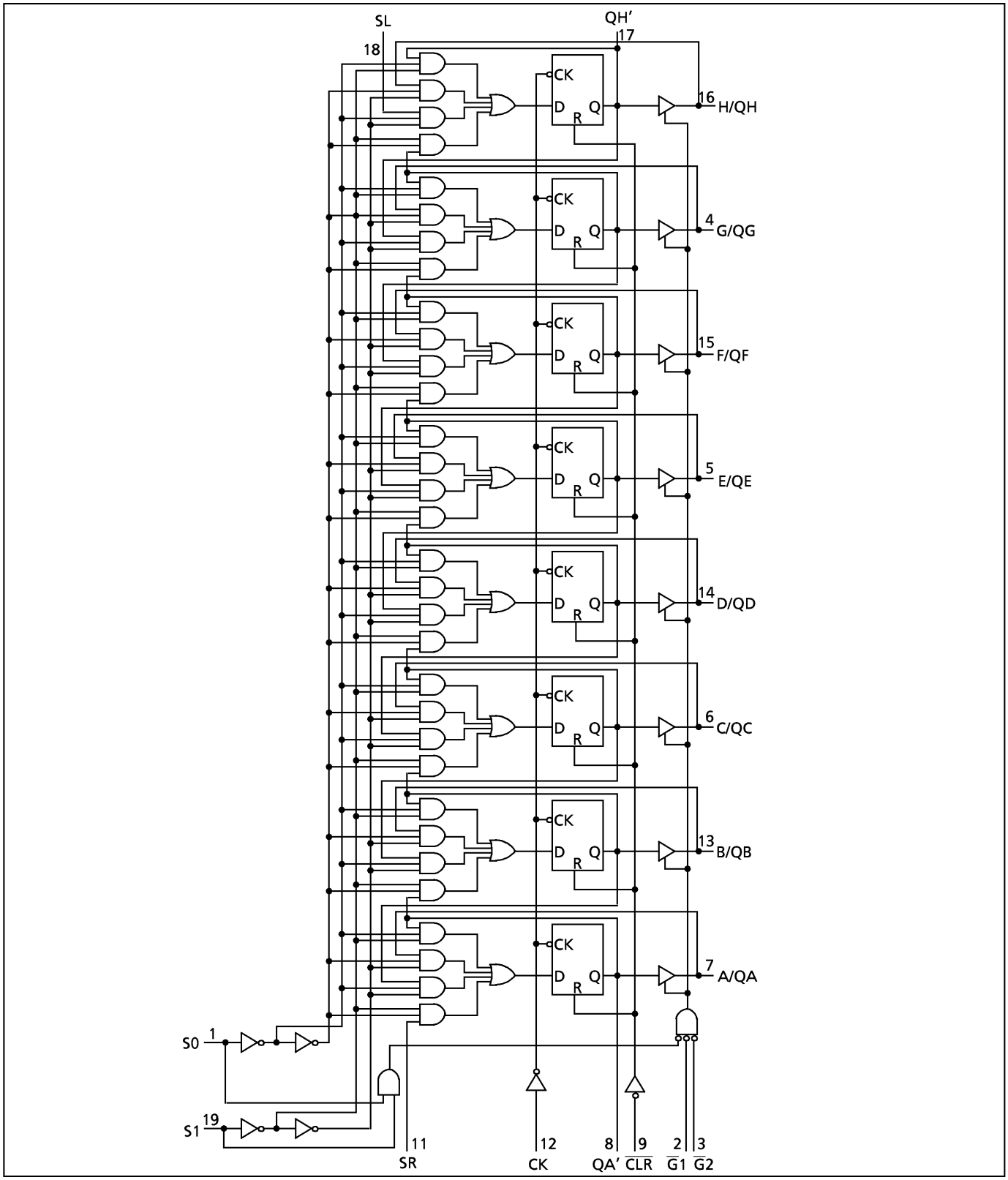
a, h : The level of the steady-state inputs A, H, respectively.

X : Don't Care.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC BUS I/O Voltage (A/QA~H/QH)	$V_{IN/OUT}$	−0.5~V_{CC}+0.5	V
DC Output Voltage (QA'~QH')	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±80	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
DC BUS I/O Voltage (A/QA~H/QH)	$V_{IN/OUT}$	0~V_{CC}	V
DC Output Voltage (QA'~QH')	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~100 (Vcc = 3.3 ± 0.3V) 0~20 (Vcc = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITON		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.50	—	—	1.50	—	V
				3.0~5.5	$V_{CC}\times0.7$	—	—	$V_{CC}\times0.7$	—	
Low-Level Input Voltage	V_{IL}			2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	$V_{CC}\times0.3$	—	$V_{CC}\times0.3$	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−QA′, QH′)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	−	12.2	17.2	1.0	19.8	ns
				50	−	14.7	20.7	1.0	23.3	
			5.0 ± 0.5	15	−	8.5	10.8	1.0	12.0	
				50	−	10.0	12.8	1.0	14.0	
Propagation Delay Time ($\overline{CLR}$−QA′, QH′)	t_{pHL}		3.3 ± 0.3	15	−	13.0	19.0	1.0	22.0	
				50	−	15.5	22.5	1.0	25.5	
			5.0 ± 0.5	15	−	9.1	11.2	1.0	13.5	
				50	−	10.8	13.2	1.0	15.5	
Propagation Delay Time (CK−QA~QH)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	−	10.3	14.3	1.0	16.6	
				50	−	12.8	17.8	1.0	20.1	
			5.0 ± 0.5	15	−	7.3	9.1	1.0	10.4	
				50	−	8.8	11.1	1.0	12.4	
Propagation Delay Time ($\overline{CLR}$−QA~QH)	t_{pHL}		3.3 ± 0.3	15	−	10.8	17.0	1.0	19.5	
				50	−	13.3	20.5	1.0	23.0	
			5.0 ± 0.5	15	−	7.7	10.5	1.0	12.0	
				50	−	9.2	12.5	1.0	14.0	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	3.3 ± 0.3	15	−	13.3	16.5	1.0	19.2	
				50	−	14.8	19.0	1.0	21.7	
			5.0 ± 0.5	15	−	8.9	9.7	1.0	11.3	
				50	−	10.4	11.2	1.0	12.6	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	3.3 ± 0.3	50	−	18.0	21.3	1.0	24.3	
			5.0 ± 0.5	50	−	11.8	13.2	1.0	15.0	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3	15	65	100	−	55	−	MHz
				50	55	90	−	50	−	
			5.0 ± 0.5	15	125	160	−	110	−	
				50	115	150	−	100	−	
Input Capacitance	C_{IN}				−	4	10	−	−	pF
BUS I/O Capacitance (A/QA~H/QH)	C_{OUT}				−	8	−	−	−	
Power Dissipation Capacitance	C_{PD}	(Note 1)			−	110	−	−	−	

Note (1) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

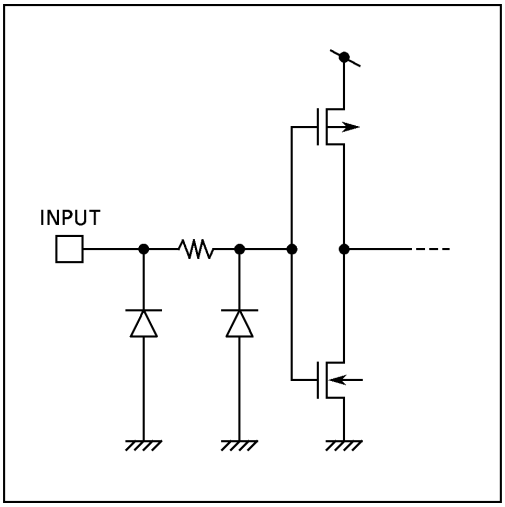
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = −40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	— —	7.0 7.0	8.0 8.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		3.3 ± 0.3 5.0 ± 0.5	— —	6.0 6.0	7.0 7.0	
Minimum Set-Up Time (SL, SR)	t_S		3.3 ± 0.3 5.0 ± 0.5	— —	8.5 5.0	10.0 5.0	
Minimum Set-Up Time (A~H)	t_S		3.3 ± 0.3 5.0 ± 0.5	— —	8.0 4.0	9.0 4.0	
Minimum Set-Up Time (S0, S1)	t_S		3.3 ± 0.3 5.0 ± 0.5	— —	14.5 7.0	17.0 8.0	
Minimum Hold Time (SL, SR)	t_h		3.3 ± 0.3 5.0 ± 0.5	— —	1.0 1.0	1.0 1.0	
Minimum Hold Time (A~H)	t_h		3.3 ± 0.3 5.0 ± 0.5	— —	0.5 1.5	0.5 1.5	
Minimum Hold Time (S0, S1)	t_h		3.3 ± 0.3 5.0 ± 0.5	— —	0 0.5	0 0.5	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		3.3 ± 0.3 5.0 ± 0.5	— —	5.0 4.0	6.0 4.0	

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

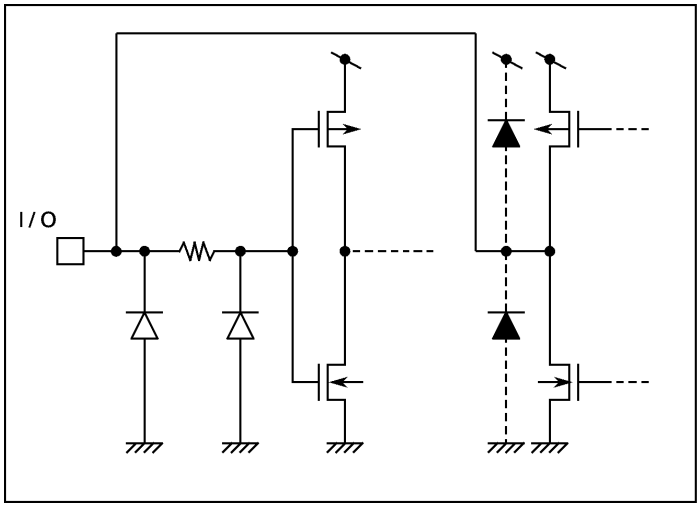
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$C_L = 50pF$	5.0	0.9 (1.0)	1.2 (1.4)	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$C_L = 50pF$	5.0	− 0.9 (− 1.0)	− 1.2 (− 1.4)	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	$C_L = 50pF$	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	$C_L = 50pF$	5.0	—	1.5	V

(Note) The value in ( ) only applies to JEDEC SOP (FW) devices.

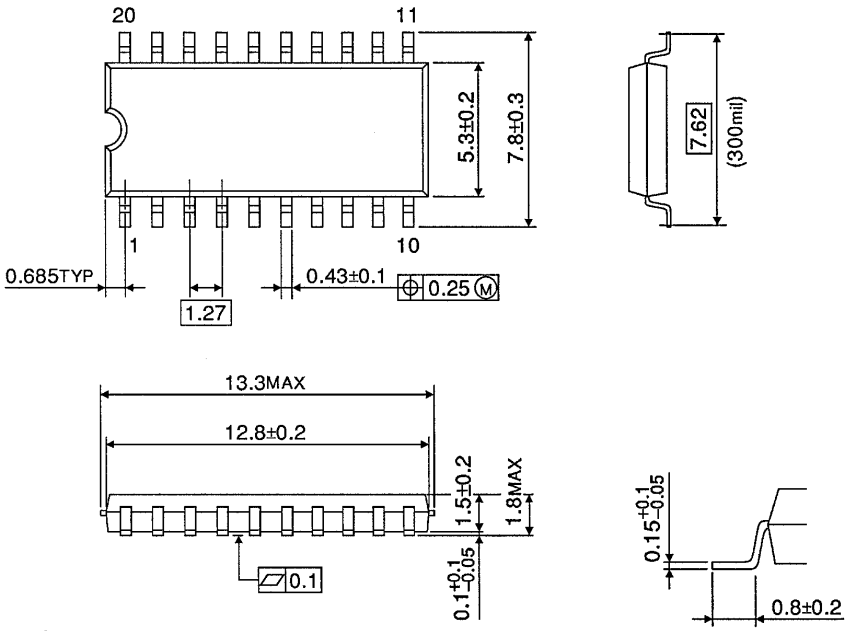
INPUT EQUIVALENT CIRCUIT



A/QA~H/QH BUS TERMINAL EQUIVALENT CIRCUIT



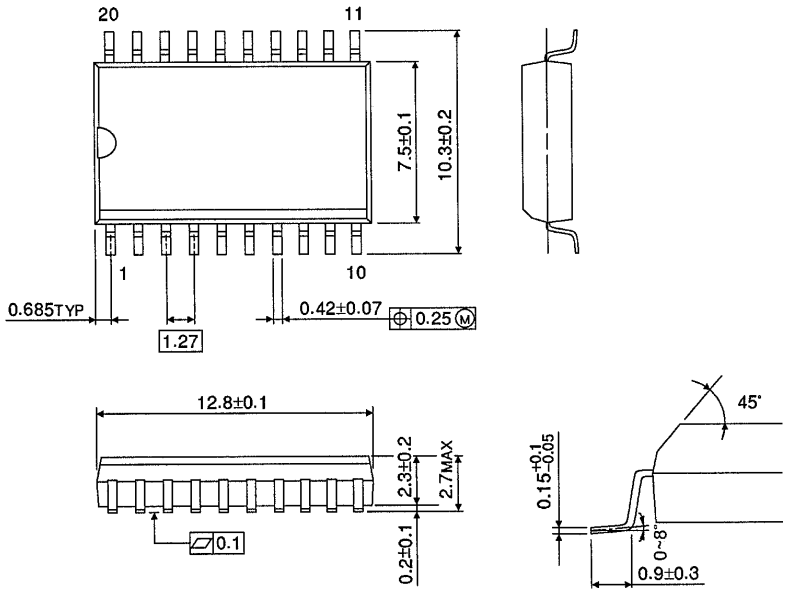
SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27) Unit in mm



Weight : 0.22g (Typ.)

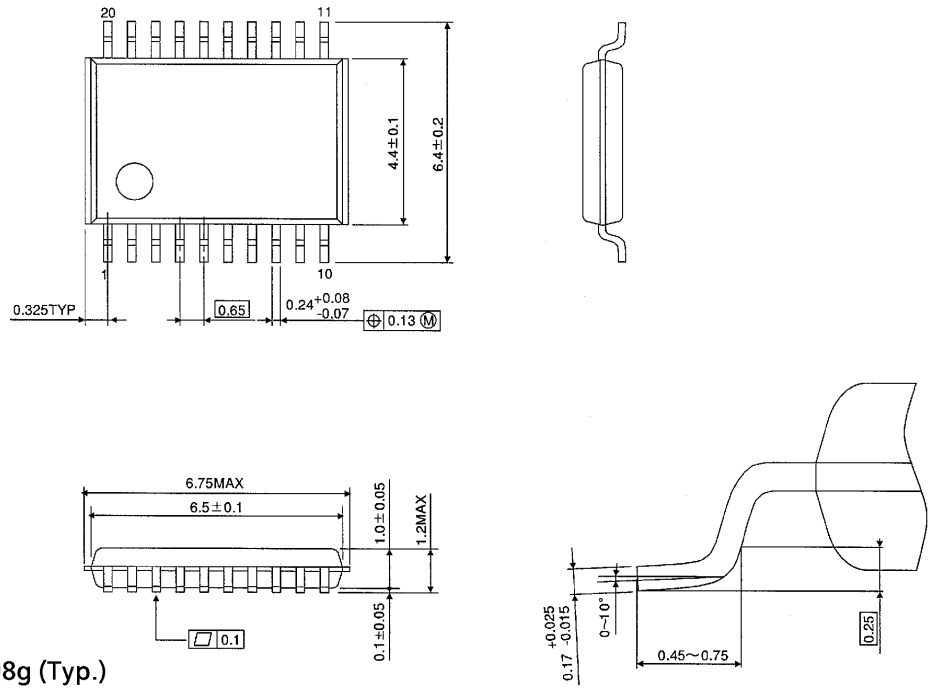
SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65) Unit in mm



Weight : 0.08g (Typ.)

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