

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

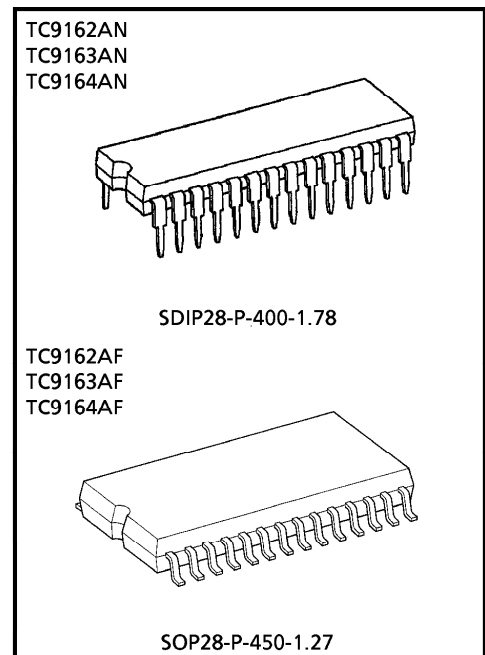
**TC9162AN, TC9163AN, TC9164AN
TC9162AF, TC9163AF, TC9164AF**

HIGH VOLTAGE ANALOG FUNCTION SWITCH ARRAY

TC9162AN/AF, TC9163AN/AF and TC9164AN/AF are analog switch arrays for high voltage application. By inputting the specified serial data, the analog switches are controlled. As each analog switch is independently controllable, switch of wide use is available.

FEATURES

- Analog switches of 16 circuits are built in, allowing to provide three types according to internal connections.
- Dual power supply of (+) and (-) can be used. In this case the switch select data is operated in a single power supply by the built-in level shifter. As the threshold level of the input inverter is designed low, interface with CMOS microcomputer is easily available.
- As the analog switches are high-voltage (30V) use and have superior linearity of on-resistance, extra low distortion and wide dynamic range can be realized.
- Owing to CMOS structure current consumption is low.
- Package is shrunked DIP 28 PIN.



Weight
 SDIP28-P-400-1.78 : 2.2g (Typ.)
 SOP28-P-450-1.27 : 0.8g (Typ.)

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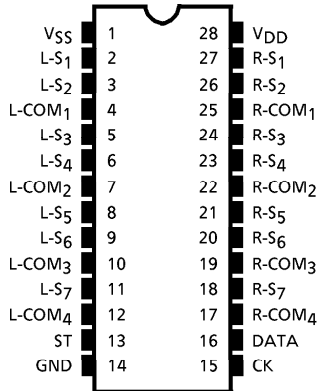
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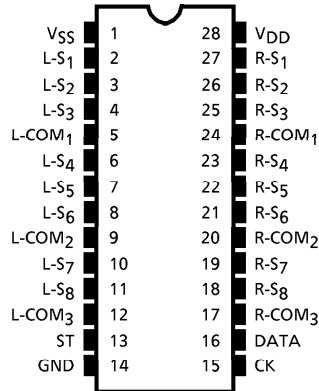
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PIN CONNECTION (TOP VIEW)

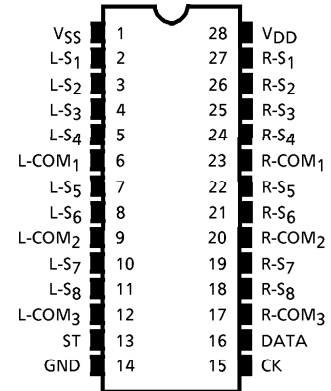
TC9162AN / AF



TC9163AN / AF

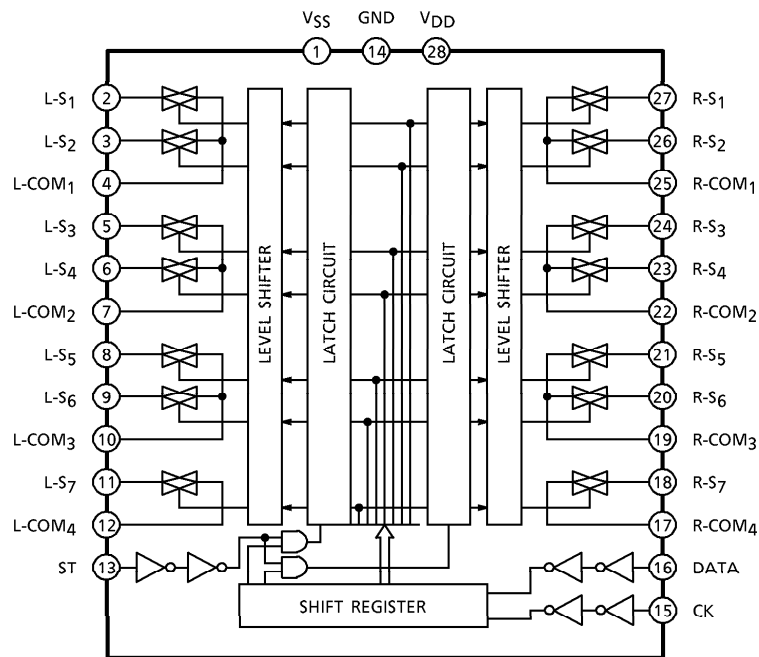


TC9164AN / AF

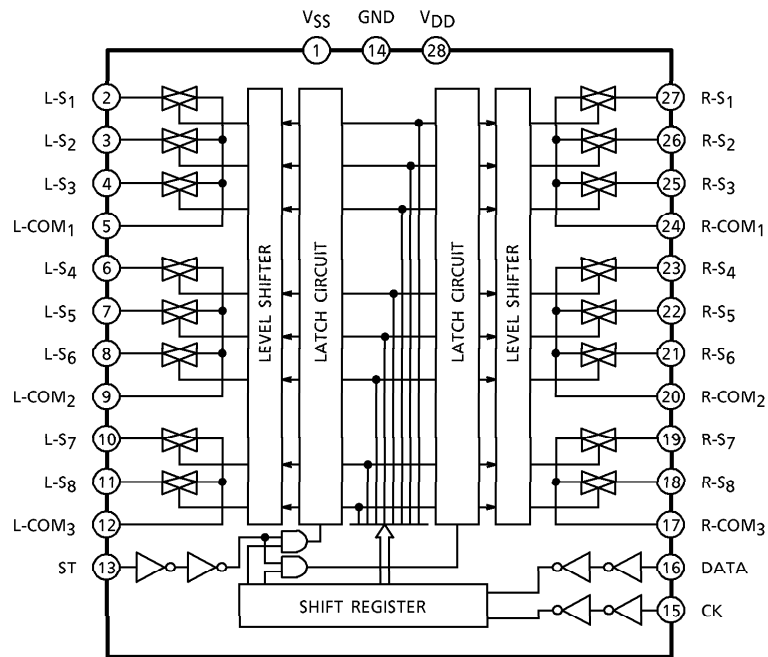


BLOCK DIAGRAM

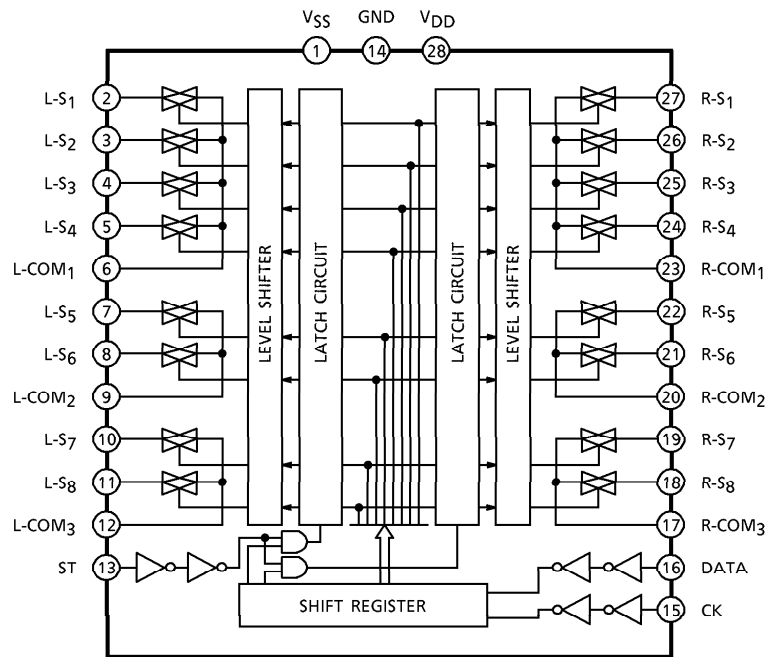
TC9162AN / AF



TC9163AN / AF



TC9164AN / AF



DESCRIPTION OF PIN FUNCTIONS (L-ch / R-ch)

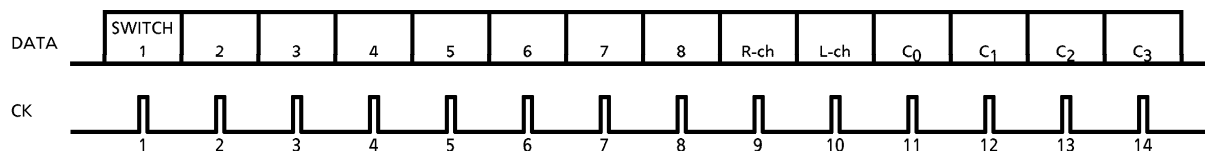
| PIN No. | | | SYMBOL | PIN NAME | FUNCTION & OPERATION | NOTE |
|-----------------|-----------------|-----------------|-----------------|-----------------------|---|------------------------------|
| TC9162 AN/AF | TC9163 AN/AF | TC9164 AN/AF | | | | |
| 1 | | | V _{SS} | - Power Terminal | Applies Supply Voltage. | — |
| 14 | | | GND | Ground Terminal | | |
| 28 | | | V _{DD} | + Power Terminal | | |
| 2 / 27 | 2 / 27 | 2 / 27 | S ₁ | Switch Input Terminal | Input & Output Terminal for Analog Switch | — |
| 3 / 26 | 3 / 26 | 3 / 26 | S ₂ | | | |
| 5 / 24 | 4 / 25 | 4 / 25 | S ₃ | | | |
| 6 / 23 | 6 / 23 | 5 / 24 | S ₄ | | | |
| 8 / 21 | 7 / 22 | 7 / 22 | S ₅ | | | |
| 9 / 20 | 8 / 21 | 8 / 21 | S ₆ | | | |
| — | 11 / 18 | 11 / 18 | S ₈ | | | |
| 4 / 25 | 5 / 24 | 6 / 23 | COM1 | | | |
| 7 / 22 | 9 / 20 | 9 / 20 | COM2 | | | |
| 10 / 19 | 12 / 17 | 12 / 17 | COM3 | | | |
| 12 / 17 | — | — | COM4 | | | |
| 13 | | | ST | Strobe Input Terminal | Strobe Input for Data Interrupt | Low Threshold Input Terminal |
| 15 | | | CK | Clock Input Terminal | Clock Input for Data Transfer | |
| 16 | | | DATA | Data Input Terminal | Serial Data Input for Switch Setting | |

DESCRIPTION OF OPERATION

DATA INPUT

Each analog switch array of TC9162AN / AF, TC9163AN / AF and TC9164AN / AF can be optionally controlled by inputting specified data to DATA, CK, and ST terminals.

The data are composed of 14 bit as follows.



As the bit 1~8 correspond to the analog switches 1 to 8 respectively, set the bit of the desired switch to the level "1" (see Note).

Bit 9 and 10 are channel selecting bit (left and right). When either one of these bit is set to level "1", the desired channel is selected. The selection is made both simultaneously ("1" and "1") as well as either right or left independently ("1" and "0", "0" or "1").

Bit 11 to 14 are code bit to be used for chip selection.

For example, when TC9162AN / AF, TC9163AN / AF and TC9164AN / AF are used simultaneously, if DATA, CK and ST terminals of each device are commonly connected, either one of TC9162AN / AF, TC9163AN / AF or TC9164AN / AF can be selected by these code bit data.

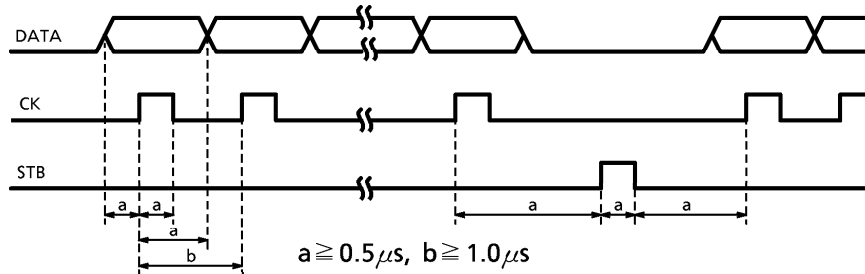
The codes are set respectively as follows :

| | C ₀ | C ₁ | C ₂ | C ₃ |
|---------------|----------------|----------------|----------------|----------------|
| TC9162AN / AF | 0 | 0 | 0 | 0 |
| TC9163AN / AF | 1 | 0 | 0 | 0 |
| TC9164AN / AF | 0 | 1 | 0 | 0 |

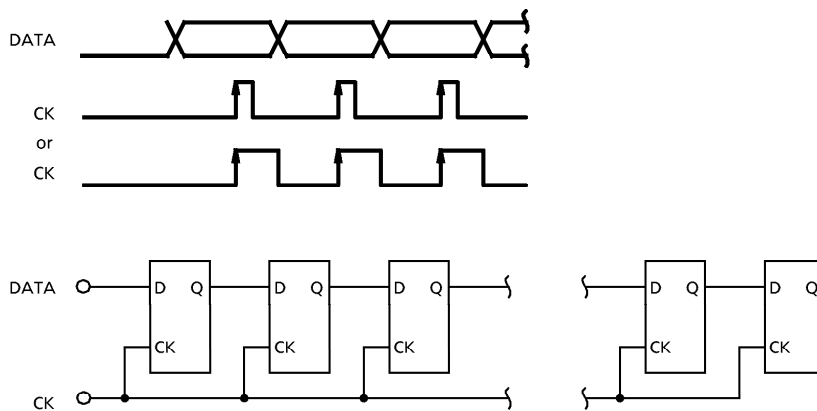
Note : As for TC9162AN / AF, the switch consists of 7 circuits.
So the 8bit must be used at level "0".

TIMING OF DATA, CK and ST

Input data to the DATA, CK and ST terminals in the following timing conditions.



The data to the DATA terminal is input to the internal shift registers sequentially with synchronizing to the rise of the input to the CK terminal.



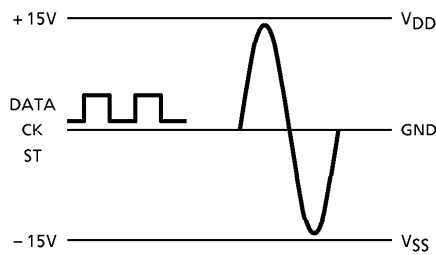
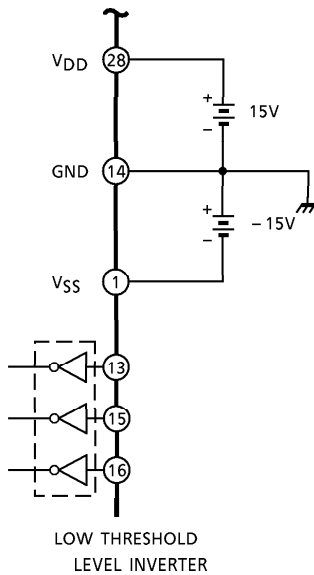
The input data are finally transferred to the latch circuit from the shift register by the ST signal, updating the previous data.

POWER SUPPLY CORRELATIONS

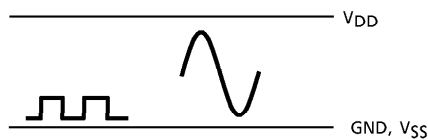
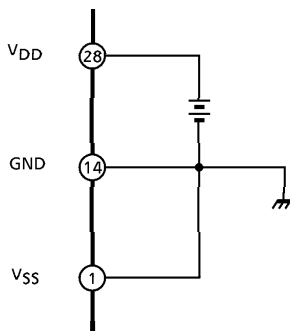
As the power supply sequence of analog switch part and control part, the analog part can be used by a dual power supply of (+) and (-), in which case, the control part operates in single power supply.

As the threshold level of the terminals of CK, DATA and ST are designed to low, CMOS microcomputers of 5V system can be easily interfaced in.

○ USE OF DUAL POWER SUPPLY



○ USE OF SINGLE POWER SUPPLY



The operating voltage range of a single power supply use is half of a dual power supply use.

MAXIMUM RATINGS (Ta = 25°C)

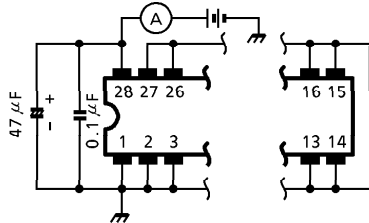
| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|-----------------------|-------------------|----------------------------------|------|
| Supply Voltage (1) | $V_{DD} - V_{SS}$ | -0.3~36 | V |
| Supply Voltage (2) | $V_{DD} - GND$ | -0.3~20 | V |
| Input Voltage | V_{IN} | $V_{SS} - 0.3 \sim V_{DD} + 0.3$ | V |
| Power Dissipation | P_D | 300 | mW |
| Operating temperature | T_{opr} | -40~85 | °C |
| Storage Temperature | T_{stg} | -65~150 | °C |

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_{DD} = 15V$, $V_{SS} = -15V$, $GND = 0V$, $T_a = 25^\circ C$)

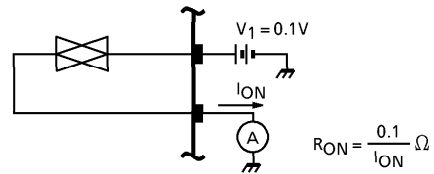
| CHARACTERISTIC | SYMBOL | TEST CIRCUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------------------|-------------------|--------------|---|------|-------|----------|---------------|
| Operating Supply Voltage (1) | $V_{DD} - V_{SS}$ | — | Dual power operation | 16 | ~ | 34 | V |
| Operating Supply Voltage (2) | $V_{DD} - GND$ | — | Single power operaiton | 8 | ~ | 18 | V |
| Operating Supply Current | I_{DD} | — | No loaded, open | — | 0.01 | 0.1 | mA |
| Back-up Voltage | V_B | — | Data holding voltage | 4 | ~ | 18 | V |
| Back-up Current | I_B | — | $V_{DD} = 4.0V$, $V_{SS} = GND = 0V$ | — | 1 | 10 | μA |
| Input Voltage | "H" level | V_{IH} | CK, DATA, ST terminal | 4 | ~ | V_{DD} | V |
| | "L" level | V_{IL} | | GND | ~ | 1.0 | |
| Operating Min. Pulse Width | t_{Min} | — | — | 0.5 | — | — | μs |
| Switch-on Resistance | R_{ON} | 2 | — | — | 80 | 100 | Ω |
| Total Harmonic Distortion | THD | 3 | $f_{in} = 0 \sim 20kHz$, $V_{in} = 1V_{rms}$ | — | 0.001 | 0.005 | % |
| Noise Voltage | V_{NO} | 4 | $f = 20 \sim 50kHz$ | — | 1.0 | 10 | μV_{rms} |

APPLICATION CIRCUIT

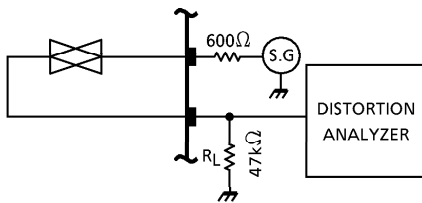
1. BACK-UP CIRCUIT



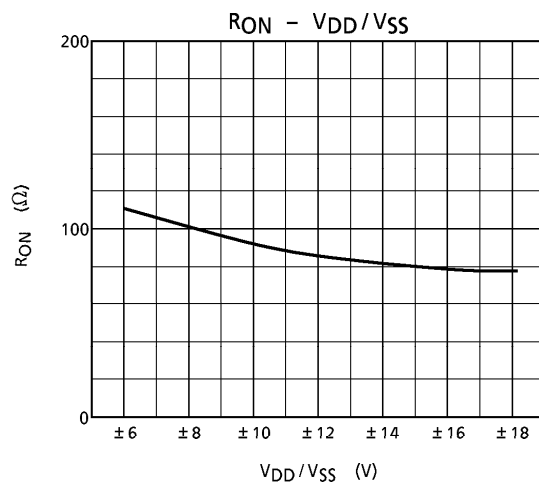
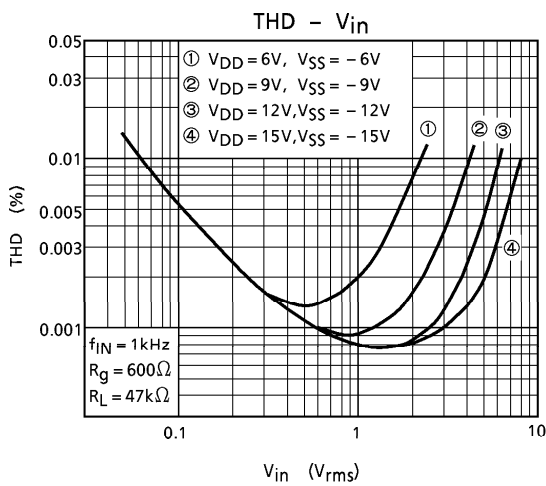
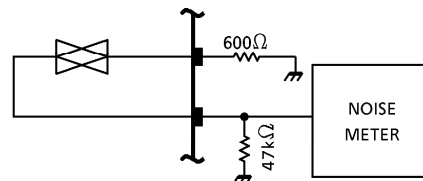
2. SWITCH-ON RESISTANCE



3. TOTAL HARMONIC DISCRPTION



4. NOISE VOLTAGE

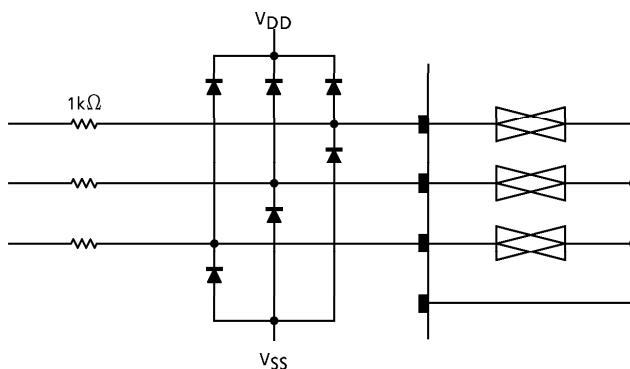


APPLICATION INFORMATION**1. AT POWER ON**

When a voltage is applied, the analog switch is under an unstable condition.
Provide external measures such as muting until the data is finally set.

2. PROTECTION AGAINST EXCESS INPUT

When there is a possibility of inputting an excess voltage, more than $V_{DD}-V_{SS}$, to the analog switch, add a protective circuit as shown below :

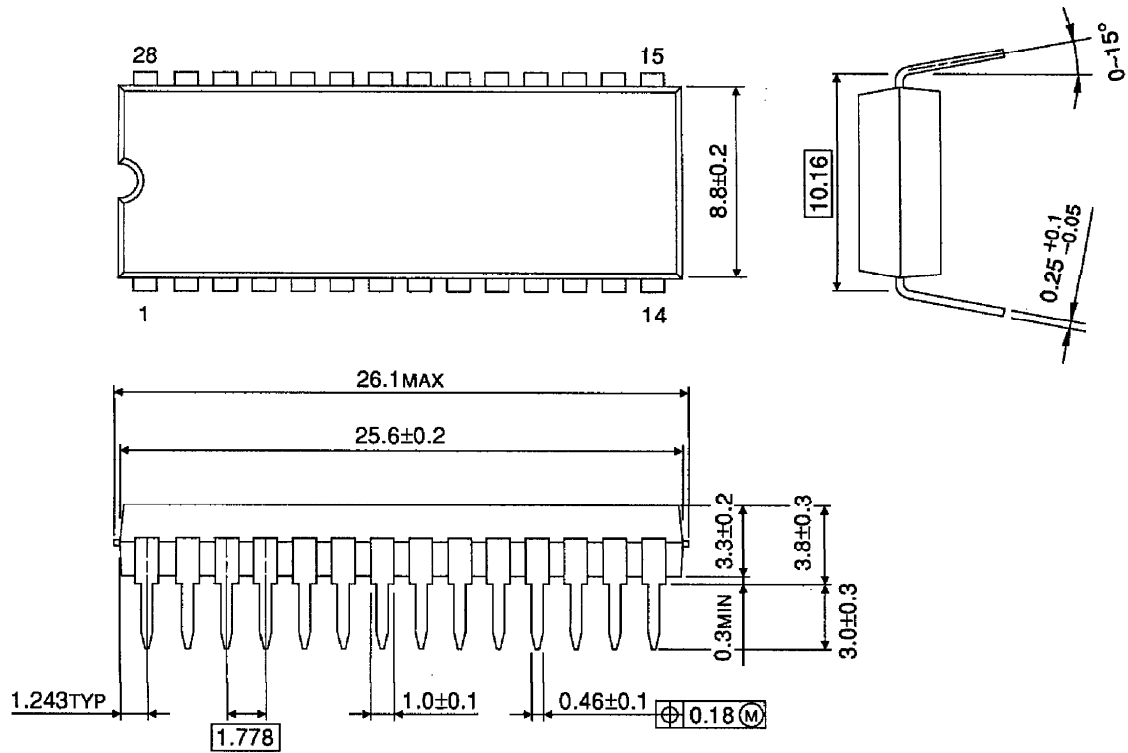
**3. NOISE AT DATA TRANSFERRING**

Some frequency of the CK signal may affect the analog switch and cause noises at data transferring.

CK signals should be at the frequency out of audio band as possible.

OUTLINE DRAWING
SDIP28-P-400-1.78

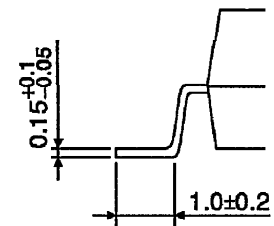
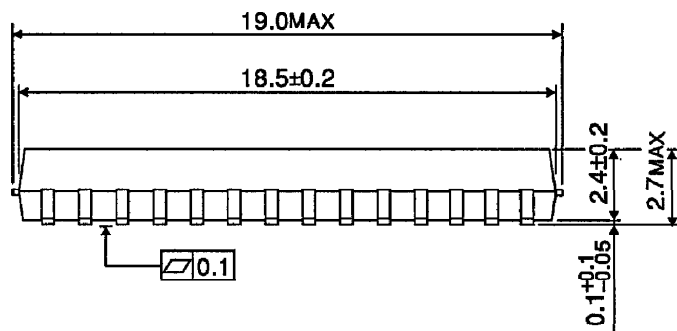
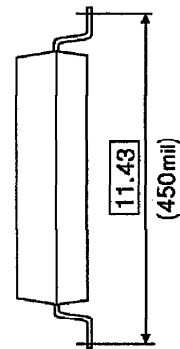
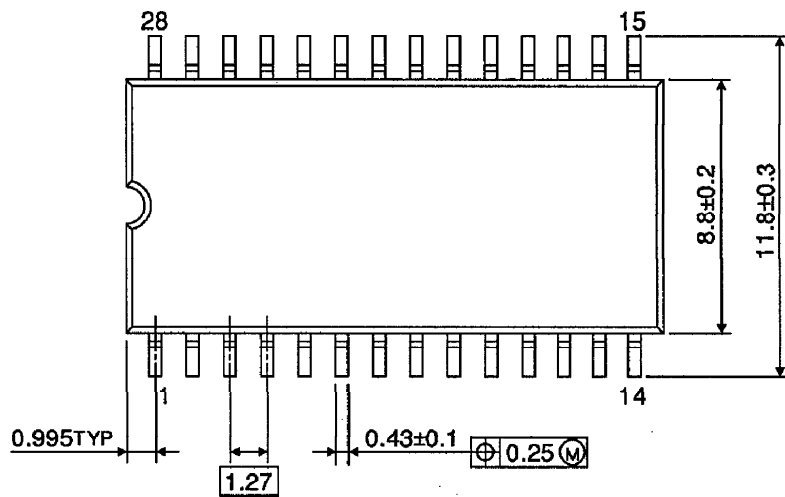
Unit : mm



Weight : 2.2g (Typ.)

OUTLINE DRAWING
SOP28-P-450-1.27

Unit : mm



Weight : 0.8g (Typ.)