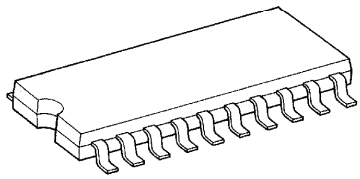
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9278F, TC9278P

Σ-Δ MODULATION SYSTEM DA CONVERTER WITH BUILT-IN 8 TIMES OVER SAMPLING DIGITAL FILTER

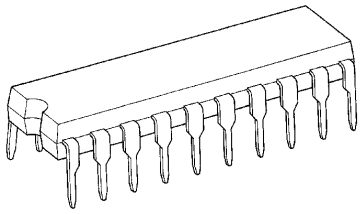
TC9278F, TC9278P are 2'nd order Σ-Δ modulation system 1bit DA converter incorporating an 8-times over sampling digital filter developed for digital audio equipment. Because the IC is small package (SOP20, DIP20) and includes the de-emphasis filter has been incorporation, it is possible to constitute reducing the size and cost of the DA converter.

TC9278F



SOP20-P-300-1.27

TC9278P



DIP20-P-300-2.54A

Weight
SOP20-P-300-1.27 : 0.48 g (Typ.)
DIP20-P-300A : 1.4 g (Typ.)

FEATURES

- Built-in 8-times over sampling digital filter.
- Low voltage operate (3.3 V).
- Built-in digital de-emphasis filter.
- Over sampling ratio (OSR) is 192 fs.
- Sampling frequency (fs) : 44.1 kHz
- Support double speed operation.
- Characteristics of the digital filter and DA converter are as follows :

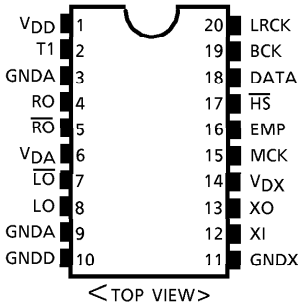
Digital filter

	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP-BAND SUPPRESSION
Standard operation	8 fs	±0.11 dB	20 k~24.1 kHz	−26 dB
Double speed operation	8 fs	±0.11 dB	20 k~24.1 kHz	−26 dB

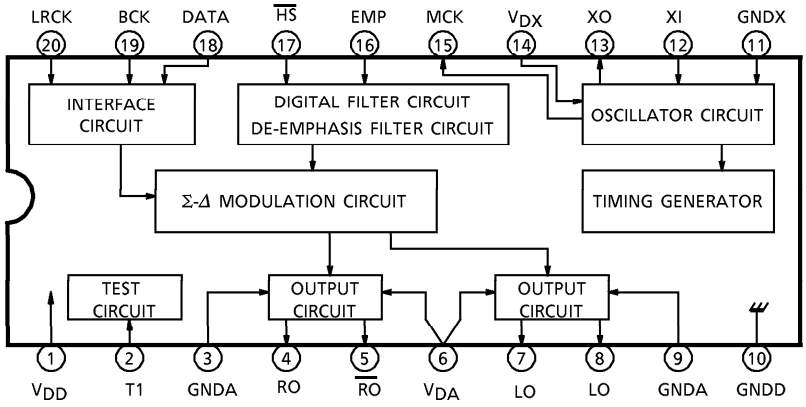
DA converter (V_{DD} = 5 V)

	OSR	NOISE DISTORTION	S/N RATIO
Standard operation	192 fs	−90 dB (Typ.)	98 dB (Typ.)
Double speed operation	96 fs	−85 dB (Typ.)	95 dB (Typ.)

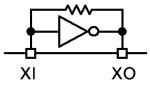
PIN CONNECTION



BLOCK DIAGRAM



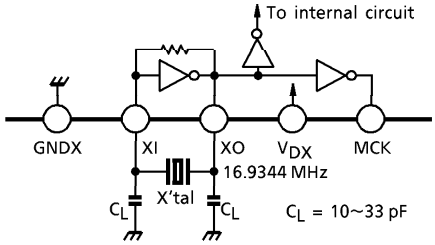
PIN FUNCTION

PIN No.	SYMBOL	I / O	FUNCTION & OPERATION	REMARKS
1	V_{DD}	—	Digital power supply pin	
2	T1	I	Test pin. Normally, use at "L".	
3	GNDA	—	Analog GND pin	
4	RO	O	Right channel data forward output pin.	
5	RO	O	Right channel data reversed output pin.	
6	V_{DA}	—	Analog power supply pin	
7	$\overline{LO}$	O	Left channel data reverse output pin.	
8	LO	O	Left channel data forward output pin.	
9	GNDA	—	Analog GND pin	
10	GNDD	—	Digital GND pin.	
11	GNDX	—	Crystal oscillator GND pin.	
12	XI	I	Crystal oscillator connection pin. Connect to a crystal oscillator, generates needed for the system. (384 fs)	
13	XO	O		
14	V_{DX}	—	Oscillator power supply pin.	
15	MCK	O	System clock output pin. (384 fs)	
16	EMP	I	De-emphasis filter ON / OFF switching pin. ON at "H" and OFF at "L".	
17	$\overline{HS}$	I	Standard / double speed operation mode switching pin. Standard operation at "H", double speed operation at "L".	
18	DATA	I	Audio data input pin.	
19	BCK	I	Bit clock input pin.	
20	LRCK	I	LR clock input pin.	

DESCRIPTION OF BLOCK OPERATION

1. Crystal oscillation circuit and timing generator

   The clock required for internal operations is generated by connecting a crystal and condensers as shown in the diagram below.
   The IC will also operate when a system clock is input from an external source through the XI pin (pin 12). However, in this situation, due consideration must be given to the fact that waveform characteristics, such as jitter and rising / falling characteristics of the system clock, significantly affect the DA converter's noise distortion and the S / N ratio.



Use a crystal with a low CI value and favorable start-up characteristics.

Fig. 1 Configuration of Crystal Oscillation Circuit

   The timing generator generates the clocks and process timing signals required for such functions as digital filtering and de-emphasis filtering.

2. Data input circuit

   DATA and the LRCK are loaded to the LSI internal shift registers on the BCK signal rising edge. It is consequently necessary for the DATA and LRCK signals to be synchronized and input on the BCK signal falling edge as indicated in the timing example below. BCK is available only 32 fs.
   Also, as DATA has been designed so that the 16 bits before the change point of LRCK are regarded as valid data, the data must be input with Right-justified mode.

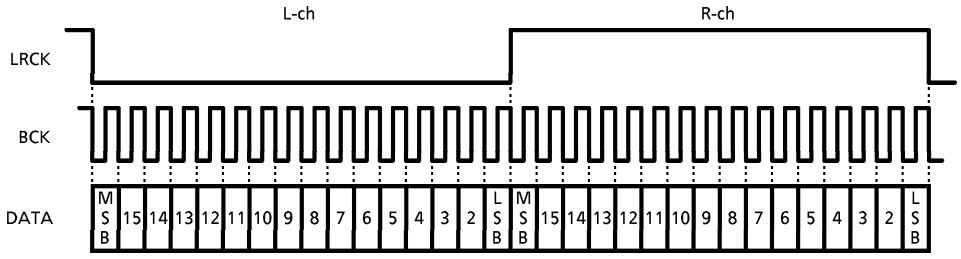


Fig.2 Example of input timing chart

3. Digital filter

The 8-times oversampling IIR digital filter eliminates the noise returned from outside the bandwidth during standard and double speed operations.

Table-1 basic characteristics of digital filter

	PASS-BAND RIPPLE	TRANSIENT BANDWIDTH	ATTENUATION
Standard operation	±0.11 dB	20.0 k~24.1 kHz	−26 dB or less
Double speed operation	±0.11 dB	20.0 k~24.1 kHz	−26 dB or less

The characteristics of the digital filter frequencies are shown below.

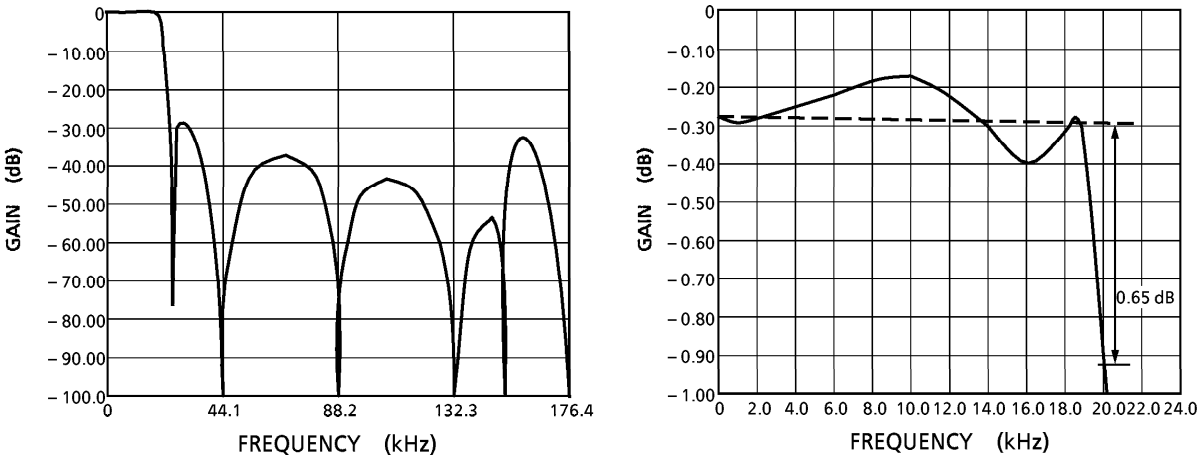


Fig.3 Digital filter frequency characteristics

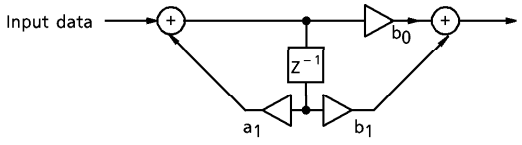
4. De-emphasis filter

The built-in IIR type digital de-emphasis filter circuit is available for fs = 44.1 kHz.
ON / OFF is controlled with the EMP pin.

Table-2 De-emphasis filter settings

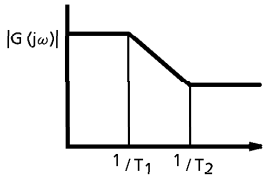
EMP PIN	H	L
De-emphasis Filter	ON	OFF

The digitalization of the de-emphasis filter eliminates the need for such external components as resistors, condensers and analog switches. In addition to this, the coefficients are aligned to reduce error in the de-emphasis filter characteristics.
The filter structure and characteristics are shown below.



Transfer function : $H(Z) = \dfrac{(b_0 + b_1 Z^{-1})}{(1 - a_1 Z^{-1})}$

Fig.4 IIR Digital De-emphasis Filter

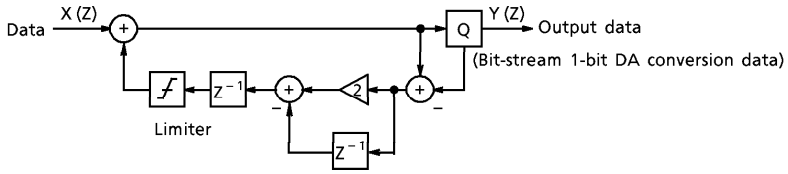


$T_1 = 50\ \mu s$, $T_2 = 15\ \mu s$

Fig.5 Filter Characteristics

5. DA conversion circuit

The IC incorporates a 2'nd order Σ-Δ modulation DA converter for two channels (simultaneous output type). The internal structure of this is shown in Fig.6.



2'nd order Σ-Δ converter : $Y(Z) = X(Z) + (1 - Z^{-1})^2 Q(Z)$

Fig.6 Σ-Δ modulation DA converter

The Σ-Δ modulation clock has been designed to operate at 192 fs. The noise shaping characteristics are shown in Fig.7.

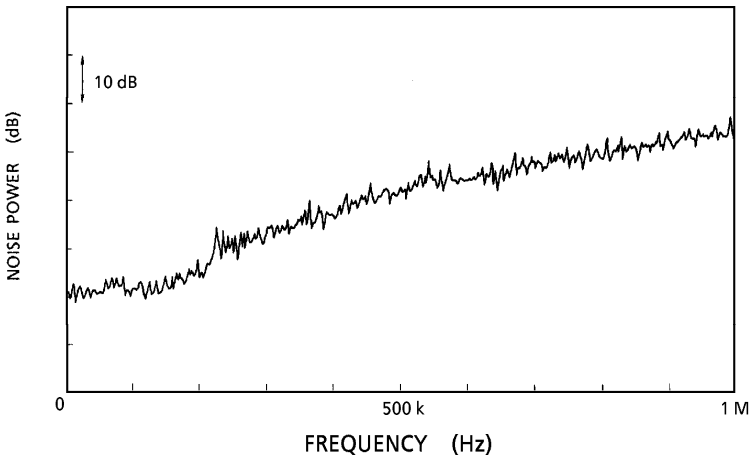


Fig.7 Noise shaping characteristic

6. Data output circuit

In this circuits, output data waveform is shaped and forward and reverse signals of bit stream data are output to the outside through a buffer.
By differentiating these forward signal and the reverse signal in the external analog circuit, DA conversion output of low distortion and high S/N ratio can be obtained.

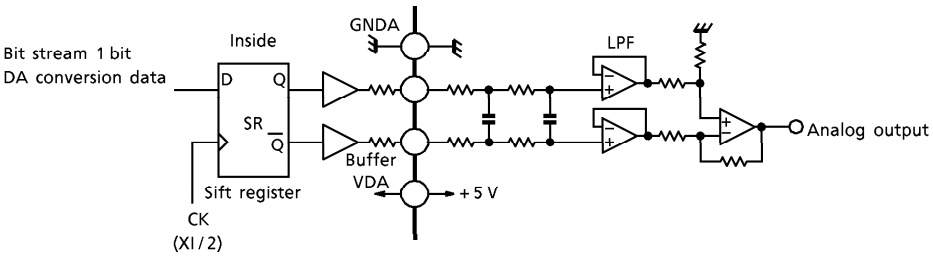


Fig.8 Construction of data output circuit

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	−0.3~6.0	V
		V_{DA}	−0.3~6.0	
		V_{DX}	−0.3~6.0	
Input Voltage		V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	TC9278F	P_D	200	mW
	TC9278P		300	
Operating Temperature		T_{opr}	−35~85	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = V_{DX} = V_{DA} = 5 V)

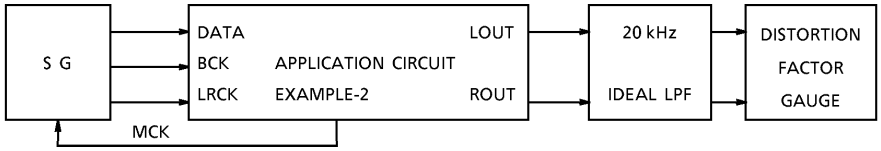
DC CHARACTERISTICS

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Supply Voltage (1)		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Operating Supply Voltage (2)		V_{DD}	—	Ta = −15~55°C (Operation frequency f_{opr} = 16.9 MHz)	3.3	3.5	5.5	V
		V_{DX}			3.3	3.5	5.5	
		V_{DA}			3.3	3.5	5.5	
Power Dissipation		I_{DD}	—	XI = 16.9 MHz	—	12	20	mA
Input Voltage	"H" Level	V_{IH}	—		V_{DD} × 0.7	—	V_{DD}	V
	"L" Level	V_{IL}			0	—	V_{DD} × 0.3	
Input Current	"H" Level	I_{IH}	—		−10	—	10	μA
	"L" Level	I_{IL}						

AC CHARACTERISTICS (Over sampling ratio = 192 fs)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Table Harmonic Distortion + Noise 1	THD + N1	1	1 kHz Sine wave, full-scale input V_{DD} = V_{DX} = V_{DA} = 5 V	—	−90	−80	dB
Table Harmonic Distortion + Noise 2	THD + N2	1	1 kHz Sine wave, full-scale input V_{DD} = V_{DX} = V_{DA} = 3.5 V	—	−86	−78	dB
S / N Ratio	S / N	1		90	98	—	dB
Dynamic Range	DR	1	1 kHz Sine wave, −60 dB input conversion	90	95	—	dB
Cross-talk	CT	1	1 kHz Sine wave, full-scale input	—	−95	−90	dB
Operating Frequency	f_{opr}	—	V_{DD} = V_{DA} = V_{DX} ≧ 4.5 V	—	16.9344	—	MHz
Input Frequency	f_{LR}	—	LRCK duty cycle = 50%	—	44.1	—	kHz
	f_{BCK}		BCK duty cycle = 50%	—	1.4112	—	MHz
Rise Time	t_r	—	LRCK, BCK (10~90%)	—	—	15	ns
Fall Time	t_f			—	—	15	
Delay Time	t_d	—	BCK ↓ Edge → LRCK, DATA	—	—	40	ns

- **TEST CIRCUIT-1** : With the use of application circuit example-2

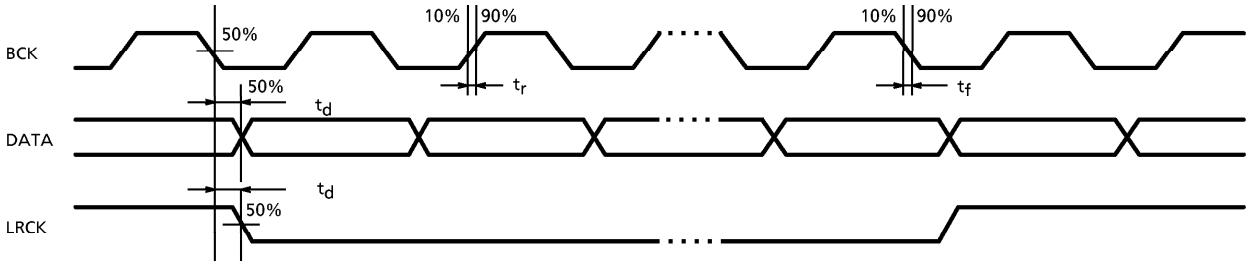


SG : ANRITSU MG-22A or equivalent
LPF : SHIBASOKU 725C internal filter
DISTORTION FACTOR GAUGE : SHIBASOKU 725C or equivalent

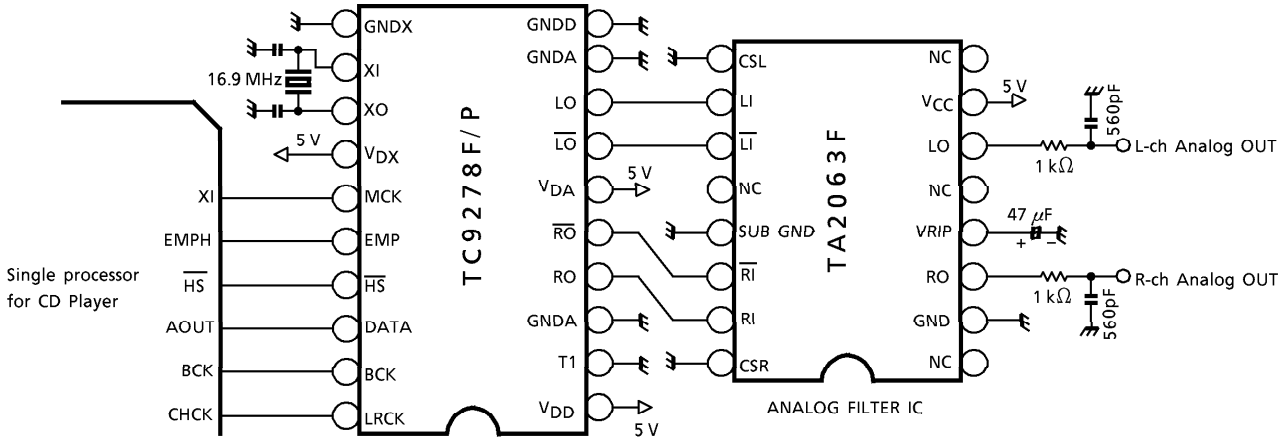
MEASURING ITEM	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S/N, DR	ON

A weight : IEC-A or equivalent

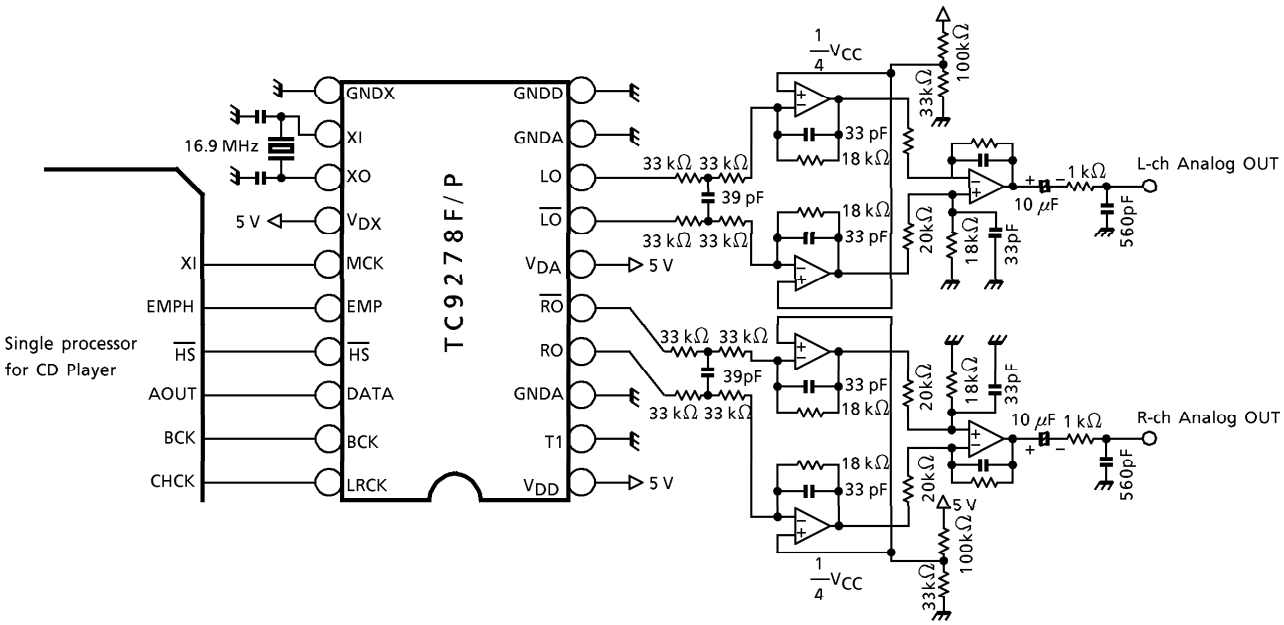
- **AC CHARACTERISTICS STIPULATED POINT** (Input signal stipulation : LRCK, BCK, DATA)



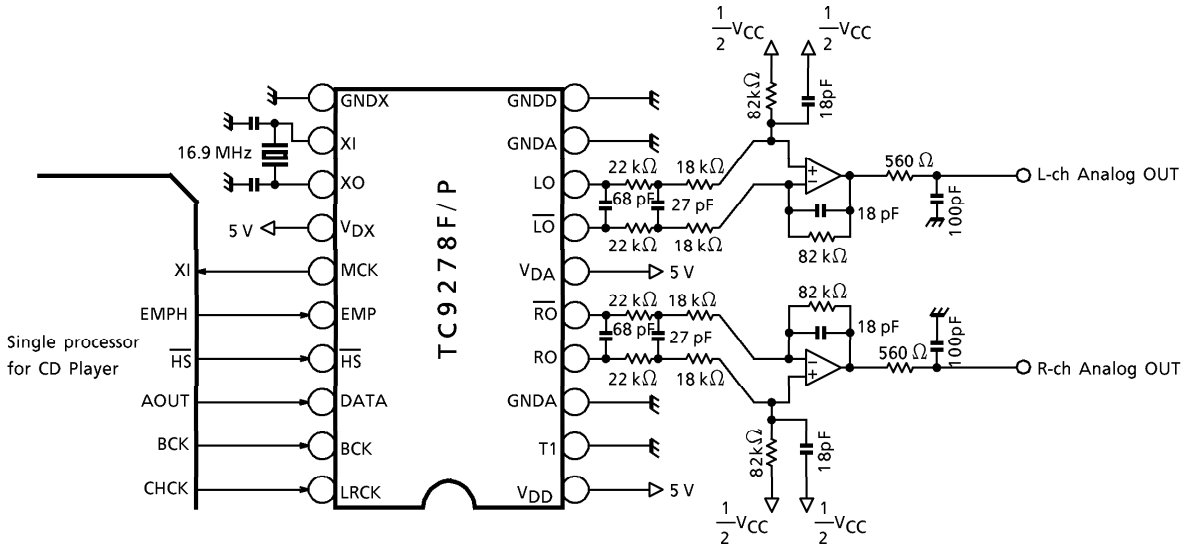
APPLICATION CIRCUIT EXAMPLE-1 (+5 V Single power supply used)



APPLICATION CIRCUIT EXAMPLE-2 (+5 V Two power supply used)



APPLICATION CIRCUIT EXAMPLE-3 (+5 V Single power supply used)

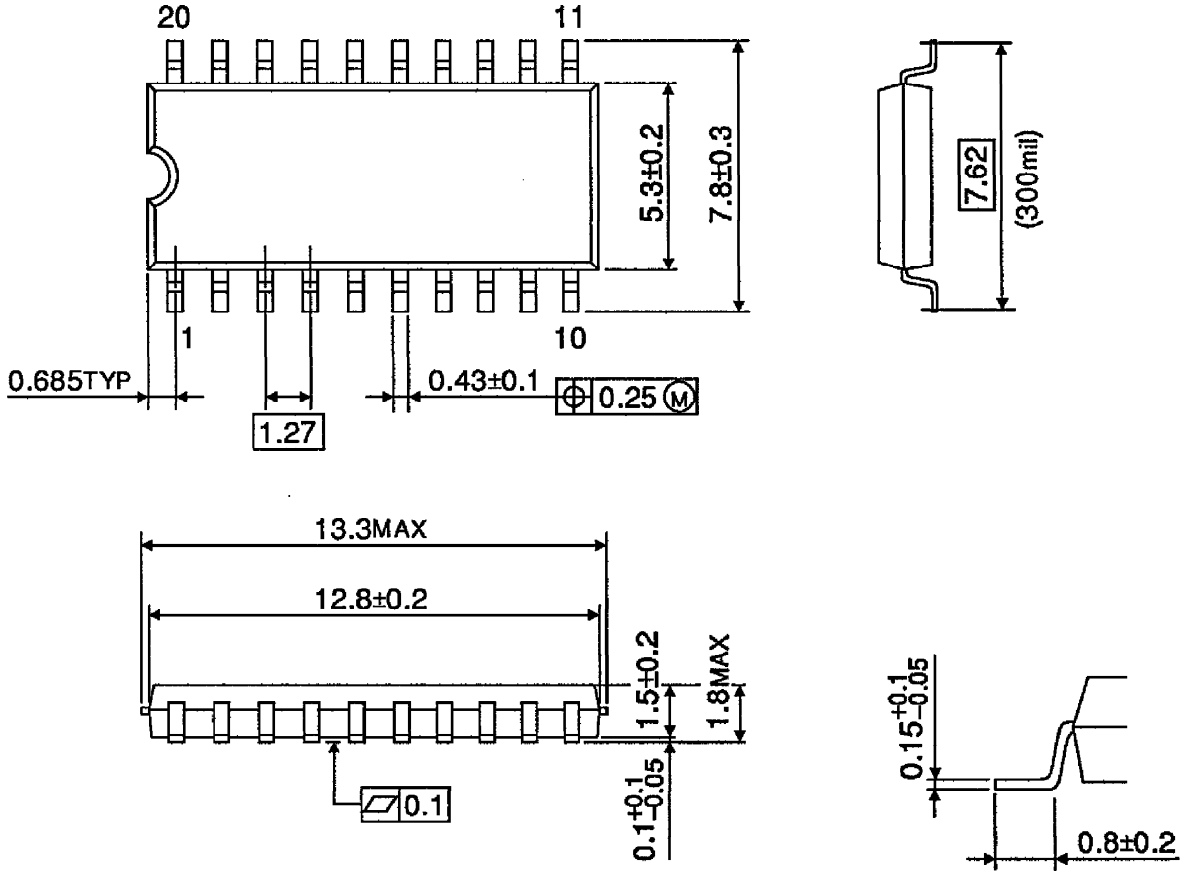


(Cautions)

- Quality of crystal oscillation waveform largely affect S/N ratio and noise distortion. Further, this is also true then system clock is input externally through the XI pin of Pin⑫.
- Suppress glitch of input signals (LRCK, BCK, DATA) as could as possible.
- The wiring between the TC9278F/P output and the analog filter amplifier input must be made the shortest.
- The capacitor between V_{DA} and GNDA, V_{DD} and GNDD, V_{DX} and GNDX shall be connected as close to the pin as possible.

PACKAGE DIMENSIONS

SOP20-P-300-1.27 Unit : mm

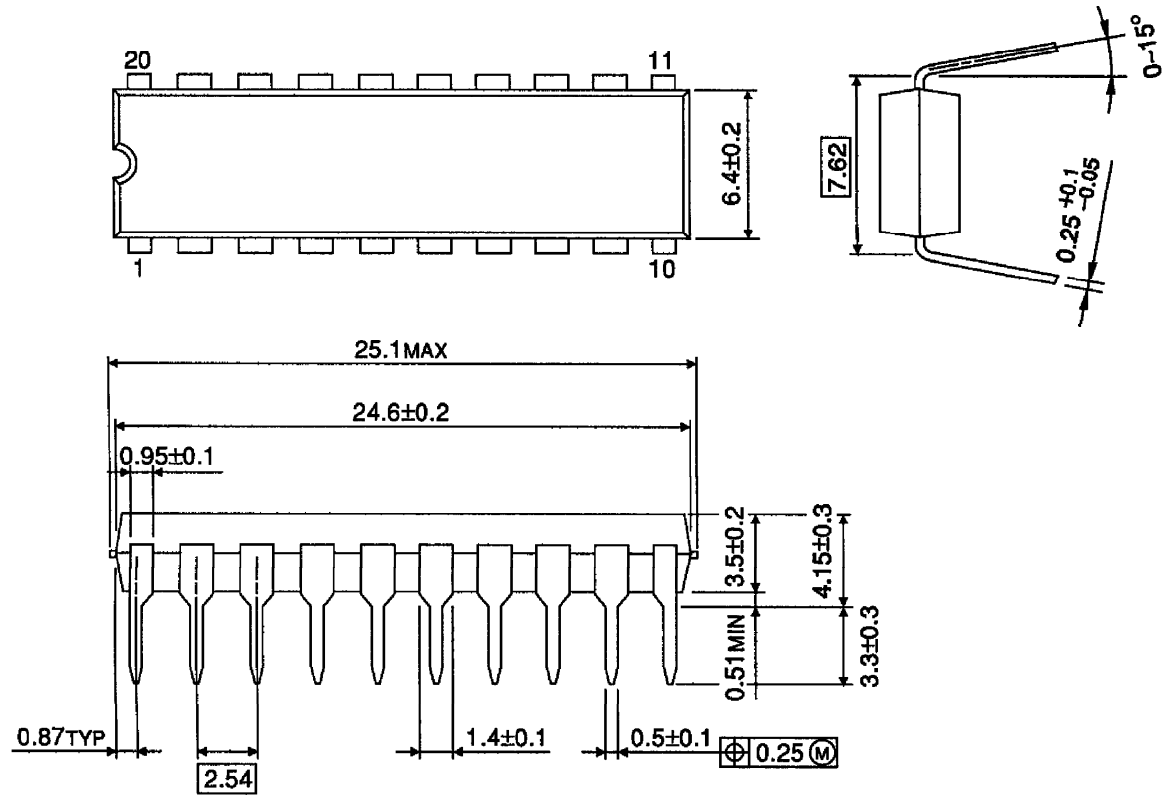


Weight : 0.48 g (Typ.)

PACKAGE DIMENSIONS

DIP20-P-300-2.54A

Unit : mm



Weight : 1.4 g (Typ.)