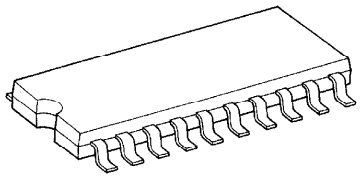
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9279F, TC9279P

Σ-Δ MODULATION SYSTEM DA CONVERTER WITH BUILT-IN 8 TIMES OVER SAMPLING DIGITAL FILTER

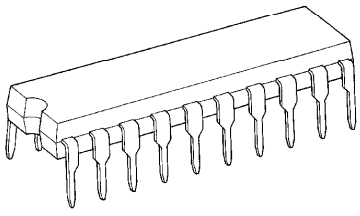
The TC9279F and TC9279P are a second-order Σ-Δ modulation system 1-bit DA converter incorporating an 8-times oversampling digital filter, dynamic digital bass boost function for use with compressor operations and an analog filter developed for digital audio equipment. Because the IC is small package (SOP20, DIP20) and includes the digital de-emphasis filter, it is possible to constitute reducing the size and cost of the DA converter.

TC9279F



SOP20-P-300-1.27

TC9279P



DIP20-P-300-2.54A

Weight
SOP20-P-300-1.27 : 0.48 g (Typ.)
DIP20-P-300-2.54A : 1.4 g (Typ.)

FEATURES

- Built-in 8-times oversampling digital filter
- Low voltage operations (3.3 V) possible
- Built-in digital de-emphasis filter
- DA converter oversampling ratio (OSR) is 192 fs
- Sampling frequency : 32 kHz, 48 kHz
- Characteristics of the digital filter and DA Converter are as follows:

Digital Filter (fs = 48 kHz)

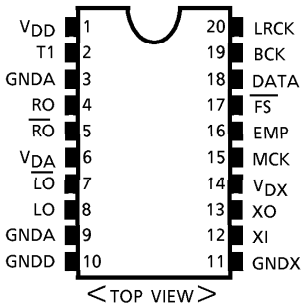
	Digital Filter	Pass-Band Ripple	Transient Band Width	Stop-Band Suppression
Standard Operation	8 fs	±0.11 dB	21.7 k~25.5 kHz	−26 dB or less

DA Converter (V_{DD} = 5.0 V)

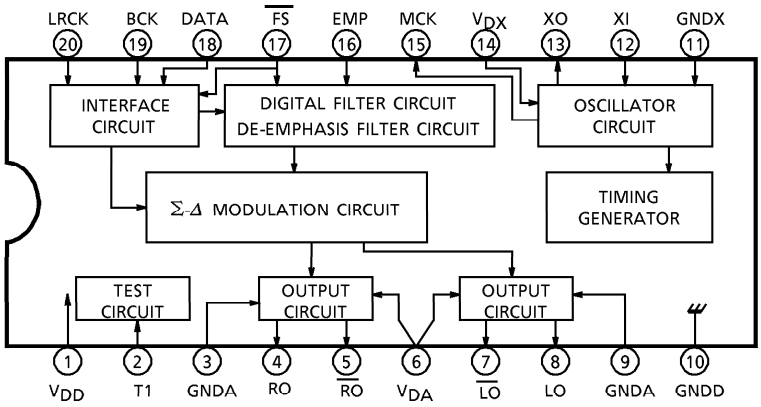
	OSR	Noise Distortion	S/N Ratio
Standard Operation	192 fs	−90 dB (Typ.)	100 dB (Typ.)

PIN CONNECTION

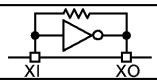
TC9279F, TC9279P



BLOCK DIAGRAM



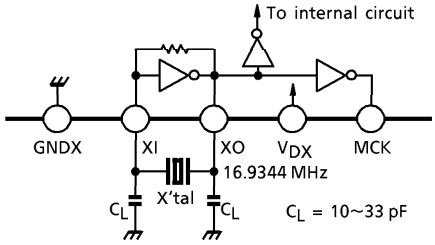
PIN FUNCTION

PIN No.	SYMBOL	I / O	FUNCTION & OPERATION	REMARKS
1	V_{DD}	—	Digital block power supply pin	
2	T1	I	Test pin. Normally, use at "L".	
3	GNDA	—	Analog GND pin for DA converter (R-channel)	
4	RO	O	R-channel data forward output pin.	
5	$\overline{RO}$	O	R-channel data reverse output pin.	
6	V_{DA}	—	Analog power supply pin for DA converter.	
7	$\overline{LO}$	O	L-channel data reverse output pin.	
8	LO	O	L-channel data forward output pin.	
9	GNDA	—	Analog GND pin for DA converter (L-channel)	
10	GNDD	—	Digital GND pin	
11	GNDX	—	Crystal oscillator GND pin	
12	XI	I	Crystal oscillator connection pin. Connecting a crystal oscillator, the system clock (384 fs) is generated.	
13	XO	O		
14	V_{DX}	—	Crystal oscillator power supply pin.	
15	MCK	O	System clock output pin (384 fs).	
16	EMP	I	De-emphasis filter ON / OFF switching pin. ON at "H" and OFF at "L".	
17	$\overline{FS}$	I	Sampling frequency mode selection pin "H" = 32 kHz, "L" = 48 kHz.	
18	DATA	I	Audio data input pin	
19	BCK	I	Bit clock input pin	
20	LRCK	I	LR clock input pin	

DESCRIPTION OF BLOCK OPERATION

1. Crystal Oscillation Circuit and Timing Generator

The clock required for internal operations is generated by connecting a crystal and condensers as shown in the diagram below.
The IC will also operate when a system clock is input from an external source through the XI pin (pin 15). However, in this situation, due consideration must be given to the fact that waveform characteristics, such as jitter and rising / falling characteristics of the system clock, significantly affect the DA converter's noise distortion and the S / N ratio.



Use a crystal with a low CI value and favorable start-up characteristics.

Fig.1 Crystal Oscillation Circuit Configuration (when in the 384 fs mode)

The timing generator generates the clocks and process timing signals required for such functions as digital filtering and de-emphasis filtering.

2. Data Input Circuit

DATA and the LRCK are loaded to the LSI internal shift registers on the BCK signal rising edge. It is consequently necessary for the DATA and LRCK signals to be synchronized and input on the BCK signal falling edge as indicated in the timing example below. Also, DATA has been designed so that the 16 bits before the change point of LRCK are regarded as valid data, the data.
BCK supports only 32 fs.

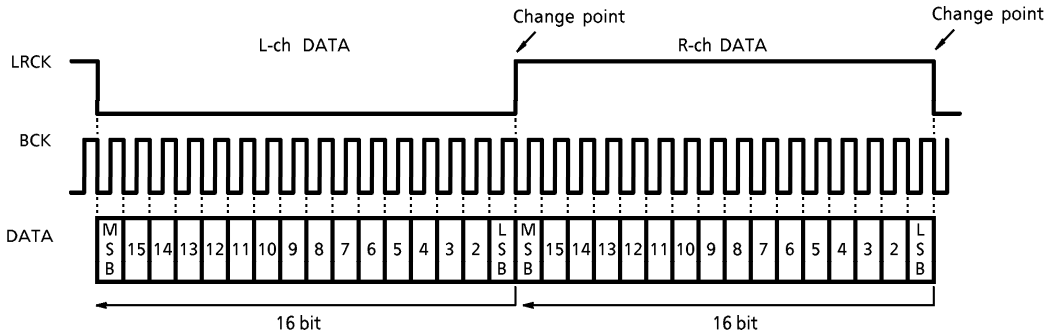


Fig.2 Example of Input Timing Chart

3. Digital Filter

The 8-times oversampling IIR digital filter eliminates the noise returned from outside the bandwidth during standard operations.

Table-1 Basic Characteristics of Digital Filter

	Pre-band Ripple	Transient Band Width	Attenuation
Standard Operation	0.011 dB	21.7 k~25.5 kHz	– 26 dB

The characteristics of the digital filter frequencies are shown below.

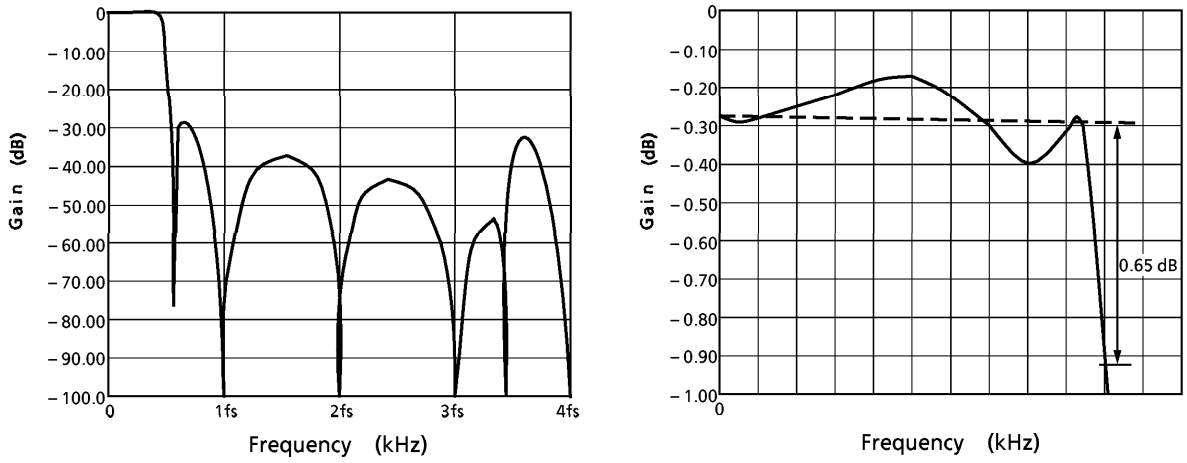
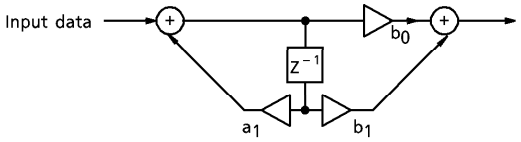


Fig.3 Digial Filter Frequency Characteristics

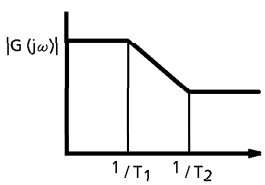
4. De-emphasis filer

The built-in IIR type de-emphasis filter circuit is available for two kinds of sampling frequency, fs of 32 kHz and 48 kHz.
The de-emphasis ON / OFF is controlled by EMP pin, and fs selection is controlled by $\overline{FS}$ pin.
Digitization of the de-emphasis filter has eliminated the necessity for external parts such as resistor, capacitor, analog switch, etc.
Further, to reduce the characteristic error of the de-emphasis filter, coefficients have been adjusted.
The construction and characteristics of the de-emphasis filter are shown below.
The digitalization of the de-emphasis filter eliminates the need for such external components as resistors, condensers and analog switches. In addition to this, the coefficients are aligned to reduce error in the de-emphasis filter characteristics.
The filter structure and characteristics are shown below.



Transfer function : $H(Z) = \dfrac{(b_0 + b_1 Z^{-1})}{(1 - a_1 Z^{-1})}$

Fig.4 IIR Digital De-emphasis Filter

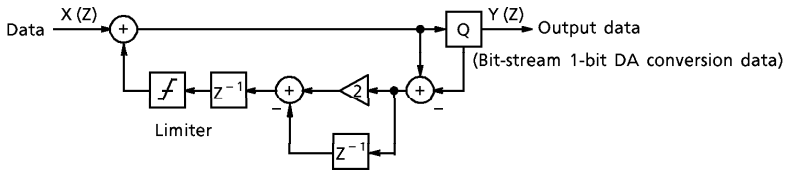


$T_1 = 50\ \mu s$, $T_2 = 15\ \mu s$

Fig.5 Filter Characteristics

5. DA Conversion Circuit

The IC incorporates a second-order Σ-Δ modulation DA converter for two channels (simultaneous output type). The internal structure of this is shown in Fig.6.



Second-order Σ-Δ converter : $Y(Z) = X(Z) + (1 - Z^{-1})^2 Q(Z)$

Fig.6. Σ-Δ modulation DA converter

The Σ-Δ modulation clock has been designed to operate at 192 fs. The noise shaping characteristics are shown in Fig.7.

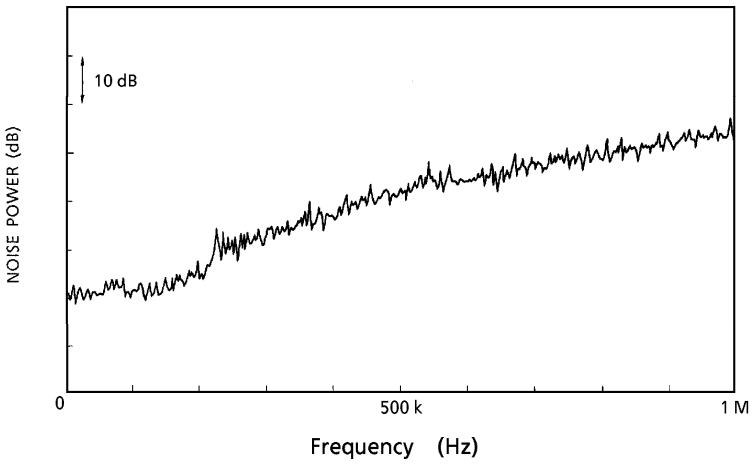


Fig.7 Noise Shaping Characteristics

6. Data Output Circuit

In this circuit, output data waveform is shaped, and forward and reverse signals of bit stream data are output to the outside through a buffer.
By differentiating these forward signal and the reverse signal in the external analog circuit, DA conversion output of low distortion and high S / N ratio can be obtained.

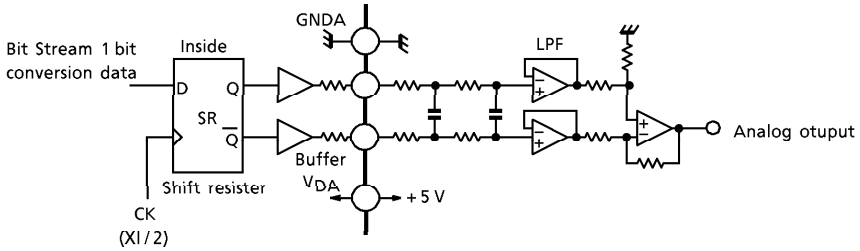


Fig.8 Construction of Data Output Circuit

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage		V_{DD}	−0.3~6.0	V
		V_{DA}		
		V_{DX}		
Input Voltage		V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	TC9279F	P_D	200	mW
	TC9279P		300	
Operating Temperature		T_{opr}	−35~85	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = V_{DX} = V_{DA} = 5 V)

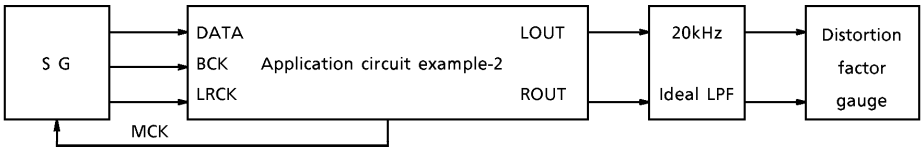
DC CHARACTERISTICS

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage (1)		V_{DD}	—	Ta = −35~85°C	4.5	5	5.5	V
		V_{DX}						
		V_{DA}						
Opeating Supply Voltage (2)		V_{DD}	—	Ta = −15~55°C (Operation frequency 12 MHz ≦ f_{opr} ≦ 18.5 MHz)	3.3	3.5	5.5	V
		V_{DX}						
		V_{DA}						
Power Dissipation		I_{DD}	—	XI = 18.4 MHz	—	12	20	mA
Input Voltage	"H" Level	V_{IH}	—		V_{DD} × 0.7	—	V_{DD}	V
	"L" Level	V_{IL}			0	—	V_{DD} × 0.3	
Input Current	"H" Level	I_{IH}	—		−10	—	10	μA
	"L" Level	I_{IL}						

AC CHARACTERISTICS (Oversampling ratio = 192 fs)

Table Harmonic Distortion + Noise 1	THD + N1	1	1 kHz sine wave, full-scale input V_{DD} = V_{DX} = V_{DA} = 5 V	—	−90	−80	dB
Table Harmonic Distortion + Noise 2	THD + N2	1	1 kHz sine wave, full-scale input V_{DD} = V_{DX} = V_{DA} = 3.5 V	—	−86	−78	dB
S/N Ratio	S/N	1		90	100	—	dB
Dynamic Range	DR	1	1 kHz sine wave −60 dB input conversion	90	95	—	dB
Cross-talk	CT	1	1 kHz sine wave full-scale input	—	−95	−90	dB
Operating Frequency	f_{opr}	—	V_{DD} = V_{DA} = V_{DX} ≧ 4.5 V	12	—	18.5	MHz
Input Frequency	f_{LR}	—	LRCK duty cycle = 50%	30	48	—	kHz
	f_{BCK}			1.0	1.536	—	MHz
Rise Time	t_r	—	LRCK, BCK (10%~90%)	—	—	15	ns
Fall Time	t_f			—	—	15	
Delay Time	t_d	—	BCK Edge → LRCK, DATA	—	—	40	ns

- Test circuit 1 : With the use of an application circuit example 2

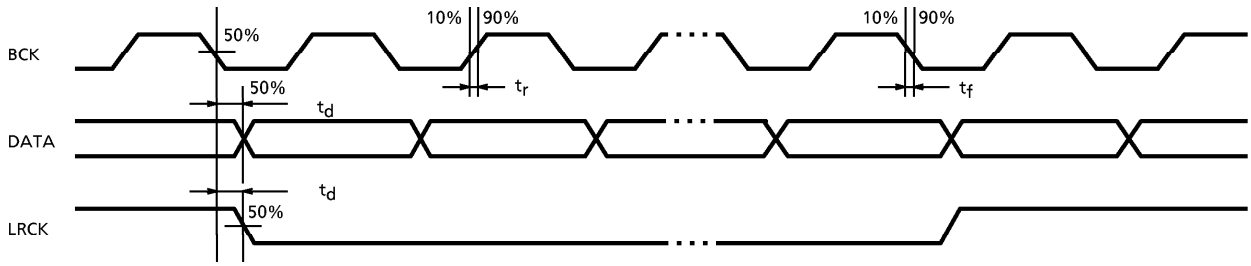


SG : Anritsu : MG-22A or equivalent
LPF : Shibasoku : Built-in 725C distortion factor gauge filter
Distortion : Shibasoku : 725C or equivalent

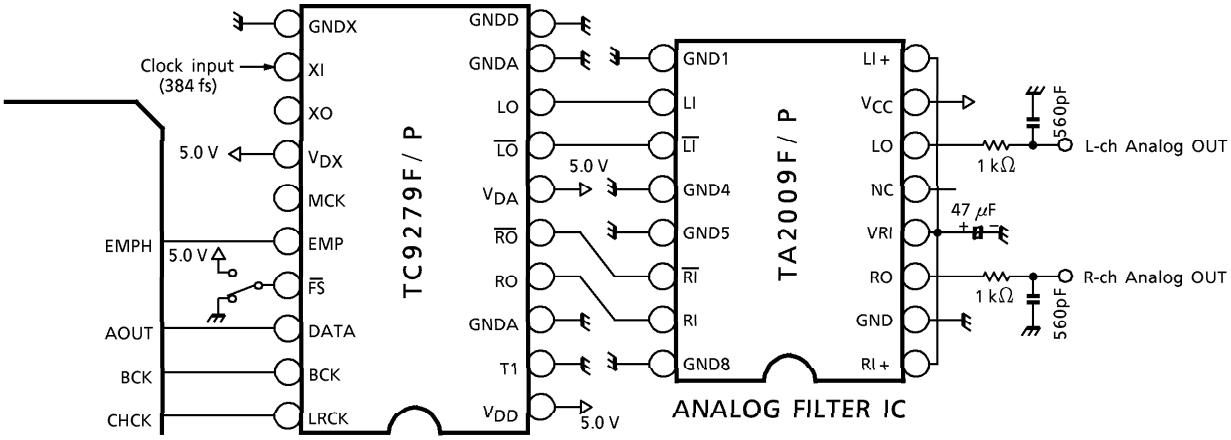
PARAMETER MEASURED	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S/N, DR	ON

A weight : IEC-A or equivalent

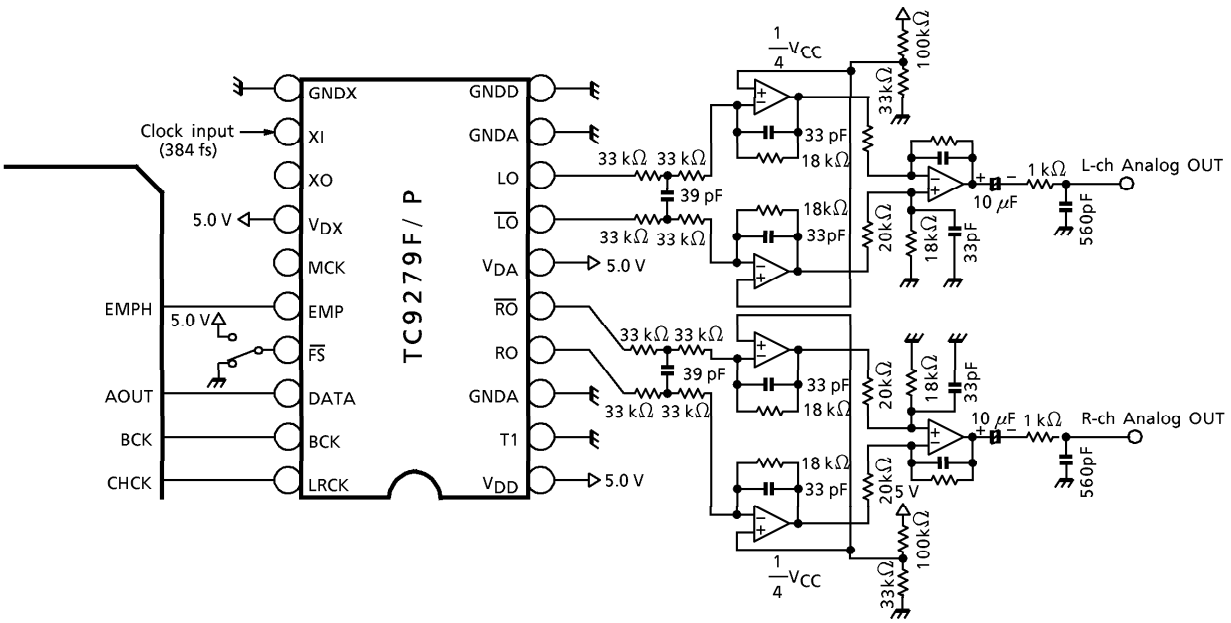
- AC Characteristics Stipulated Point (Input signal stipulation : LRCK, BCK, DATA)



APPLICATION CIRCUIT EXAMPLE-1 (+5 V Single Power Supply Used)



APPLICATION CIRCUIT EXAMPLE-2 (±5V Two Power Supply Used)

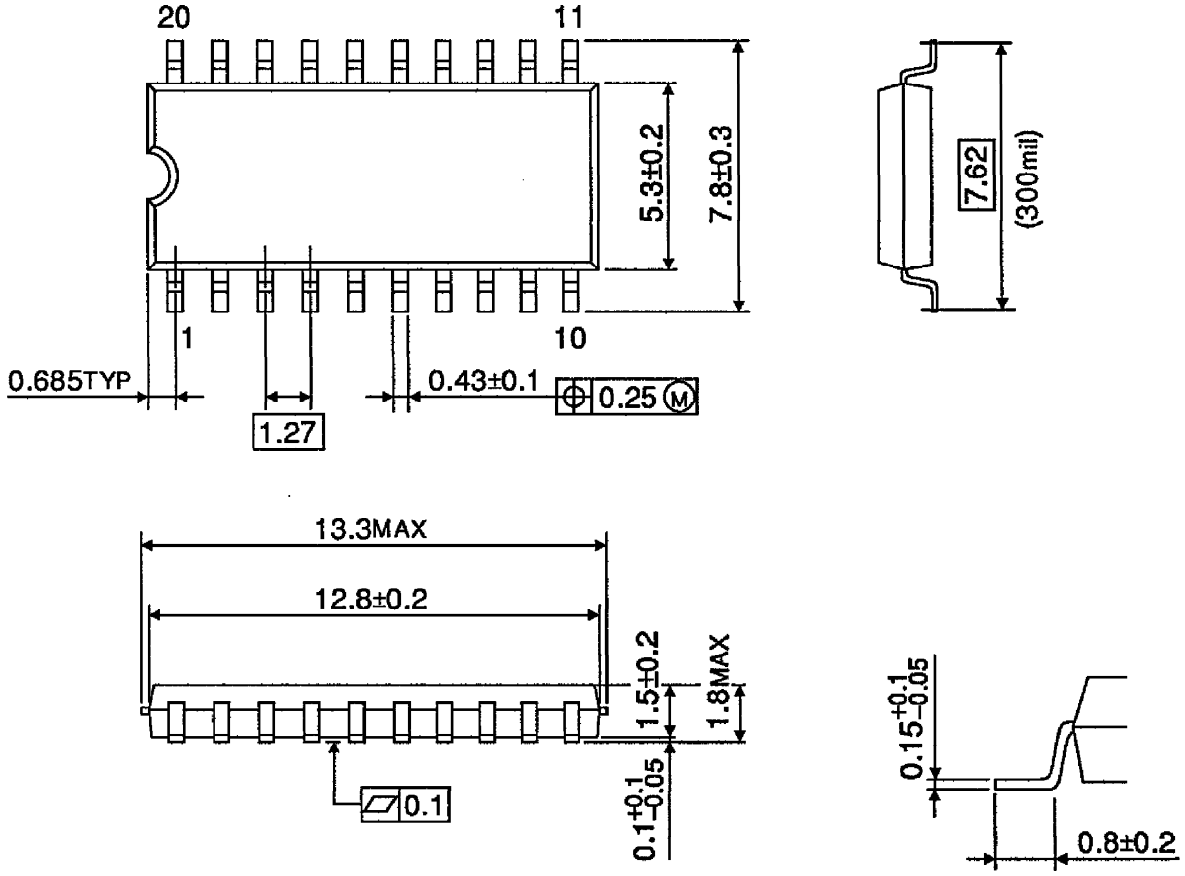


(Cautions)

- Quality of crystal oscillation waveform largely affect S/N ratio and noise distortion. Further, this is also true when system clock is input externally through the XI pin of pin 12.
- Suppress the input signals grige (LRCK, BCK, DATA) as small as possible.
- The wiring between the output pin of the TC9279F/P and the input pin of analog filter amplifier must be wired as short as possible.
- The condencer between V_{DA} and GNDA shall be connected as close to the pin as possible.

PACKAGE DIMENSIONS

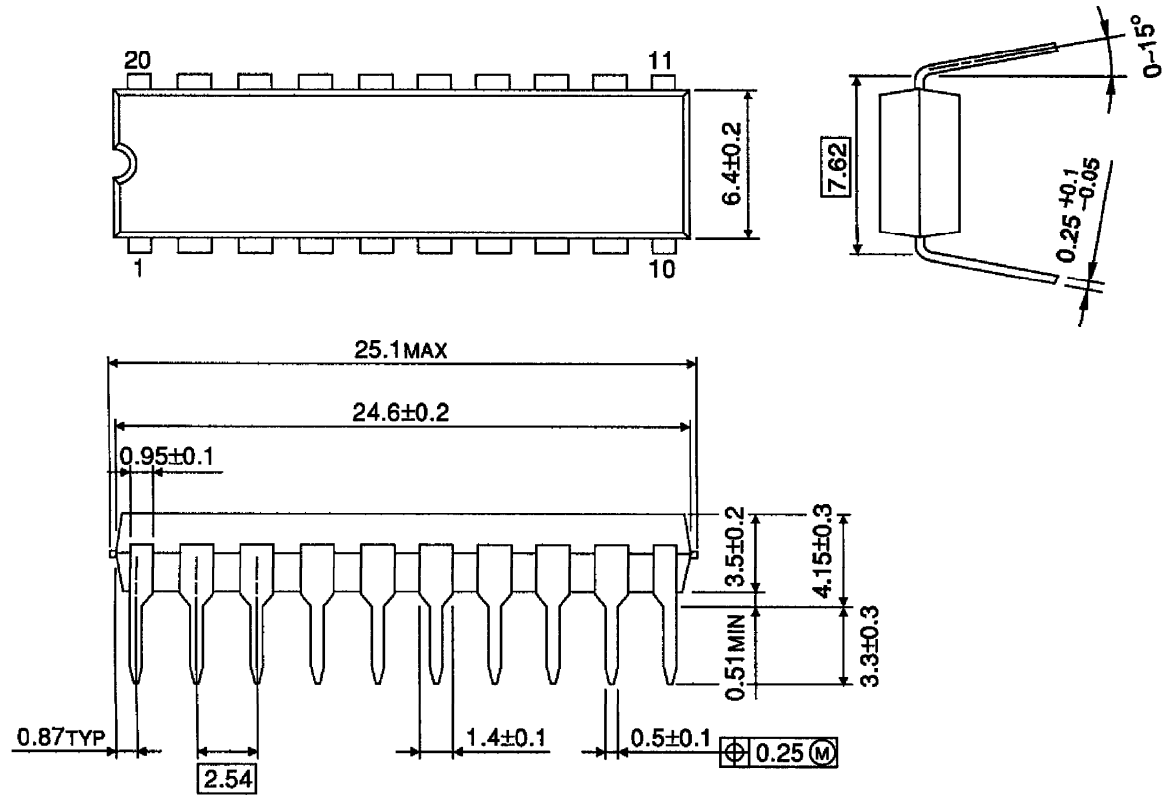
SOP20-P-300-1.27 Unit : mm



Weight : 0.48 g (Typ.)

PACKAGE DIMENSIONS

DIP20-P-300-2.54A Unit : mm



Weight : 1.4 g (Typ.)

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