TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62382AFN

8CH LOW INPUT ACTIVE DARLINGTON SINK DRIVER

The TD62382AFN is non-inverting transistor array which is comprised of eight Low saturation output stages and PNP input stages.

This device can be operated by source input voltage and is suitable for operation with a 5-V general pourposed logic IC such as TTL, 5-V CMOS and 5-V Microprocessor which have sink current output drivers.

Applications include relay, hammer, lamp and LED display drivers.

Please observe the thermal condition for using.

FEATURES

• Low Saturation Output : 0.23 V (MAX)

 $@ I_{out} = 40 \text{ mA (MAX)}$

Package Type
SSOP18 pin (0.65 mm pitch)
Output Rating
50 V (MIN) / 50 mA (MAX)

• Low Level Active Input

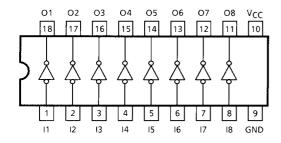
• Input Compatible with TTL and 5-V CMOS

Standard Supply Voltage

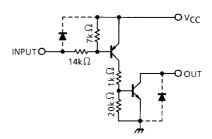
SSOP18-P-225-0.65

Weight: 0.09 g (Typ.)

PIN CONNECTION (TOP VIEW)



SCHEMATICS (EACH DRIVER)



Note: The input and output parasitic diodes cannot be used as clamp diodes.

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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT	
Supply Voltage	V _{CC}	-0.5~7.0	V	
Output Sustaining Voltage	V _{CE} (SUS)	-0.5~50	V	
Output Current	lout	50	mA / ch	
Input Voltage	V _{IN}	-22~VCC + 0.5	V	
Input Current	I _{IN}	10	mA	
Power Dissipation	P _D (Note)	0.96	W	
Operating Temperature	T _{opr}	-40~85	°C	
Storage Temperature	T _{stg}	-55~150	°C	

Note: On Glass Epoxy PCB (50 × 50 × 1.6 mm Cu 40%)

RECOMMENDED OPERATING CONDITIONS ($Ta = -40 \sim 85$ °C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT	
Supply Voltage		V _{CC}		4.5	5.0	5.5	V	
Output Sustaining Voltage		V _{CE} (SUS)		0	1	50	V	
Output Current		I _{OUT}	DC 1 Circuit	0	1	40	mA / ch	
			8 Circuits	0	1	40		
		V_{IN}		-20	_	V_{CC}		
Input Voltage	Output On	V _{IN (ON)}		-20	ı	V _{CC} - 3.5	V	
	Output Off	V _{IN (OFF)}		V _{CC} - 0.3	ı	V _{CC} + 0.5		
Power Dissipation		P _D (Note)		_	_	0.4	W	

Note: On Glass Epoxy PCB (50 × 50 × 1.6 mm Cu 40%)

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Output Leakage Current		I _{CEX}	1	V _{CC} = 5.5 V, I _{IN} = 0 V _{OUT} = 35 V, Ta = 75°C		1	_	100	μΑ
Output Saturation Voltage		V _{CE (sat)}	2	V _{CC} = 4.5 V, V _{IN} = 0.8 V I _{OUT} = 40 mA		-	_	0.23	V
Input Current	Output On I _{IN}	lua.u	3	V _{CC} = 5.5 V, V _{IN} = 0.4 V		_	-0.32	-0.45	mA
		IN (ON)		V _{CC} = 5.5 V, V _{IN} = -20 V		_	_	-2.6	
	Output Off	I _{IN (OFF)}	4			_	_	-40	μA
Input Voltage (Output on)		V _{IN (ON)}	5			-20	_	V _{CC} -3.5	V
Supply Current	Output On	I _{CC(ON)}		V _{CC} = 5.5 V, V _{IN} = 0 V		_	_	6	mA / ch
	Output Off	I _{CC(OFF)}	6	V _{CC} = V _{IN} = 5.5 V Ta = 75°C		-	_	100	μΑ
Turn-On Delay		t _{ON}	7	V _{CC} = 5 V	V _{OUT} = 50 V R _L = 1 kΩ	_	0.1	_	LIC.
Turn-Off Delay		t _{OFF}		C _L = 15 pF	V _{OUT} = 50 V R _L = 1 kΩ		3.0	_	μs

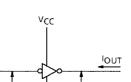
TEST CIRCUIT

1. ICEX

CEX

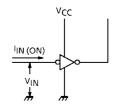
VOUT

2. VCE (sat)



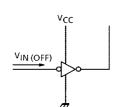
VCE (sat)

3. I_{IN} (ON)



4. I_{IN} (OFF)

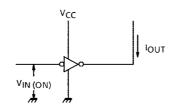
OPEN



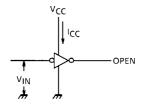
Vcc

5. V_{IN} (ON)

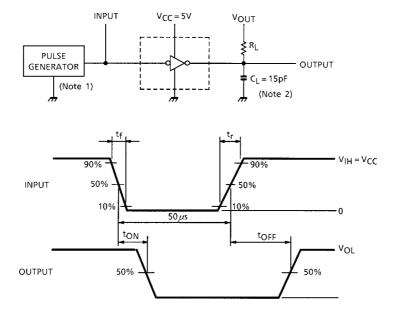
 V_{IN}



6. Icc



7. ton, toff



Note 1: Pulse Width 50 μs , Duty Cycle 10%

Output Impedance 50 Ω , $t_r \le 10$ ns, $t_f \le 5$ ns

Note 2: C_L includes probe and jig capacitance.

PRECAUTIONS for USING

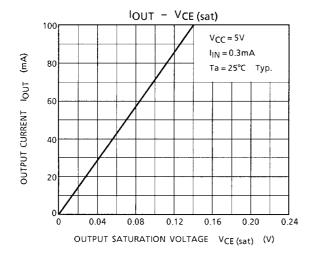
This IC does not include built-in protection circuits for excess current or overvoltage.

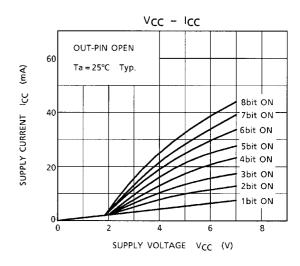
If this IC is subjected to excess current or overvoltage, it may be destroyed.

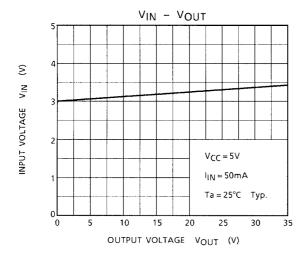
Hence, the utmost care must be taken when systems which incorporate this IC are designed.

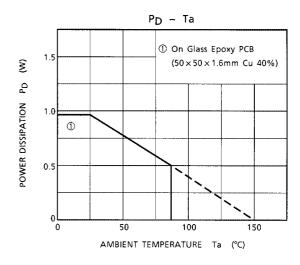
Utmost care is necessary in the design of the output line, VCC and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

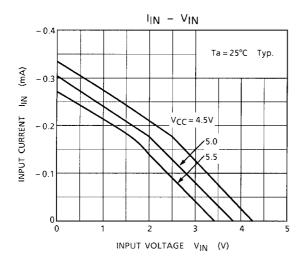
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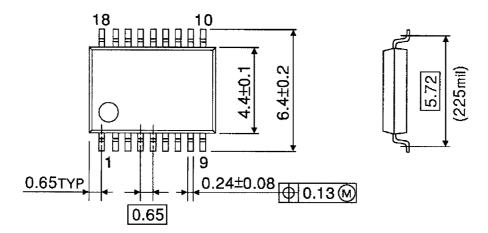


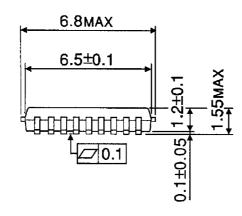


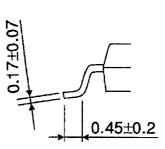


PACKAGE DIMENSIONS

SSOP18-P-225-0.65 Unit: mm







Weight: 0.09 g (Typ.)

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RESTRICTIONS ON PRODUCT USE

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