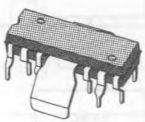
SGS-THOMSON MICROELECTRONICS

TDA1170S

TV VERTICAL DEFLECTION SYSTEM

- SYNCHRONIZATION CIRCUIT
- OSCILLATOR AND RAMP GENERATOR
- HIGH POWER GAIN AMPLIFIER
- FLYBACK GENERATOR
- VOLTAGE REGULATOR



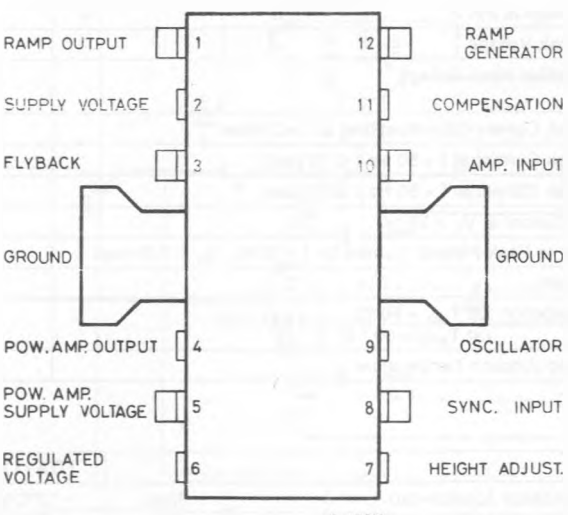
FIN DIP 12

ORDER CODES : TDA1170S

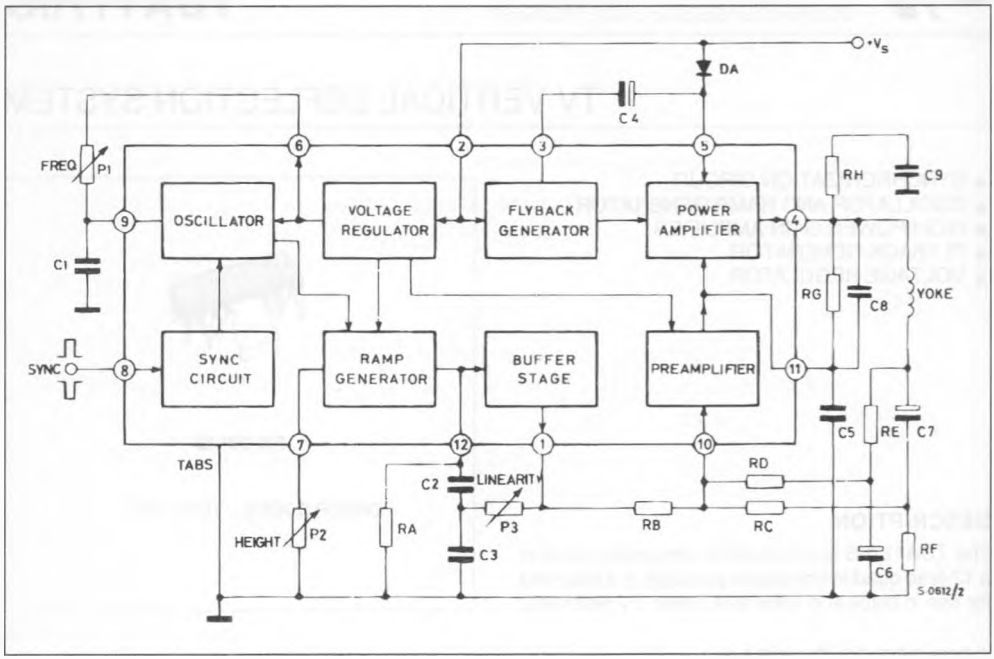
DESCRIPTION

The TDA1170S is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

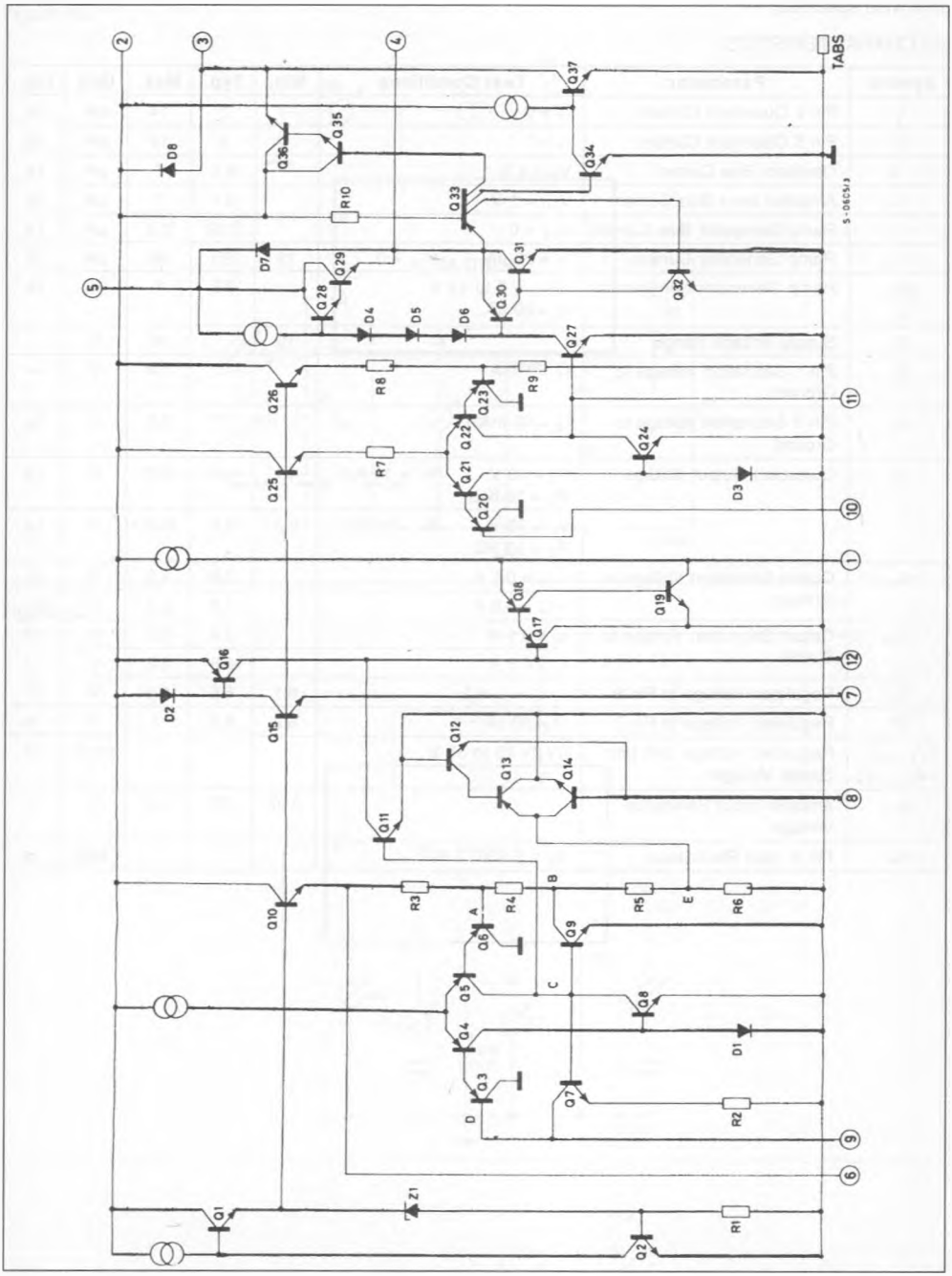
Symbol	Parameter		Value	Unit
V_S	Supply Voltage at Pin 2		35	V
V_4, V_5	Flyback Peak Voltage		60	V
V_{10}	Power Amplifier Input Voltage		+ 10 − 0.5	V V
I_o	Output Peak Current (non repetitive) at t = 2 msec		2	A
I_o	Output Peak Current at f = 50 Hz t ≤ 10 µsec		2.5	A
I_o	Output Peak Current at f = 50 Hz t > 10 µsec		1.5	A
I_3	Pin 3 DC Current at $V_4 < V_2$		100	mA
I_3	Pin 3 Peak to Peak Flyback Current for f = 50 Hz, $t_{fly} \leq 1.5$ msec		1.8	A
I_8	Pin 8 Current		± 20	mA
P_{tot}	Power Dissipation : at T_{tab} = 90 °C at T_{amb} = 80 ° C	TDA1170S	5 1	W W
T_{stg}, T_j	Storage and Junction Temperature		− 40 to 150	°C

THERMAL DATA

			TDA1170S	TDA1170SH
$R_{th\ j-tab}$	Thermal Resistance Junction–tab	Max	12°C/W	10°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	70°C/W(*)	80°C/W

(*) Obtained with tabs soldered to printed circuit with minimized copper area.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (refer to the test circuits, V_s = 35 V, T_{amb} = 25 °C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_5	Pin 5 Quiescent Current	$I_4 = 0$		8	15	mA	1b
$-I_9$	Oscillator Bias Current	$V_9 = 1$ V		0.1	1	µA	1a
$-I_{10}$	Amplifier Input Bias Current	$V_{10} = 1$ V		0.1	1	µA	1b
$-I_{12}$	Ramp Generator Bias Current	$V_{12} = 0$		0.02	0.3	µA	1a
$-I_{12}$	Ramp Generator Current	$I_7 = 20$ µA $V_{12} = 0$	19	20	24	µA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp Generator Non-linearity	$\Delta V_{12} = 0$ to 12 V $I_7 = 20$ µA		0.2	1	%	1b
V_s	Supply Voltage Range		10		36	V	–
V_1	Pin 1 Saturation Voltage to Ground	$I_1 = 1$ mA		1	1.4	V	–
V_3	Pin 3 Saturation Voltage to Ground	$I_3 = 10$ mA		1.7	2.6	V	1a
V_4	Quiescent Output Voltage	$V_s = 10$ V $R_1 = 10$ KΩ $R_2 = 10$ KΩ	4.1	4.4	4.75	V	1a
		$V_s = 35$ V $R_1 = 30$ KΩ $R_2 = 10$ KΩ	8.3	8.8	9.45	V	1a
V_{4L}	Output Saturation Voltage to Ground	$-I_4 = 0.1$ A		0.9	1.2	V	1c
		$-I_4 = 0.8$ A		1.9	2.3	V	1c
V_{4H}	Output Saturation Voltage to Supply	$I_4 = 0.1$ A		1.4	2.1	V	1d
		$I_4 = 0.8$ A		2.8	3.2	V	1d
V_6	Regulated Voltage at Pin 6		6.1	6.5	6.9	V	1b
V7	Regulated Voltage at Pin 7	$I_7 = 20$ µA	6.2	6.6	7	V	1b
$\frac{\Delta V_6}{\Delta V_s}$. $\frac{\Delta V_7}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_s = 10$ to 35 V		1		mV/V	1b
V_{10}	Amplifier Input Reference Voltage		2.07	2.2	2.3	V	–
R_8	Pin 8 Input Resistance	$V_8 \leq 0.4$ V	1			MΩ	1a

Figure 1 : DC Test Circuit.

Figure 1a.

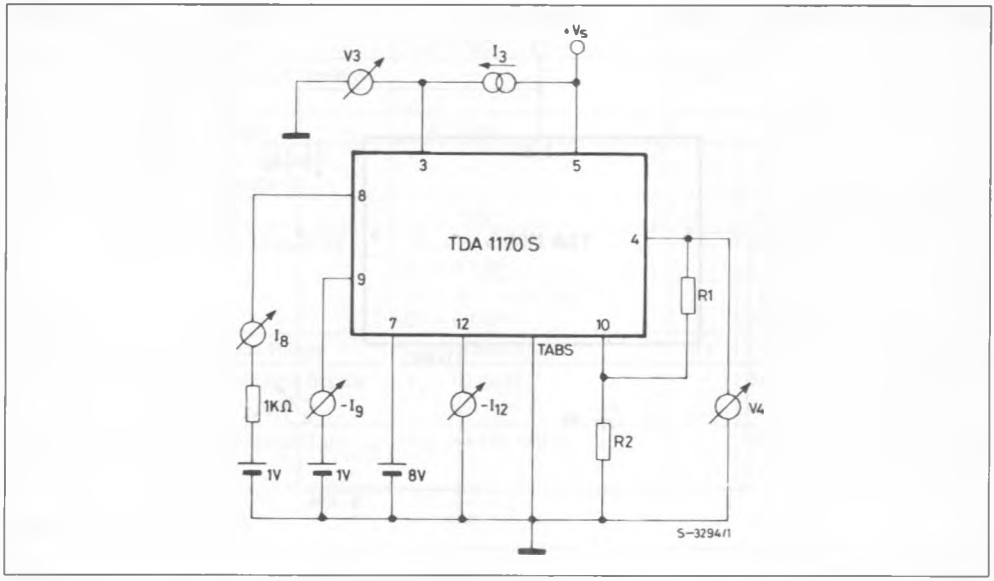


Figure 1b.

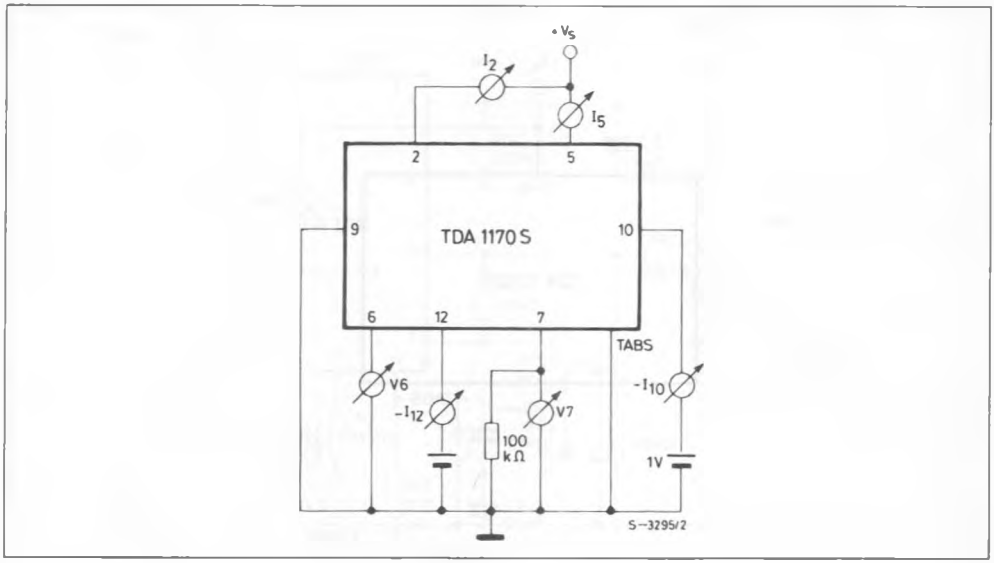


Figure 1c.

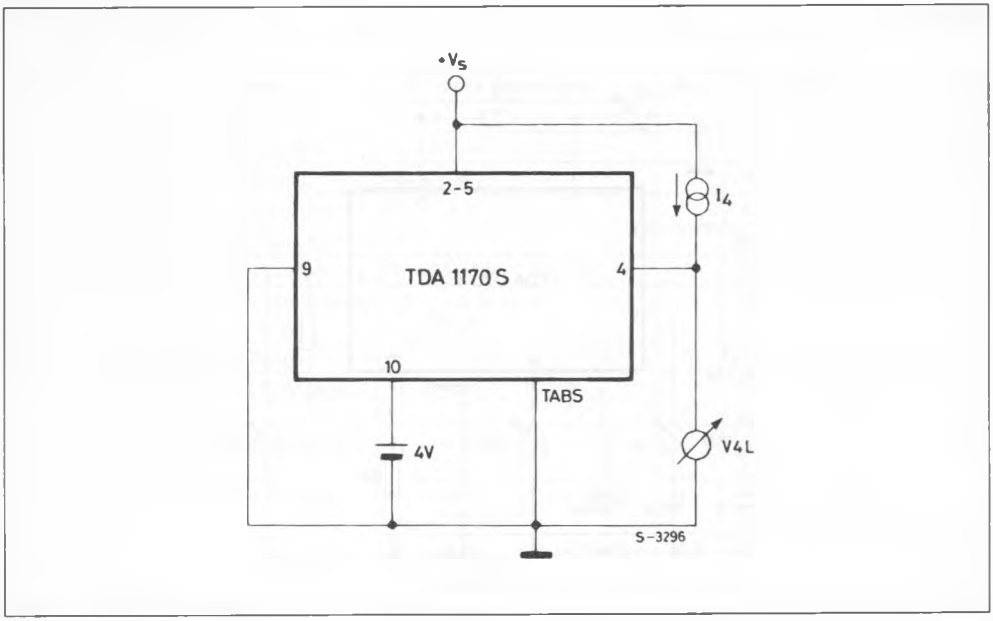
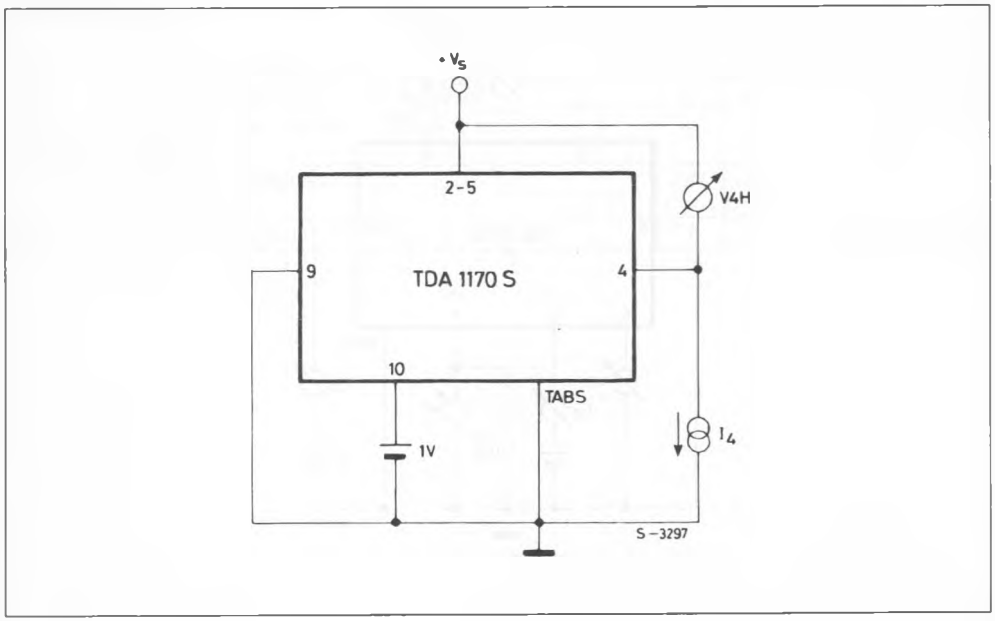


Figure 1d.



AC CHARACTERISTICS (refer to the test circuit, V_s = 25 V; f = 50 Hz ; T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_s	Supply Current	I_y = 1 App		140		mA	2
I_8	Sync. Input Current (positive or negative)		500			µA	2
V_4	Flyback Voltage	I_y = 1 App		51		V	2
V_9	Peak to Peak Oscillator Sawtooth Voltage			2.4		V	2
t_{fly}	Flyback Time	I_y = 1 App		0.7		ms	2
f_o	Free Running Frequency	$(P_1 + R_1)$ = 300 KΩ C_2 = 0.1 µF		42.2		Hz	2
		$(P_1 + R_1)$ = 260 KΩ C_2 = 0.1 µF		52 48.5		Hz	2
Δf	Synchronization Range	I_8 = 0.5 mA	14			Hz	2
$\frac{\Delta f}{\Delta Vs}$	Frequency Drift with Supply Voltage	V_s = 10 to 35 V		0.005		Hz/V	2
$\left\lvert\frac{\Delta f}{\Delta T_{tab}}\right\rvert$	Frequency Drift with Tab Temperature	T_{tab} = 40 to 120 °C		0.01		Hz/°C	2

Figure 2 : AC Test Circuit.

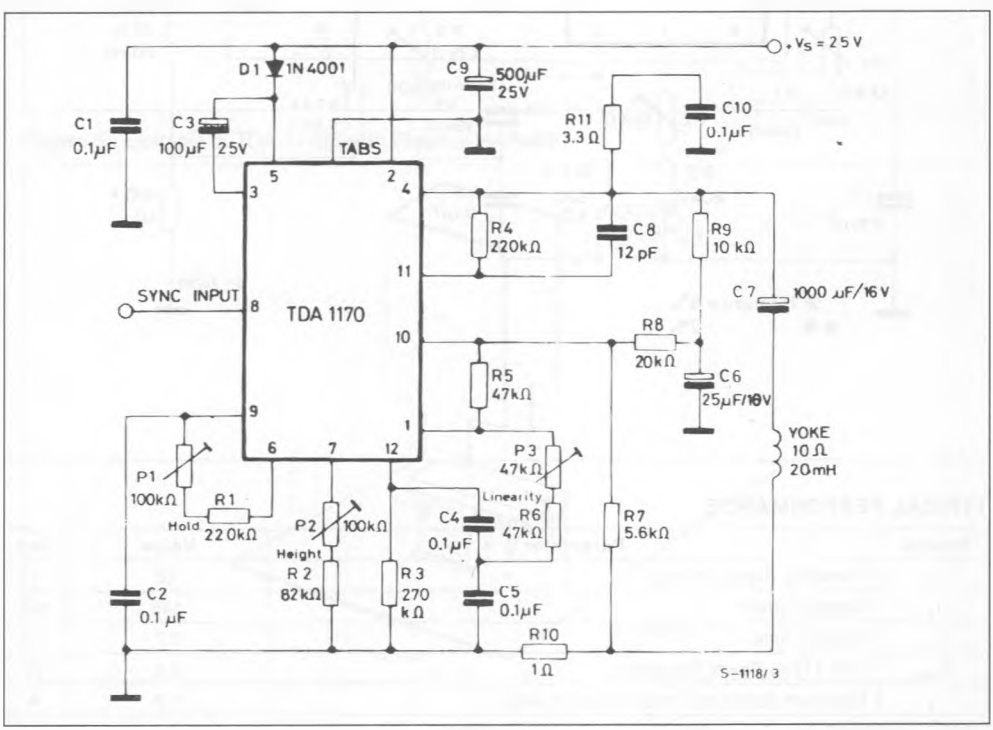
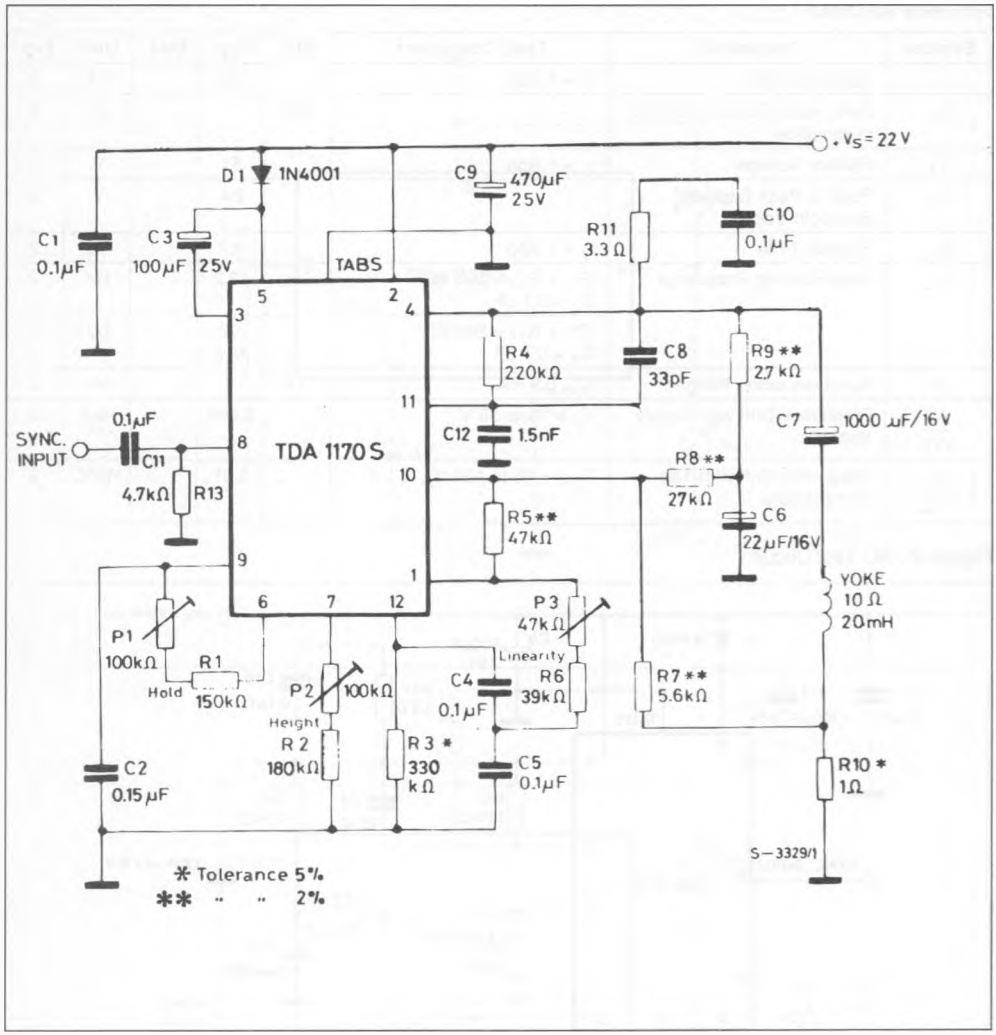


Figure 3 : Typical Application Circuit for Large Screen B/W TV SET (R_y = 10 Ω, L_y = 20 mH, I_y = 1 App).



TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	22	V
I_s	Supply Current	145	mA
t_{fly}	Flyback Time	0.7	ms
P_{tot}	TDA 1170S Power Dissipation	2.3	W
I_y	Maximum Scanning Current (peak to peak)	1.2	A

For safe working up to T_{amb} = 60 °C a heatsink of R_{th} = 14 °C/W is required.

TDA1170S

The junction to ambient thermal resistance of the TDA 1170S can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 4) or to an external heatsink (fig. 5).

The diagram of fig. 6 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "s" of two equal square copper areas having a thickness of 35 µ (1.4 mil).

Figure 4 : Example of P.C. Board Copper Area is Used as Heatsink.

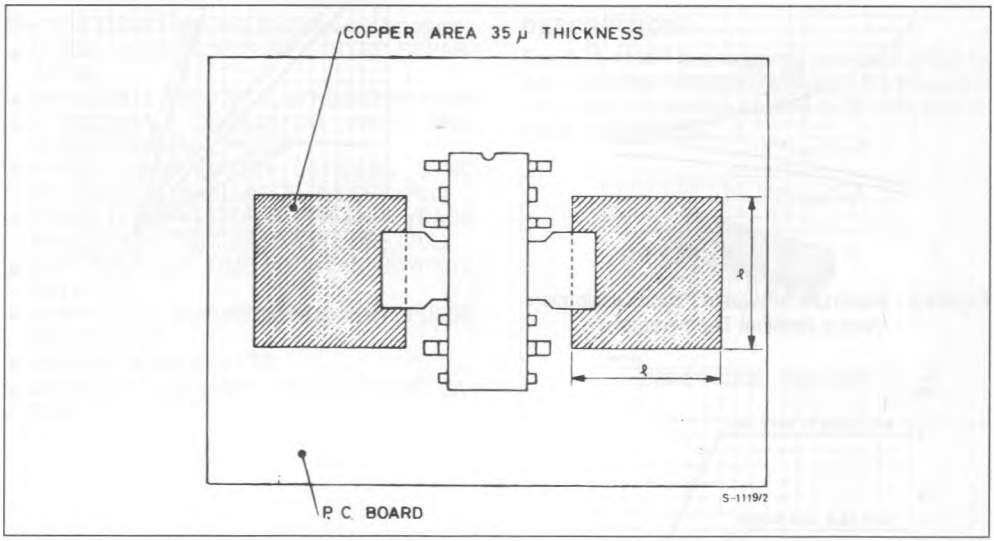


Figure 5 : Example of TDA 1170S with External Heatsink.

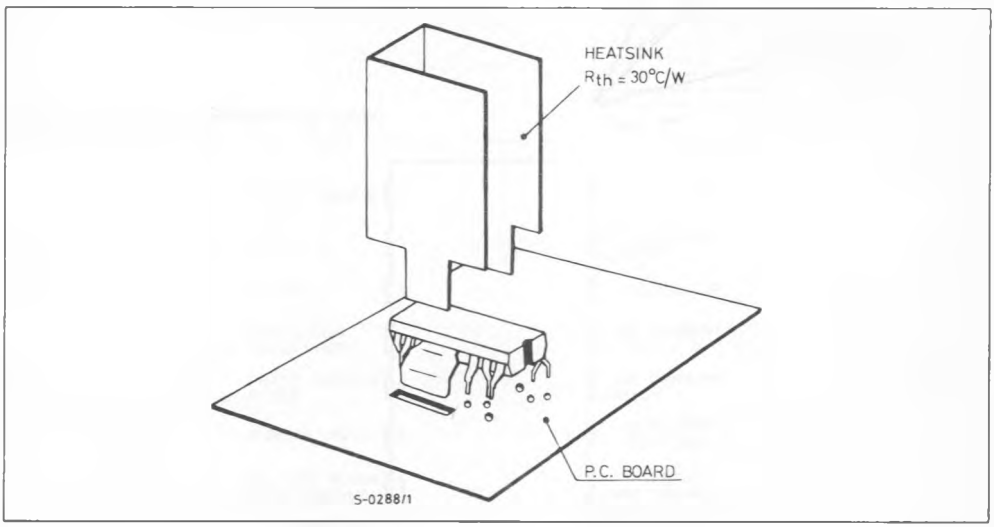


Figure 6 : Maximum Power Dissipation and Junctional-ambient Thermal Resistance vs. "S".

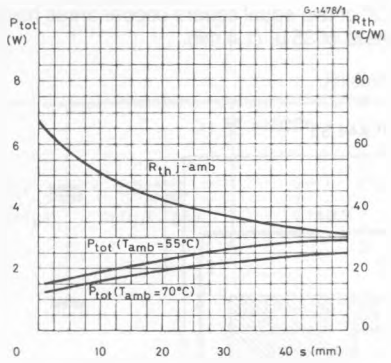


Figure 7 : Maximum Allowable Power Dissipation Versus Ambient Temperature.

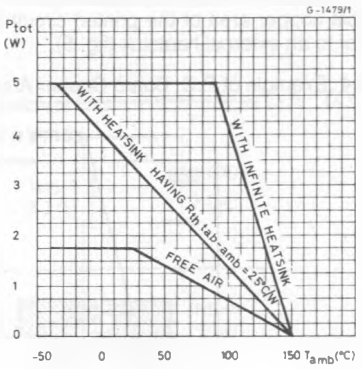


Figure 8 : Maximum Allowable Power Dissipation Versus Ambient Temperature.