

DATA SHEET

TDA4882

Advanced monitor video controller
for OSD

Product specification
Supersedes data of December 1994
File under Integrated Circuits, IC02

1997 Sep 04

Advanced monitor video controller for OSD**TDA4882**

CONTENTS

1	FEATURES
2	GENERAL DESCRIPTION
3	QUICK REFERENCE DATA
4	ORDERING INFORMATION
5	BLOCK DIAGRAM
6	PINNING
7	FUNCTIONAL DESCRIPTION
7.1	General
7.2	Brightness control
7.3	Contrast control
7.4	Output stages
7.5	Input clamping
7.6	Vertical blanking
7.7	Horizontal blanking
7.8	Cut-off and black-level stabilization
7.9	On Screen Display
7.10	Test mode
8	LIMITING VALUES
9	THERMAL CHARACTERISTICS
10	CHARACTERISTICS
11	APPLICATION AND TEST INFORMATION
11.1	Recommendations for building the application board
12	INTERNAL PIN CONFIGURATION
13	PACKAGE OUTLINE
14	SOLDERING
14.1	Introduction
14.2	Soldering by dipping or by wave
14.3	Repairing soldered joints
15	DEFINITIONS
16	LIFE SUPPORT APPLICATIONS

Advanced monitor video controller for OSD

TDA4882

1 FEATURES

- 85 MHz video controller
- Fully DC controllable
- 3 separate video channels
- Input black-level clamping
- White level adjustment for 2 channels only
- Brightness control with correct grey scale tracking
- Contrast control for all 3 channels simultaneously
- Cathode feedback to internal reference for cut-off control, which allows unstabilized video supply voltage
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch-off input for screen protection
- Sync on green operation possible
- On Screen Display (OSD) facility.

2 GENERAL DESCRIPTION

The TDA4882 is an RGB pre-amplifier for colour monitor systems with SVGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT.

With special advantages the circuit can be used in conjunction with the TDA485x monitor deflection IC family.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		7.2	8.0	8.8	V
I_P	supply current		36	48	60	mA
$V_{i(b-w)}$	input voltage, black-to-white		–	0.7	1.0	V
$V_{o(b-w)}$	output voltage, black-to-white	nominal contrast; channels 1 and 3 gain control pins open-circuit	–	0.79	–	V
$I_{o(b-w)}$	output current, black-to-white		–	50	–	mA
I_{OM}	peak output current		–	–	100	mA
B	bandwidth	–3 dB	70	85	–	MHz
G_{nom}	nominal voltage gain	nominal contrast; channels 1 and 3 gain control pins open-circuit	–	1	–	dB
ΔG	gain control difference for 2 channels	relative to G_{nom}	–5	–	+2.6	dB
$CR_{contrast}$	contrast control	$V_{i(CC)} = 1$ to 6 V	–22	–	+3.4	dB
$C_{OSD(min)}$	minimum contrast for OSD	$V_{i(CC)} = 0.7$ V	–	–40	–	dB
ΔV_{bl}	brightness control related to nominal output signal amplitude		–11	–	+34	%
T_{amb}	operating ambient temperature		–20	–	+70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4882	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1

Advanced monitor video controller for OSD

TDA4882

5 BLOCK DIAGRAM

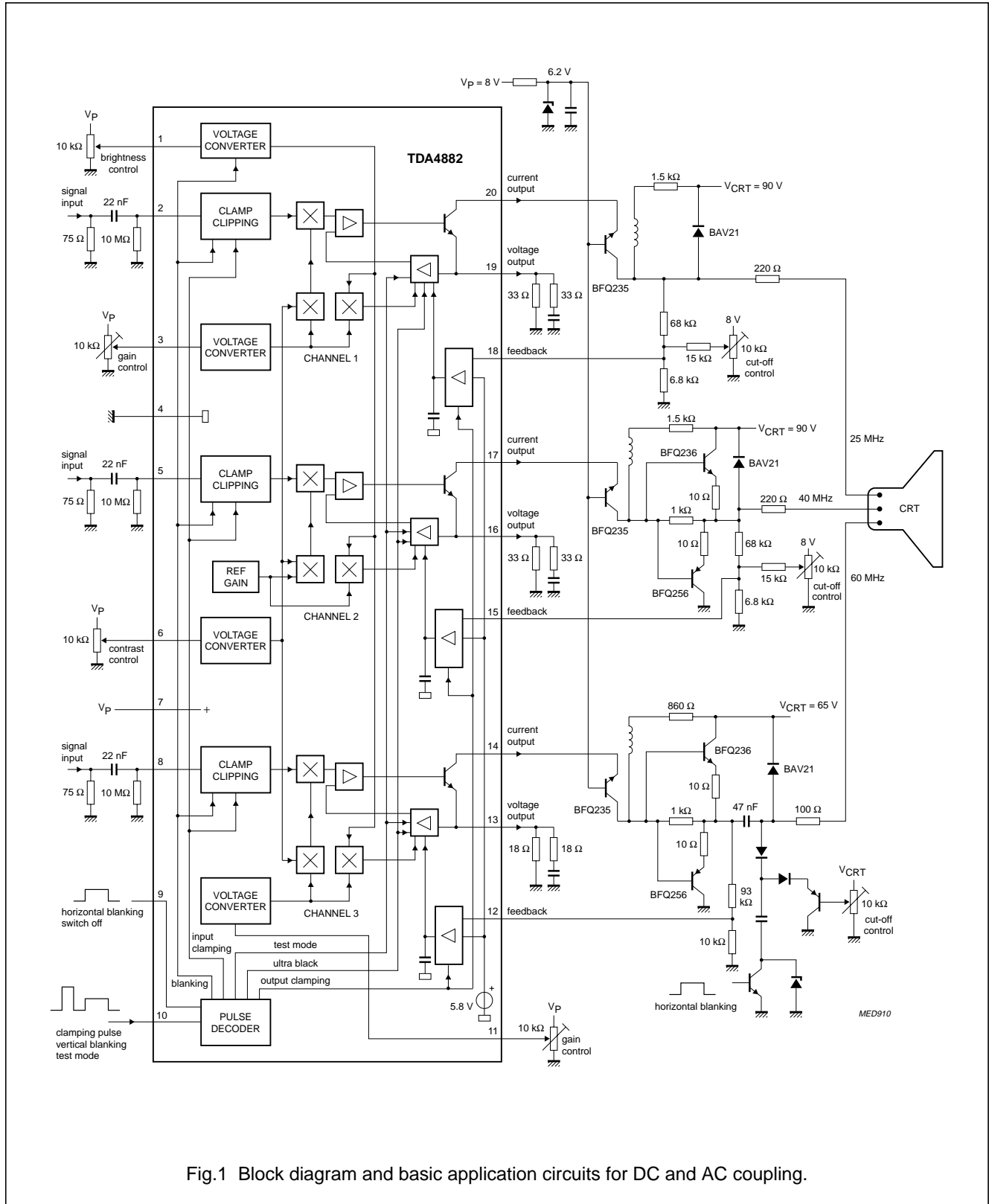


Fig.1 Block diagram and basic application circuits for DC and AC coupling.

Advanced monitor video controller for OSD

TDA4882

6 PINNING

SYMBOL	PIN	DESCRIPTION
BC	1	brightness control
VIN1	2	signal input channel 1
GC1	3	gain control channel 1
GND	4	ground
VIN2	5	signal input channel 2
CC	6	contrast control, OSD switch
V _P	7	supply voltage
VIN3	8	signal input channel 3
HBL	9	horizontal blanking, switch-off
CL	10	input clamping, vertical blanking, test mode
GC3	11	gain control channel 3
FB3	12	feedback channel 3
VOUT3	13	voltage output channel 3
IOUT3	14	current output channel 3
FB2	15	feedback channel 2
VOUT2	16	voltage output channel 2
IOUT2	17	current output channel 2
FB1	18	feedback channel 1
VOUT1	19	voltage output channel 1
IOUT1	20	current output channel 1

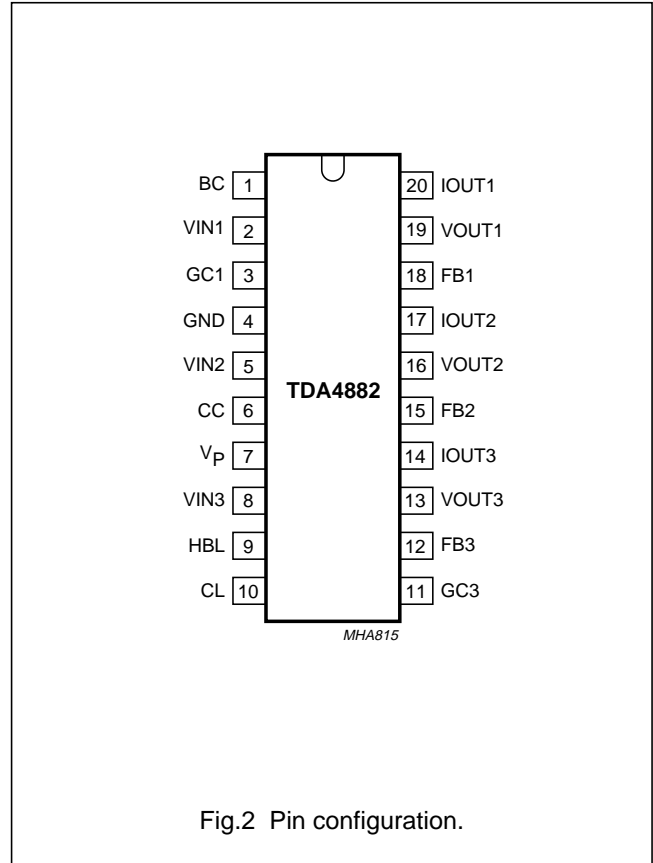


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 General

Figure 4 illustrates the signal processing. The RGB input signals 0.7 V (p-p) are capacitively coupled into the TDA4882 from a low ohmic source and are clamped to an internal DC voltage (artificial black level). Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. Channels 1 and 3 have a maximum total voltage gain of 7 dB (maximum contrast and maximum individual channel gain), channel 2 having 4.4 dB (maximum contrast and nominal gain). With the nominal channel gain of 1 dB and nominal contrast setting the nominal black-to-white output signal is 0.79 V (p-p). Brightness, contrast and gain control is by DC voltage.

7.2 Brightness control

Brightness control (Fig.4) yields a simultaneous signal black-level shift of the three channels relative to a reference black level.

For nominal brightness (pin 1 open-circuit) the signal black level is equal to the reference black level.

7.3 Contrast control

Contrast is voltage controlled to affect the three channels simultaneously (Fig.4). To provide the correct white point, individual gain controls adjust the signals of channels 1 and 3 relative to the reference channel 2. Gain setting also changes contrast to achieve correct grey scale tracking.

7.4 Output stages

The output stages provide both voltage and current outputs. External cascode transistors reduce power consumption of the IC and prevent breakdown of the output transistors. Signal output currents and peaking characteristics are determined by external components at the voltage outputs and the video supply. The channels have separate internal feedback loops which ensure large signal linearity and marginal signal distortion irrespective of output transistor thermal V_{BE} variation (Fig.8).

Advanced monitor video controller for OSD

TDA4882

7.5 Input clamping

The clamping pulse (Fig.17) is for input clamping only. The input signals are at black level during the clamping pulse and are clamped to an internal artificial black level. The coupling capacitors provide black-level storage. The threshold for the clamping pulse is higher than that for vertical blanking, therefore, the rise and fall times of the clamping pulse need to be faster than 75 ns/V during transition from 1 to 3.5 V.

7.6 Vertical blanking

The vertical blanking pulse (Fig.17) will be detected if the input voltage is higher than the threshold voltage for approximately 320 ns but does not exceed the threshold for the clamping pulse in the time between. During the vertical blanking pulse the input clamping is disabled to avoid misclamping in the event of composite input signals. The input signal is blanked and the artificial black level is inserted instead. Also the brightness is set internally to its nominal value, thus the output signal is at reference black level. The DC value of the reference black level will be adjusted by cut-off stabilization.

7.7 Horizontal blanking

During horizontal blanking (Fig.18) the output signal is set to reference black level and output clamping is activated. If the voltage exceeds the switch-off threshold, the signal is blanked and switched to ultra-black level for screen protection and spot suppression during V-flyback.

Ultra-black level is the lowest possible channel output voltage and is not dependent on cut-off stabilization.

7.8 Cut-off and black-level stabilization

For cut-off stabilization (DC coupling to the CRT) and black-level stabilization (AC coupling) the video signal at the cathode or the coupling capacitor is divided by an adjustable voltage divider and fed to the channel feedback inputs. During horizontal blanking time this signal is compared with an internal DC voltage of approximately 5.8 V. Any difference will lead to a reference black-level correction by charging or discharging the integrated capacitor which stores the reference black-level information between the horizontal blanking pulses.

7.9 On Screen Display

For OSD (Fig.3), fast switching of control pin 6 to less than 1 V (e.g. 0.7 V) blanks the input signals. The OSD signals can easily be inserted to the external cascode transistor.

7.10 Test mode

During test mode (pins 9 and 10 connected to V_p) the black levels at the channel voltage outputs are set internally to typical 0.7 V with nominal brightness and 3 V DC at channel signal inputs.

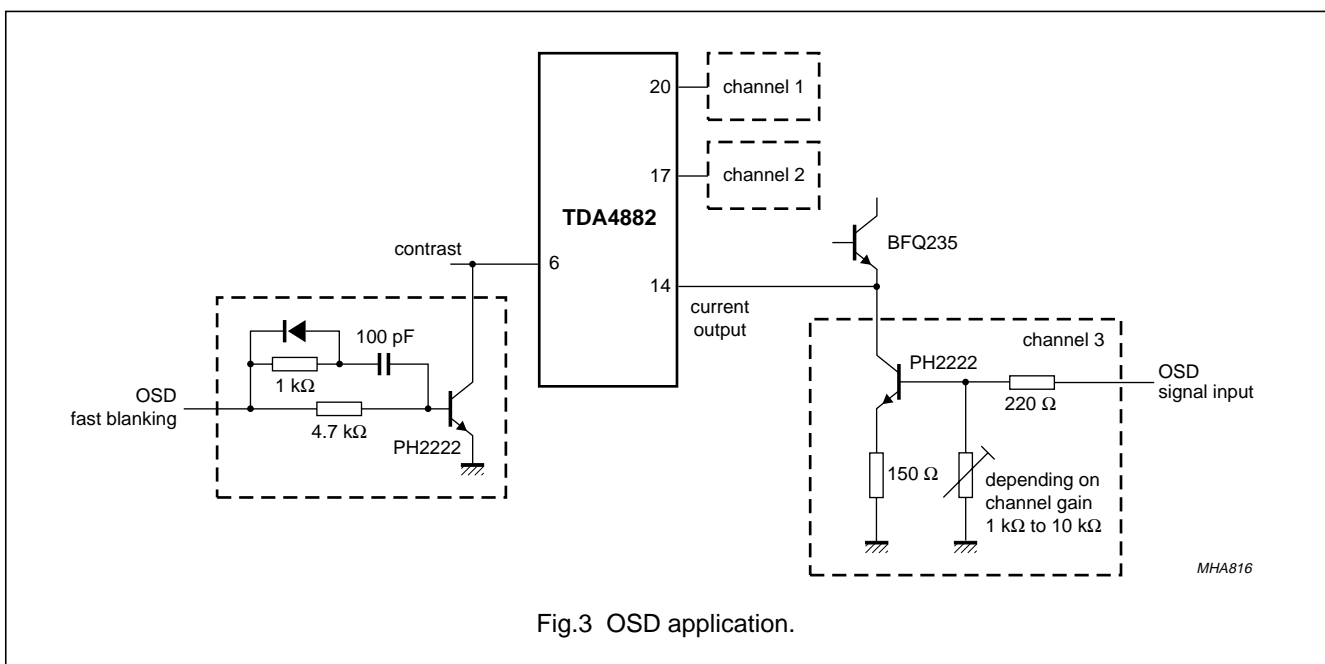


Fig.3 OSD application.

Advanced monitor video controller for OSD

TDA4882

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{ext}	external DC voltage applied to the following pins:			
	pin 7 (V_P)	0	8.8	V
	pins 2, 5 and 8 (signal inputs)	-0.1	V_P	V
	pins 20, 17 and 14 (current outputs)	-0.1	V_P	V
	pins 12, 15 and 18 (channel feedback inputs)	-0.1	+0.7	V
	pins 1, 6, 3 and 11 (brightness, contrast and gain control inputs)	-0.1	V_P	V
	pin 9 (horizontal blanking input)	-0.1	$V_P + 0.7$	V
	pin 10 (input clamping input)	-0.1	$V_P + 0.7$	V
$I_{o(\text{av})}$	average output current (pins 20, 17 and 14); note 1	0	50	mA
I_{OM}	peak output current (pins 20, 17 and 14)	0	100	mA
P_{tot}	total power dissipation	-	1200	mW
T_{stg}	storage temperature	-25	+150	°C
T_{amb}	operating ambient temperature	-20	+70	°C
T_j	junction temperature	-25	+150	°C
V_{ESD}	electrostatic handling for all pins; note 2	-500	+500	V

Notes

- Signal amplitude of 50 mA black-to-white is possible if the average current (including blanking times and signal variation against time) does not exceed 50 mA. The maximum power dissipation of 1200 mW has to be considered.
- Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{\text{th}(j-a)}$	thermal resistance from junction to ambient	in free air	65	K/W

Advanced monitor video controller for OSD

TDA4882

10 CHARACTERISTICS

$V_P = 8.0\text{ V}$; $T_{amb} = 25\text{ °C}$; all voltages measured to GND (pin 4); note 1; see Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		7.2	8.0	8.8	V
I_P	supply current		36	48	60	mA
Video signal inputs (channels 1, 2 and 3)						
$V_{i(b-w)}$	input voltage, black-to-white		–	0.7	1.0	V
$V_{i(\text{clamp})}$	DC voltage during input clamping (artificial black + V_{BE})		2.8	3.1	3.4	V
I_i	DC input current	no clamping; $V_i = V_{i(\text{clamp})}$; $T_{amb} = -20\text{ to }+70\text{ °C}$	–0.05	+0.05	+0.25 0	μA
		during clamping; $V_i = V_{i(\text{clamp})} + 0.7\text{ V}$	50	75	120	μA
		during clamping; $V_i = V_{i(\text{clamp})} - 0.7\text{ V}$	–120	–75	–50	μA
Brightness control; note 2; Fig.5						
$V_{i(BC)}$	input voltage		1.0	–	6.0	V
$R_{i(BC)}$	input resistance		40	50	60	k Ω
$V_{i(BC)(nom)}$	input voltage for nominal brightness	pin 1 open-circuit	2.0	2.25	2.5	V
ΔV_{bl}	black-level voltage change at voltage outputs referred to reference black level during output clamping ($V_{i(HBL)} > 1.6\text{ V}$) related to output signal amplitude with nominal 0.7 V (p-p) input signal and nominal contrast ($V_{i(CC)} = 4.3\text{ V}$) for any gain setting	$V_{i(BC)} = 1.0\text{ V}$	–13	–11	–9.5	%
		$V_{i(BC)} = 6.0\text{ V}$	30	34	37	%
		pin 1 open-circuit	–	–	0.8	%
ΔV_{BT}	difference of ΔV_{bl} between any two channels		–1.2	0	+1.2	%
Contrast control; note 3; Fig.6						
$V_{i(CC)}$	input voltage		1.0	–	6.0	V
$V_{i(CC)(max)}$	maximum input voltage		–	–	$V_P - 1$	V
$V_{i(CC)(nom)}$	input voltage for nominal contrast	note 4	–	4.3	–	V
$I_{i(CC)}$	input current	$V_{i(CC)} = 4.3\text{ V}$	–5	–1	–0.1	μA
C/C_{nom}	contrast relative to nominal contrast	$V_{i(CC)} = 6.0\text{ V}$; pins 3 and 11 open-circuit	2.4	3.4	–	dB
		$V_{i(CC)} = 1.0\text{ V}$; pins 3 and 11 open-circuit	–26	–22	–19	dB
$V_{i(CC)(min)}$	input voltage for minimum contrast	pins 3 and 11 open-circuit	–	0.7	–	V
ΔG_{track}	tracking of output signals of channels 1, 2 and 3	$1\text{ V} < V_{i(CC)} < 6\text{ V}$; note 5	–	0	0.5	dB
$t_{df(C)}$	delay between leading (falling) edges of contrast voltage and voltage output waveforms	$V_{i(CC)} = 4.3\text{ V to }0.7\text{ V}$; input fall time at pin 6: $t_{f(CC)} = 2\text{ ns}$; note 6; Fig.10	–	7	20	ns

Advanced monitor video controller for OSD

TDA4882

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{dr(C)}$	delay between trailing edges (rising) of contrast voltage and voltage output waveforms	$V_{i(CC)} = 0.7 \text{ V to } 4.3 \text{ V}$; input rise time at pin 6: $t_{r(CC)} = 2 \text{ ns}$; note 6; Fig.10	–	15	25	ns
$t_{f(C)}$	fall time of voltage output waveform	90% to 10% amplitude; input fall time at pin 6: $t_{f(CC)} = 2 \text{ ns}$; note 6; Fig.10	–	6	15	ns
$t_{r(C)}$	rise time of voltage output waveform	10% to 90% amplitude; input rise time at pin 6: $t_{r(CC)} = 2 \text{ ns}$; note 6; Fig.10	–	6	15	ns
Gain control (channel 1 and channel 3); note 7; Fig.7						
$V_{i(GC)}$	input voltage		1.0	–	6.0	V
$V_{i(GC)(nom)}$	input voltage for nominal gain	pins 3 and 11 open-circuit	3.6	3.75	3.95	V
$R_{i(GC)}$	input resistance		44	55	66	k Ω
ΔG	gain control difference relative to nominal gain (channels 1 and 3 only)	$V_{i(CC)} = 4.3 \text{ V}$; $V_{i(GC)} = 6 \text{ V}$	2	2.6	3.3	dB
		$V_{i(CC)} = 4.3 \text{ V}$; $V_{i(GC)} = 1 \text{ V}$	–5.5	–5	–4.5	dB
Feedback input (channels 1, 2 and 3); note 8; Fig.8						
$V_{ref(int)}$	internal reference voltage		5.6	5.8	6.1	V
$I_{o(FB)(max)}$	maximum output current	during output clamping; $V_{i(FB)} = 3 \text{ V}$	–500	–100	–60	nA
$\Delta V_{bl(CRT)}$	black-level variation at CRT	note 9	0	40	200	mV
$\Delta V_{ref(T)}$	variation of $V_{ref(int)}$ in the temperature range	$T_{amb} = -20 \text{ to } +70 \text{ }^\circ\text{C}$	0	20	50	mV
$\Delta V_{ref(int)(VP)}$	variation of $V_{ref(int)}$ with supply voltage	$7.2 \text{ V} \leq V_P \leq 8.8 \text{ V}$	0	60	100	mV
Voltage outputs (channels 1, 2 and 3)						
$V_{o(b-w)(nom)}$	nominal signal output voltage (black-to-white value)	pins 3 and 11 open-circuit; $V_{i(CC)} = 4.3 \text{ V}$; $V_{i(b-w)} = 0.7 \text{ V}$	0.69	0.79	0.89	V
$V_{blx(max)}$	maximum adjustable black-level voltage	during output clamping; $T_{amb} = -20 \text{ to } +70 \text{ }^\circ\text{C}$	1	1.2	1.4	V
$V_{bl(SO)}$	black-level voltage during switch-off, equal to minimum adjustable black-level voltage	$V_{i(HBL)} = V_P$; $R_O = 33 \text{ } \Omega$; $T_{amb} = -20 \text{ to } +70 \text{ }^\circ\text{C}$	30	45	100	mV
$V_{bl(TST)}$	black-level voltage during test mode	$V_{i(HBL)} = V_P$; $V_{i(CL)} = V_P$; pin 1 open-circuit; $V_i = V_{I(clamp)}$; note 10	0.3	0.7	1.2	V
S/N	signal-to-noise ratio	note 11	–	50	44	dB
$d_{O(th)}$	output thermal distortion	$I_{o(b-w)} = 50 \text{ mA}$; note 12	–	0.6	1	%
$\Delta V_{bl(f)}$	black-level variation between clamping pulses	line frequency 30 kHz	–	0.5	4.5	mV
$V_{offset(max)}$	maximum offset during sync clipping	$V_i < V_{I(clamp)}$; note 13; Fig.9	0	7	15	mV

Advanced monitor video controller for OSD

TDA4882

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta V_{o(b-w)(T)}$	variation of nominal output signal (black-to-white value) with temperature	pins 3 and 11 open-circuit; $V_{i(CC)} = 4.3 \text{ V}$; $V_{i(b-w)} = 0.7 \text{ V}$; $T_{amb} = -20 \text{ to } +70 \text{ }^\circ\text{C}$	0	2.5	10	%
Current outputs (channels 1, 2 and 3); note 14						
$I_{o(b-w)}$	output current (black-to-white value)		–	50	–	mA
		with peaking	–	–	100	mA
$V_{20-19}; V_{17-16}; V_{14-13}$	start of HF-saturation voltage of output transistors	$I_o = 50 \text{ mA}$	–	–	2.0	V
		$I_o = 100 \text{ mA}$	–	–	2.2	V
$I_{bi(SO)}$	output current during switch-off	$V_{i(HBL)} = V_P$; $R_O = 33 \text{ } \Omega$	0	20	900	μA
Frequency response at voltage outputs; note 15; Figs 11, 12 and 13						
$\Delta G_{(f)}$	gain decrease by frequency response	70 MHz; single channel	–	1.3	3	dB
$t_{r(O)}$	rise time at voltage output	10% to 90% amplitude; input rise time = 1 ns	–	4.1	5.0	ns
dV_O	overshoot of output signal pulse related to actual output pulse amplitude	single channel; input rise time = 2.5 ns; $V_{i(b-w)} = 0.7 \text{ V}$; pins 3 and 11 open-circuit; $V_{i(CC)} = 4.3 \text{ V}$	–	4	8	%
Crosstalk at voltage outputs with speed up circuit; note 16; Figs 14, 15 and 16						
$\alpha_{ct(tr)}$	transient crosstalk		–	–	–20	dB
Threshold voltages for clamping, blanking and switch-off; note 17						
$V_{i(HBL)}$	threshold for horizontal blanking (blanking, output clamping)		1.2	1.4	1.6	V
	threshold for switch-off (blanking, minimum black-level, no output clamping)		5.8	6.5	6.8	V
$R_{i(HBL)}$	input resistance	against ground	50	80	110	k Ω
$t_{d(Hblank)}$	delay between horizontal blanking input and output signal blanking	input rise time at pin 9 > 100 ns; note 18; Fig.18	–	40	60	ns
$V_{i(CL)}$	threshold for vertical blanking (blanking, no input clamping)	note 19; Fig.17	1.2	1.4	1.6	V
	threshold for clamping (input clamping, no blanking)	note 19; Fig.17	2.6	3.0	3.5	V
	threshold for test mode (no clamping, no blanking, see $V_{bi(TST)}$ above)	for test mode also $V_{i(HBL)} > 6.8 \text{ V}$ (switch-off)	$V_P - 1$	–	V_P	V
$I_{i(CL)}$	current	$V_{i(CL)} < V_P - 1 \text{ V}$	–3	–1	–	μA
		$V_{i(CL)} \geq V_P - 1 \text{ V}$	–	100	–	μA

Advanced monitor video controller for OSD

TDA4882

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{r(CL)}, t_{f(CL)}$	rise and fall time for clamping pulse	note 19; Fig.17	–	–	75	ns/V
$t_{w(clamp)}$	width of clamping pulse		0.6	–	–	μ s
$t_{d(Vblank)}$	delay between vertical blanking input and internal blanking	note 19; Fig.17	260	320	380	ns

Notes to the characteristics

1. Definition of levels:

- Artificial black level:** internal signal level behind input emitter follower during input clamping and signal clipping. This level is inserted instead of the input signal during blanking.
- Reference black level:** DC voltage during output clamping at voltage outputs, not influenced by brightness, contrast or gain setting, adjustable by cut-off stabilization.
- Cut-off level:** corresponding DC voltage at CRT cathode in closed feedback loop.
- Black level:** actual signal black level at either the voltage outputs or cathode, it can be adjusted by (brightness \times gain), it refers to reference black level or cut-off level.
- Ultra-black level, switch-off level:** lowest adjustable reference black level, lowest signal level at voltage outputs.
- The minimum guaranteed control range for reference black level is 0.1 to 1 V. The ultra-black level is dependent on the external resistor R_O at pins 13, 16 and 19 (voltage outputs) to ground.

$$g) V_{bl(SO)} \approx \frac{R_o}{3.5 \text{ k}\Omega + R_o} \times 4.65 \text{ V}$$

2. Linear control range is 1 to 6 V for $V_{i(BC)}$, independent of supply voltage.

3. Linear control range is 1 to 6 V for $V_{i(CC)}$, independent of supply voltage. Open pin 6 leads to maximum contrast setting. It is recommended not to exceed $V_{i(CC)} = V_P - 1 \text{ V}$ to avoid saturation of internal circuitry. For $V_{i(CC)} < V_{i(CC)(min)} \approx 0.7 \text{ V}$ a small negative signal ($\approx -40 \text{ dB}$) will appear. For frequency dependency of contrast control see note 15.

4. Definition for nominal output signals: input $V_{i(b-w)} = 0.7 \text{ V}$, gain pins 3 and 11 open-circuit, contrast control $V_{i(CC)} = V_{i(CC)(nom)}$.

$$5. \Delta G_{track} = 20 \times \text{maximum of } \left\{ \left| \log \left(\frac{A_1}{A_{10}} \times \frac{A_{20}}{A_2} \right) \right|; \left| \log \left(\frac{A_1}{A_{10}} \times \frac{A_{30}}{A_3} \right) \right|; \left| \log \left(\frac{A_2}{A_{20}} \times \frac{A_{30}}{A_3} \right) \right| \right\} \text{ dB}$$

A_x : signal output amplitude in channel x at any contrast setting between 1 and 6 V.

A_{x0} : signal output amplitude in channel x at nominal contrast and same gain setting.

6. Typical step in contrast voltage and response at signal outputs for nominal input signal $V_{i(b-w)} = 0.7 \text{ V}$ (OSD fast blanking input/output).

7. Linear control range is 1 to 6 V for $V_{i(GC)}$, independent of supply voltage.

8. The internal reference voltage can be measured at pins 18, 15 and 12 (channel feedback inputs) during output clamping ($V_{i(HBL)} = 2 \text{ V}$) in closed feedback loop.

9. Slow variations of video supply voltage V_{CRT} (Fig.1) will be suppressed at CRT cathode by cut-off stabilization. Change of V_{CRT} by 5 V leads to specified change of cut-off voltage.

10. The test mode allows testing without input and output clamping pulses. The signal inputs have to be biased via resistors to the previously measured clamp voltages of approximately 3 V (artificial black level + V_{BE}). Signal and brightness blanking is not possible during test mode. The current outputs should be adjusted by resistors $\gg R_O$ from voltage outputs to a positive voltage (e.g. V_P).

Advanced monitor video controller for OSD

TDA4882

11. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):

$$\frac{S}{N} = 20 \times \log \frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}} \text{ dB}$$

12. Large output swing e.g. $I_{o(b-w)} = 50 \text{ mA}$ leads to signal-dependent power dissipation in output transistors. Thermal V_{BE} variation is compensated.
13. Composite signals will not disturb normal operation because an internal clipping circuit cuts all signal parts below black level.
14. The output current approximately follows the equation $I_o = V_o \left(\frac{1}{R_O} + \frac{1}{2.2 \text{ k}\Omega} \right) - 500 \mu\text{A}$ for $V_o > V_{bl(SO)}$ and with R_O = external resistor at voltage output to ground. The external RC combination (Fig.1) at pins 19, 16 and 13 (voltage outputs) enables peak currents during transients.
15. Frequency response, crosstalk and pulse response have been measured at voltage outputs on a special printed-circuit board with 50Ω line in/out connections and without peaking, see Chapter 11.
16. Crosstalk between any two voltage outputs (e.g. channels 1 and 2).
- Input conditions:** one channel (channel 1) with nominal input signal and minimum rise time. The inputs of the other channels capacitively coupled to ground (channels 2 and 3). Gain pins 3 and 11 open-circuit.
 - Output conditions:** output signal of channel 1 is set by contrast control voltage, to $V_{o(b-w)} = V_{o(VOUT1)} = 0.7 \text{ V}$, the rise time should be 5 ns. Output signal of channel 2 then is $V_{o(b-w)} = V_{o(VOUT2)}$.
 - Transient crosstalk:** $\alpha_{ct(tr)} = 20 \times \log \frac{V_{o(VOUT2)}}{V_{o(VOUT1)}} \text{ dB}$
 - Crosstalk as a function of frequency has been measured without peaking circuit, with nominal input signal and nominal settings.
17. The internal threshold voltages are derived from a stabilized voltage. The internal pulses are generated while the input pulses are higher than the thresholds. Voltages less than -0.1 V at pins 9 and 10 can influence black-level control and should be avoided.
18. The delay between HBL input pulse (horizontal blanking) and output signal blanking pulse and also brightness blanking (ΔV_{bl}), at the voltage outputs, depends on the input rise time of the HBL pulse. The specified values for $t_{d(Hblank)}$ are valid for HBL rise times greater than 100 ns only.
19. For $75 \text{ ns/V} < t_{r(CL)}$, $t_{r(CL)} < 240 \text{ ns/V}$, generation of internal input clamping and blanking pulse is not defined. Pulses not exceeding the threshold of input clamping (typical 3 V) will be detected as blanking pulses.

Advanced monitor video controller for OSD

TDA4882

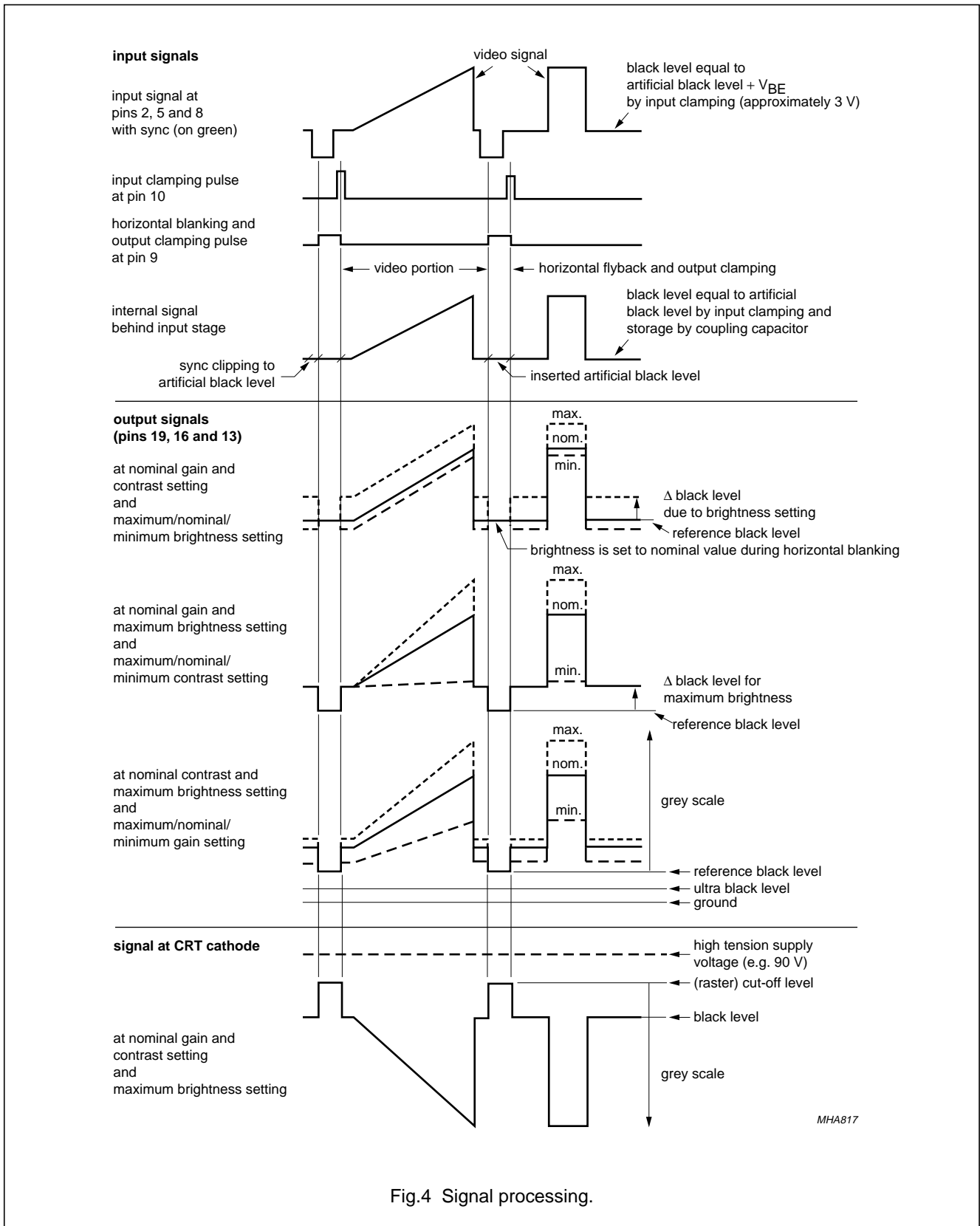
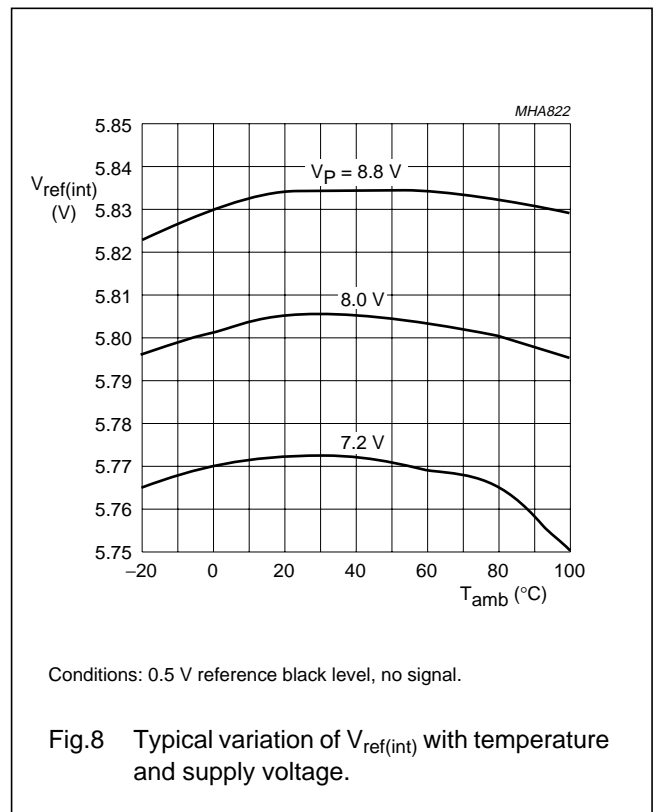
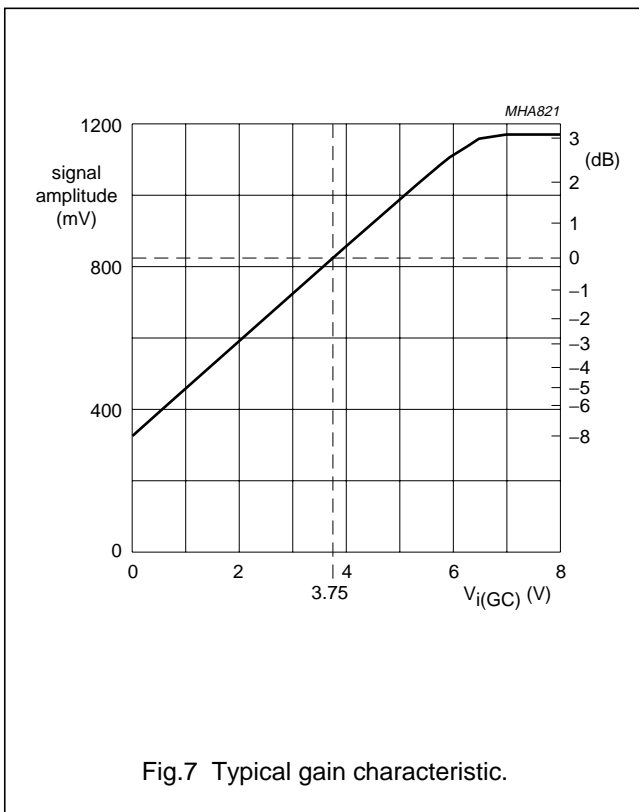
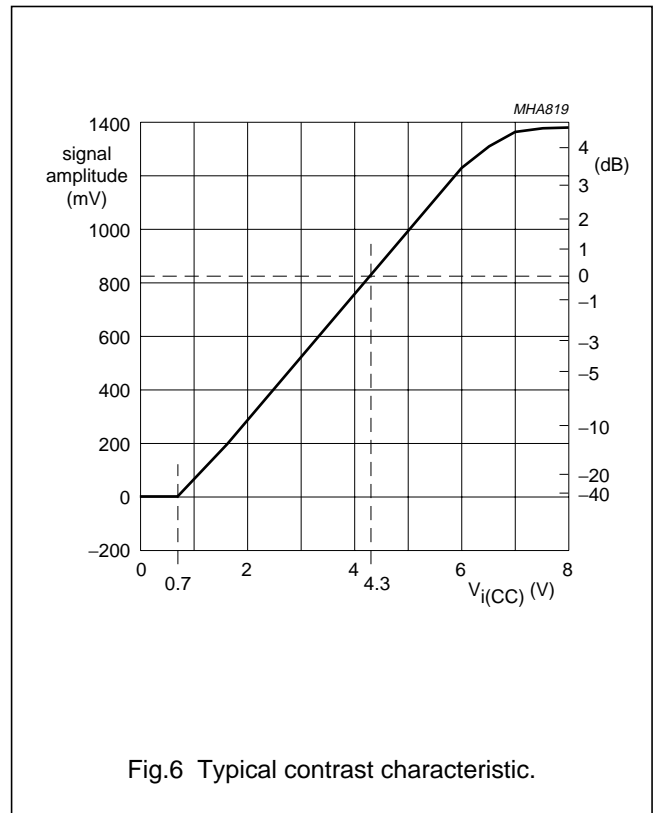
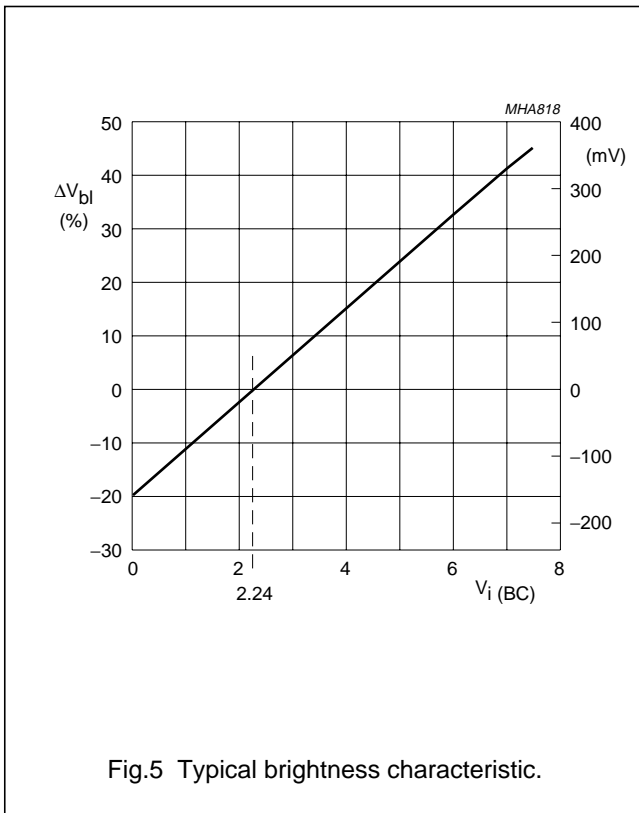


Fig.4 Signal processing.

Advanced monitor video controller for OSD

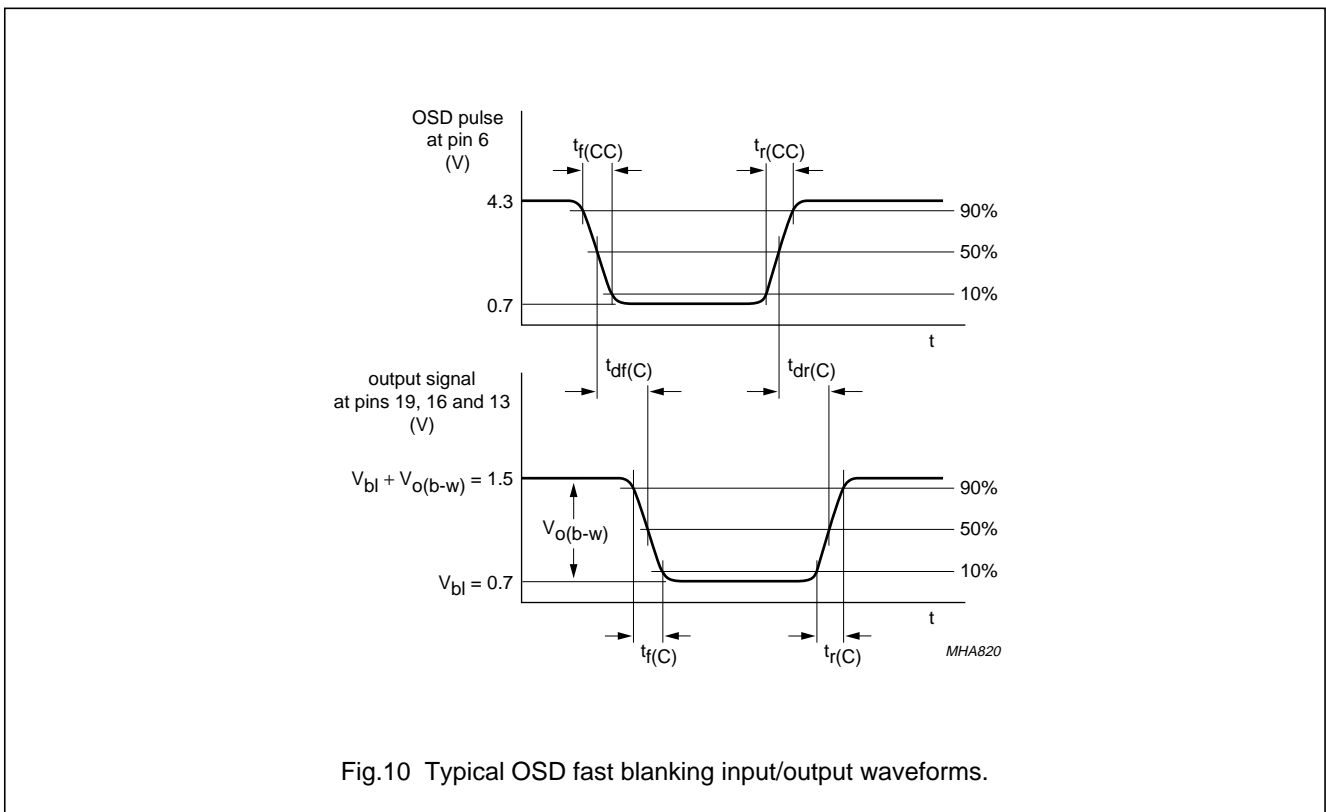
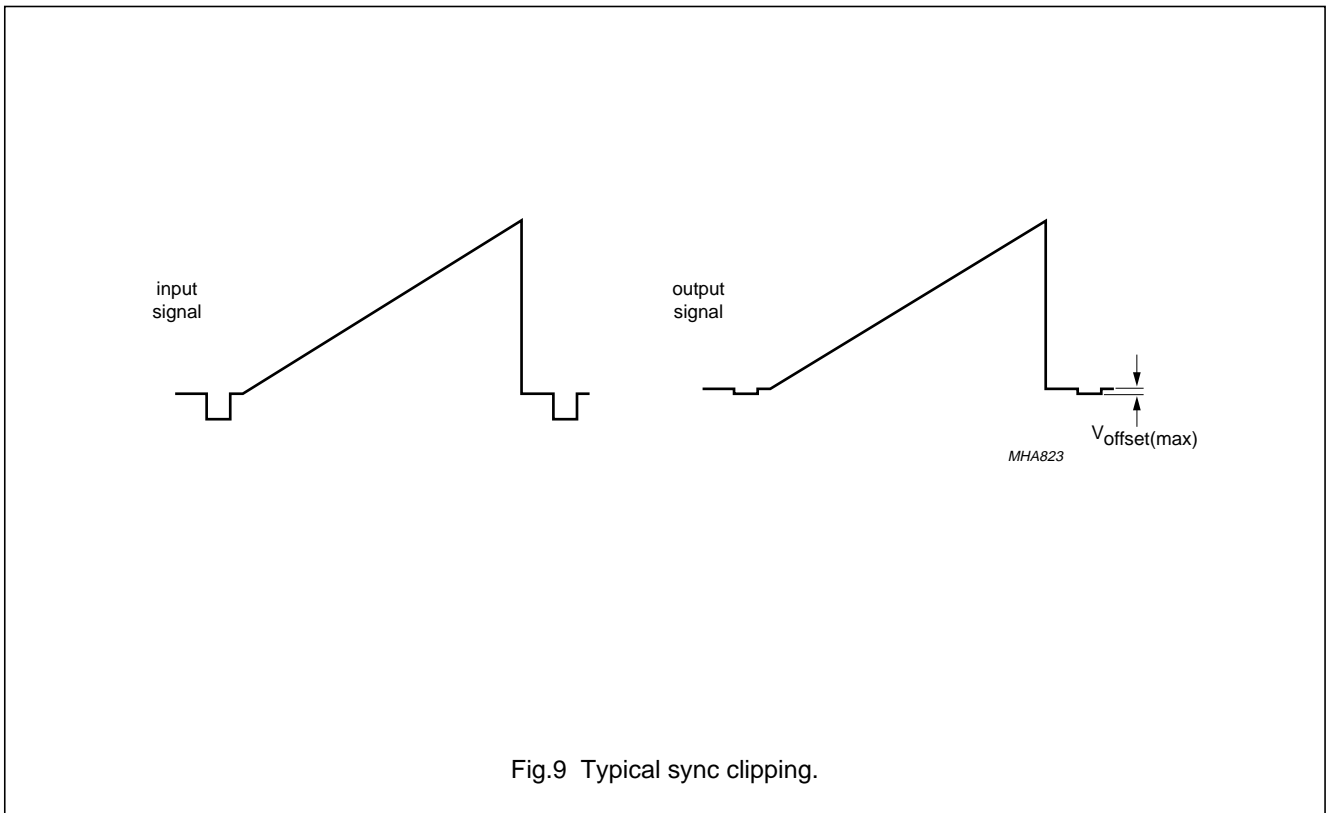
TDA4882



Conditions: 0.5 V reference black level, no signal.

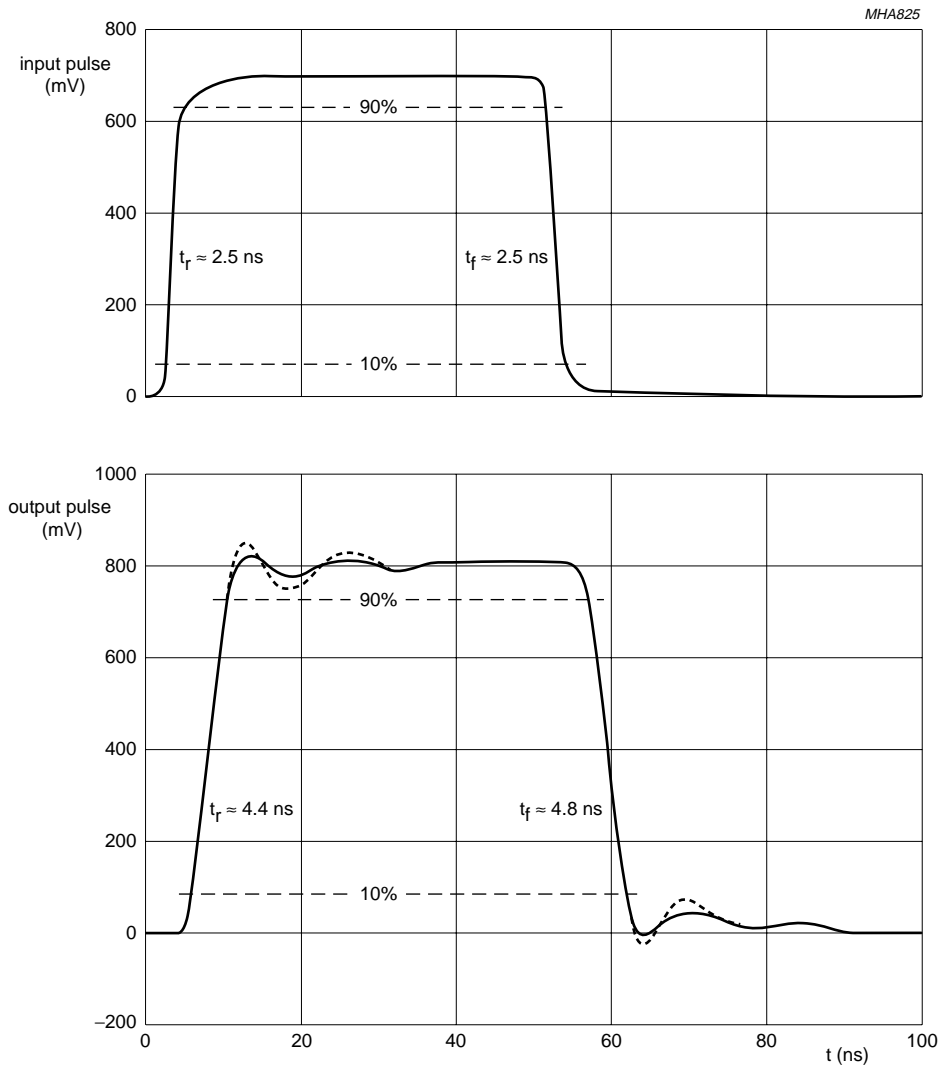
Advanced monitor video controller for OSD

TDA4882



Advanced monitor video controller for OSD

TDA4882

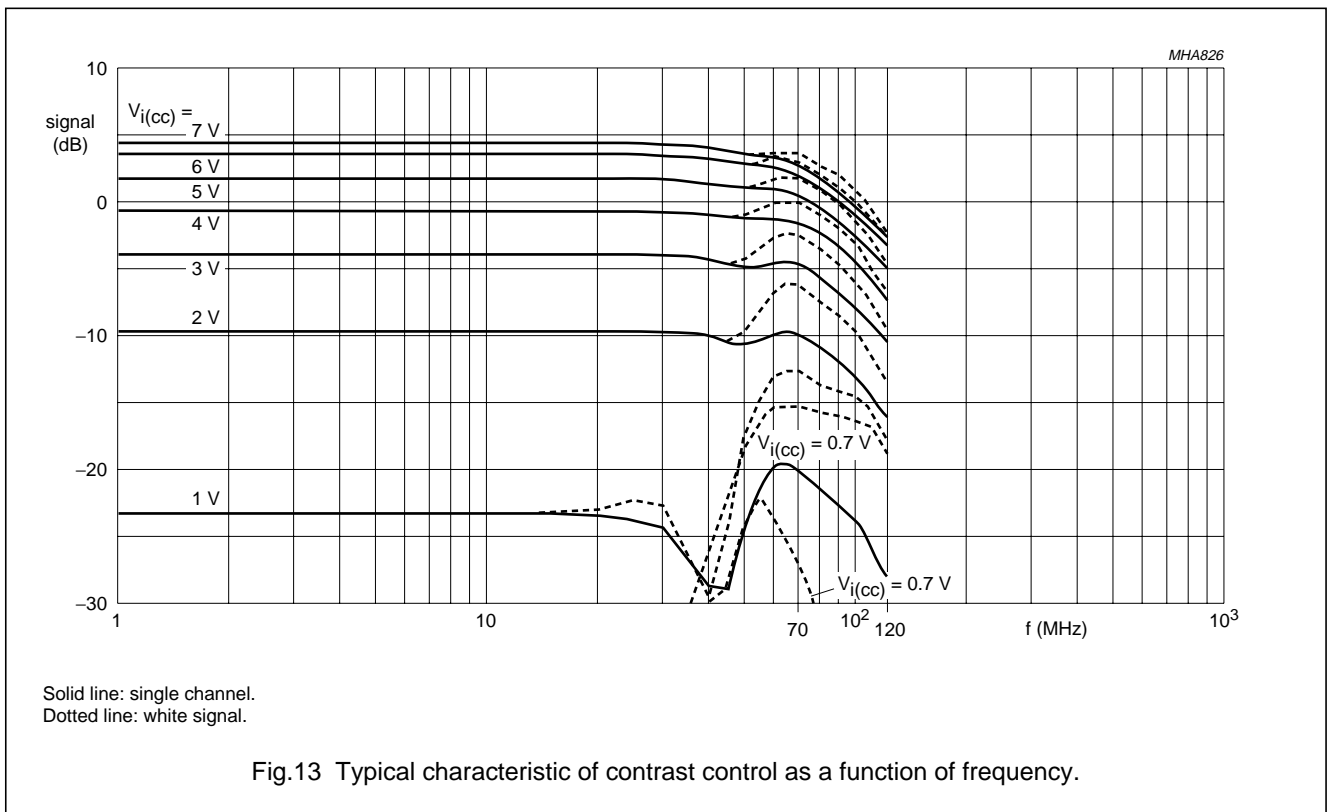
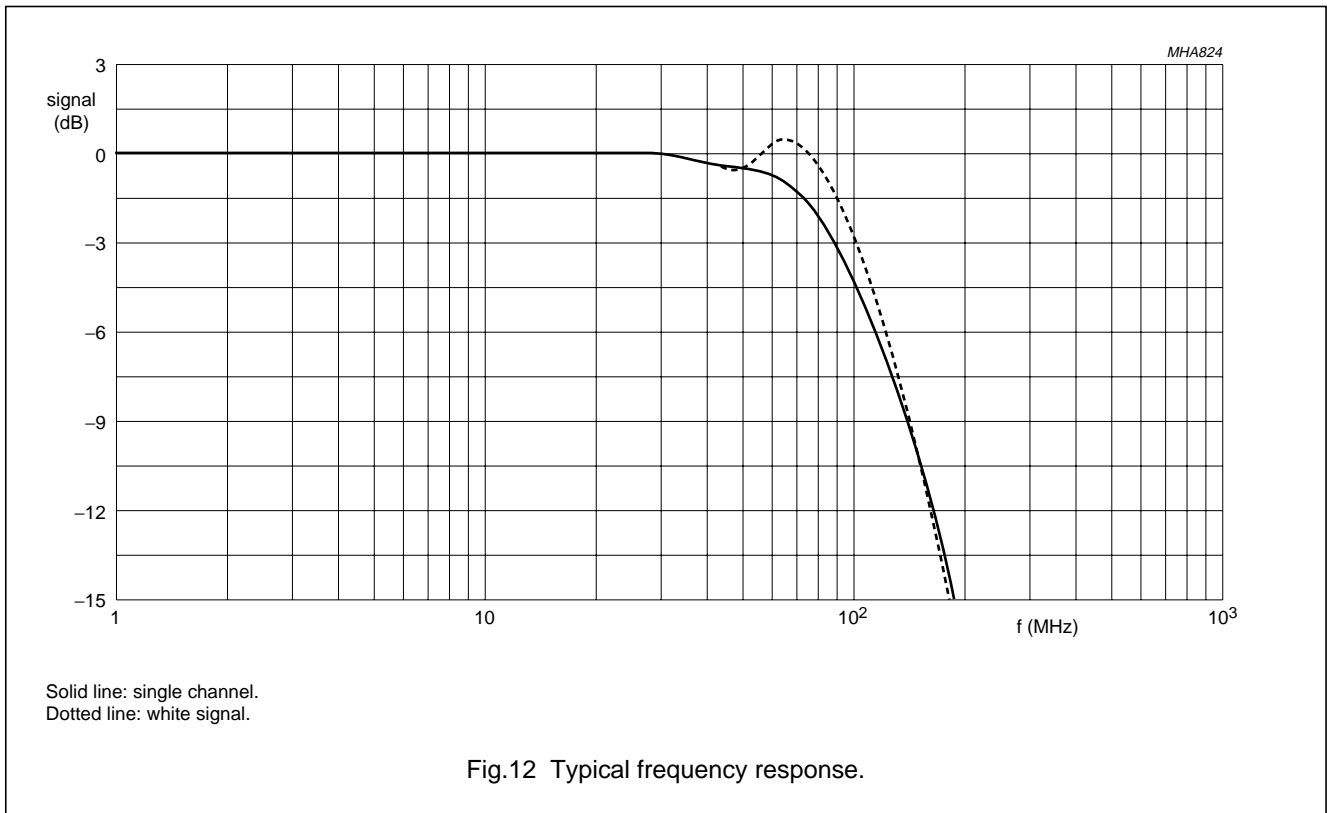


Solid line: single channel.
Dotted line: white pattern.

Fig.11 Typical pulse response: VIN1, VIN2 and VIN3 → VOUT1, VOUT2 and VOUT3.

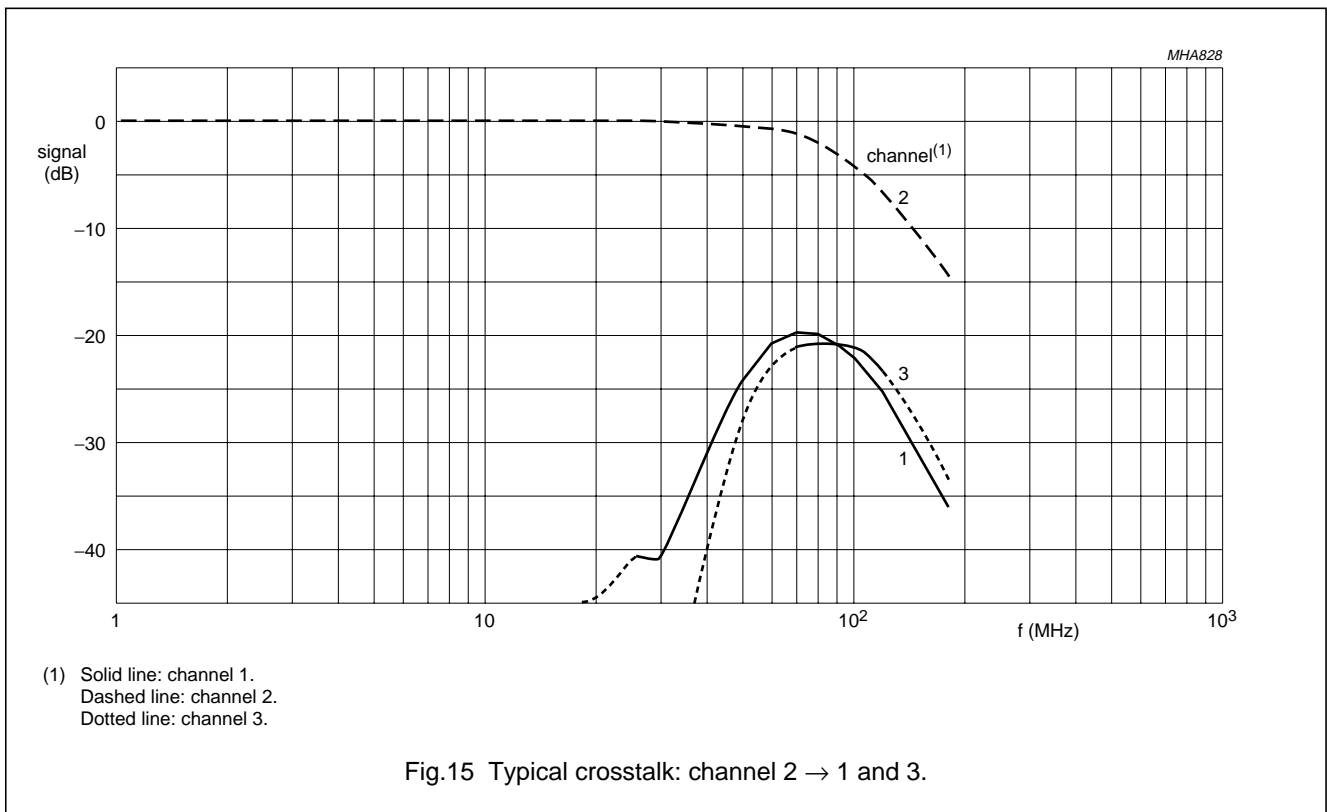
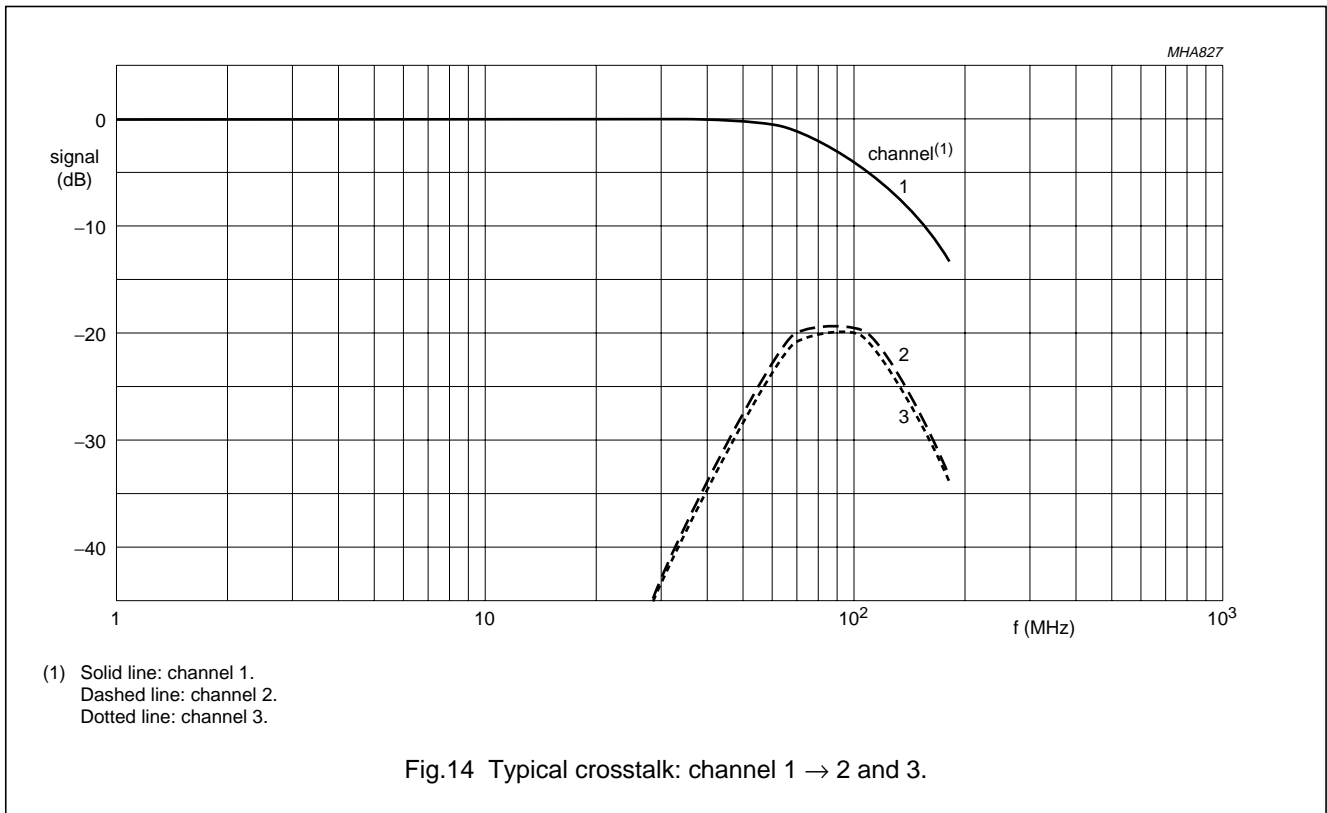
Advanced monitor video controller for OSD

TDA4882



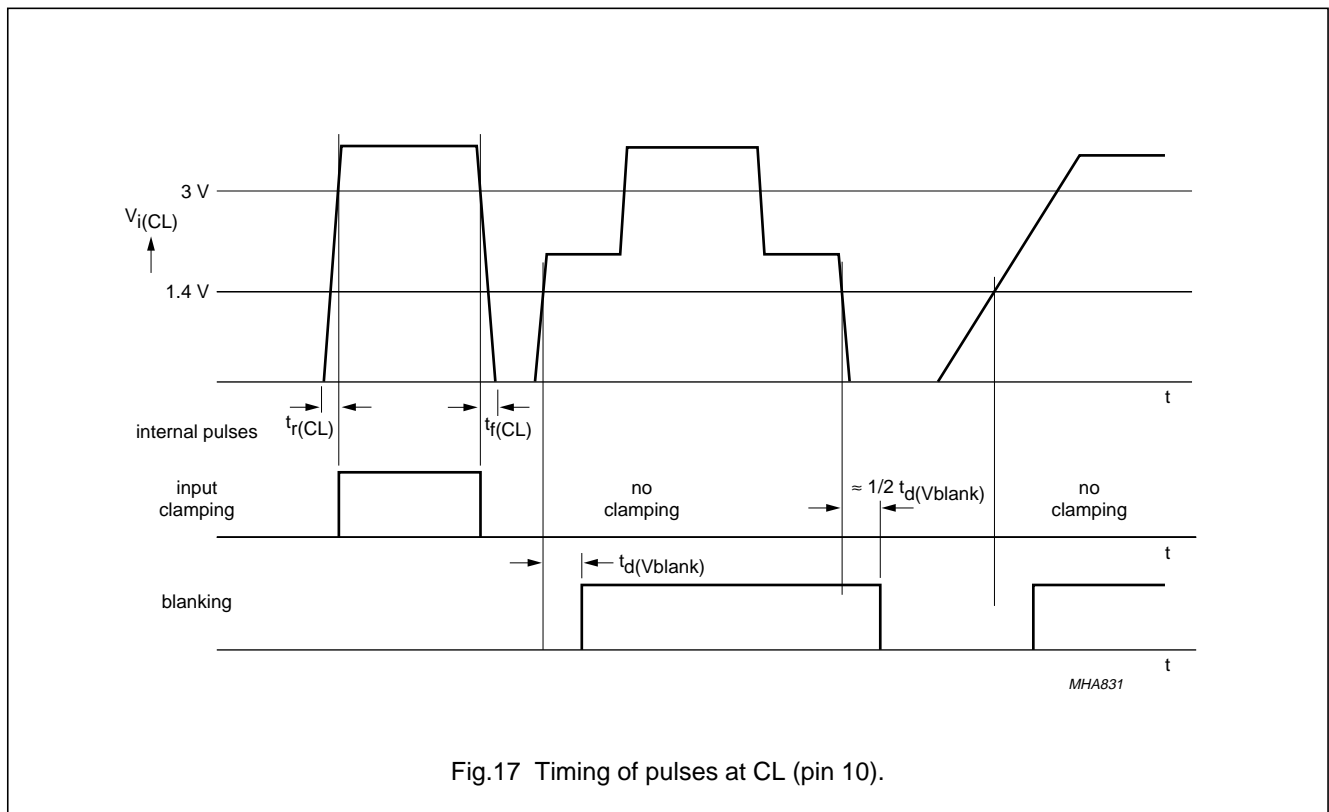
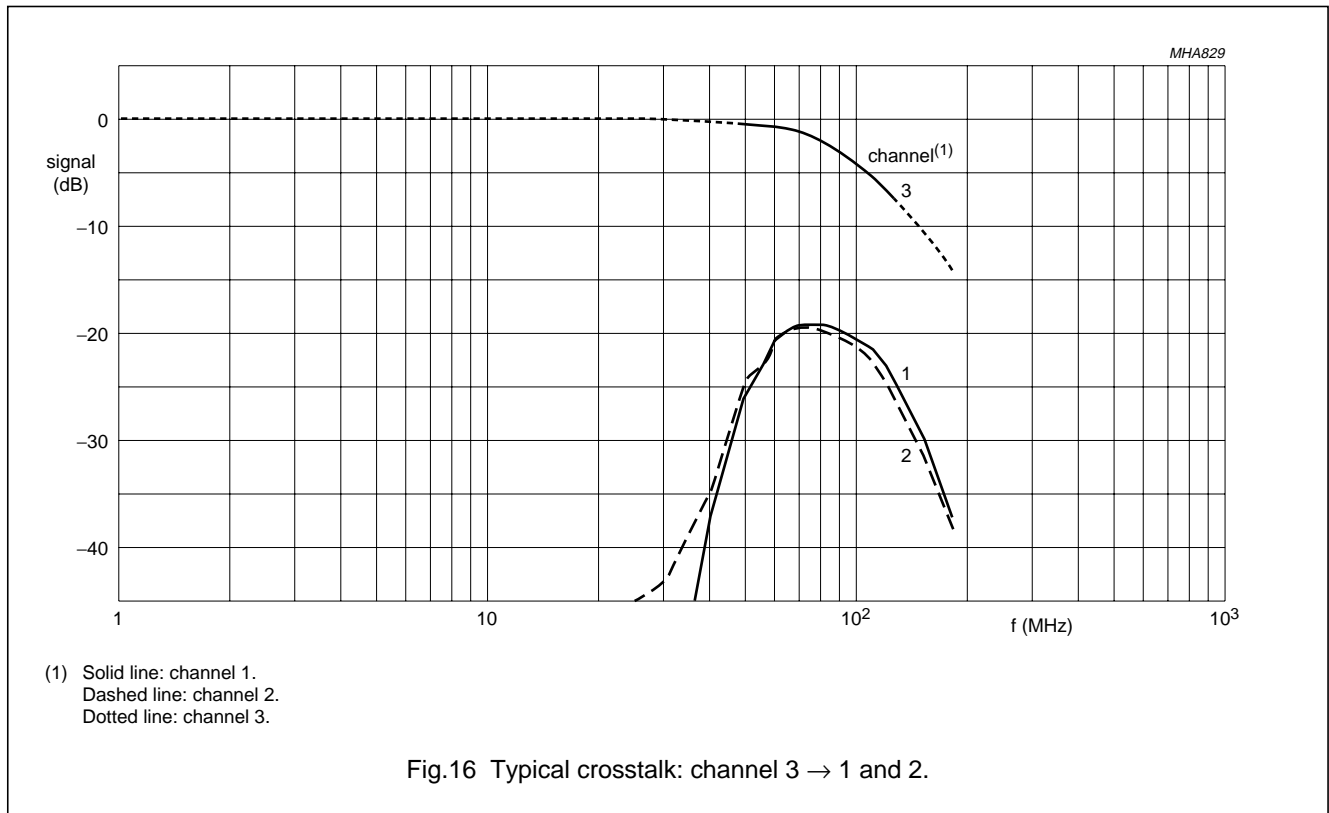
Advanced monitor video controller for OSD

TDA4882



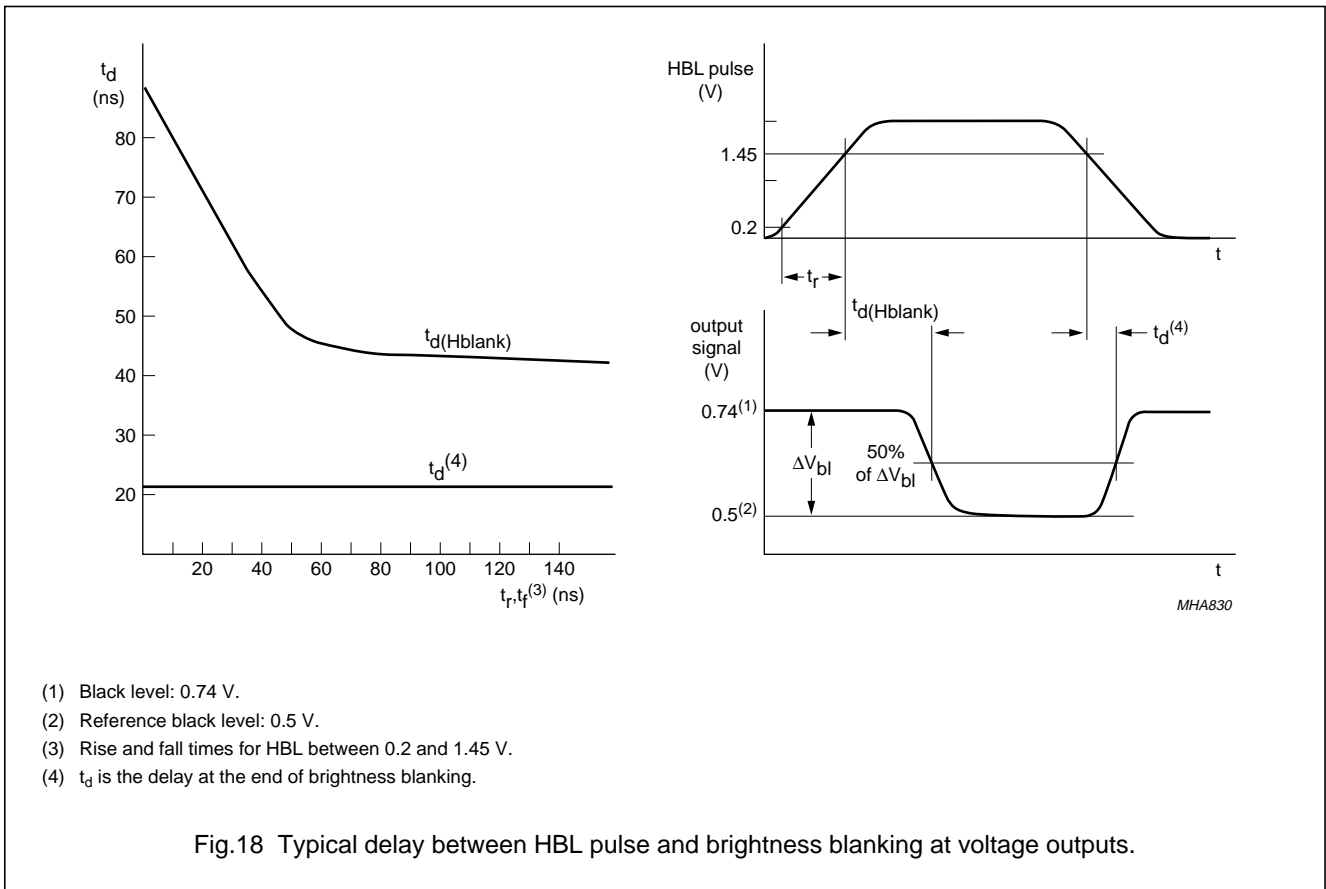
Advanced monitor video controller for OSD

TDA4882



Advanced monitor video controller for OSD

TDA4882



Advanced monitor video controller for OSD

TDA4882

11 APPLICATION AND TEST INFORMATION

For high frequency measurements and special application, a printed-circuit board with only a few external components is built. Figure 19 shows the application circuit and Fig.20 the layout of the double sided printed board. All components on the underside and R13, R14 and R15 on the top are SMD types. Short HF loops and minimum crosstalk between the channels as well as input and output are achieved by properly shaped ground areas star connected to the IC ground pin.

The HF input signal can be fed to the subclick connectors P1, P2 and P3 by a 50 Ω line. The line is then terminated by a 51 Ω resistor on the board. With choice of jumper connections (J1, J2 and J3) it is possible to connect channel inputs to its input connector, to connect all channels to one input connector (white pattern) and to ground each input via the coupling capacitor.

For operation without input clamping, e.g. test mode, the DC bias can be provided by VIDC (connector P21) if a short-circuit at J4, J5 and J6 is made (solder short or low-value SMD resistor).

The output signal can be monitored via 50 Ω terminated lines at the voltage outputs (subclick connectors P4, P5 and P6). With 100 Ω in parallel to the 50 Ω terminated line the effective load resistance at the voltage outputs is 33 Ω . The mismatch seen from the line towards the IC has no significant effect if the line is match terminated. A peaking circuit, C15, R16 for channel 1 (C16, R17 for channel 2 and C17, R18 for channel 3), can be added for realistic loading of the voltage outputs.

Black-level adjustment is made by VIOS, VFBX (external voltages at connector P21) and resistors R19, R22 and R25 for channel 1 (channel 2: R20, R23 and R26; channel 3: R21, R24 and R27). If R19 is equal to the effective load resistor at the voltage output the reference black level ($V_{\text{ref(bl)}}$) is approximately:

$$V_{\text{ref(bl)}} = \text{VIOS} - V_{\text{ref(int)}} - (V_{\text{ref(int)}} - \text{VFBX}) \times \frac{R22}{R25}$$

$V_{\text{ref(int)}}$ is the internal reference voltage at the feedback input (typical 5.8 V). By this it is possible to adjust the reference black level and the voltage at the current outputs independently.

DC control for brightness, contrast and gain is provided at connectors P21 and P22. Contrast control can also be set by the potentiometer R28 (jumper J11). The series resistor R11 is necessary if fast OSD switching is activated via 50 Ω line (P10), a line termination can be provided at the connector P9. Clamping and blanking pulses are fed to the IC via connectors P7 and P8. Connector P23 is used for power supply. The capacitors C7 and C8 should be located as near as possible to the IC pins.

11.1 Recommendations for building the application board

- General
 - Double-sided board
 - Short HF loops by large ground plane on the rear.
- Voltage outputs
 - Capacitive loads as small as possible
 - Short interconnection via resistor to ground.
- Supply voltage
 - Capacitors as near as possible to the pins
 - Use of high-frequency capacitors (low self inductance, e.g. SMD).
- Resonance suppression. The external interconnection inductance to the current outputs can build a resonance together with the internal substrate capacitance. A damping resistor of 10 to 30 Ω near to the IC pin can suppress such oscillations.

Advanced monitor video controller for OSD

TDA4882

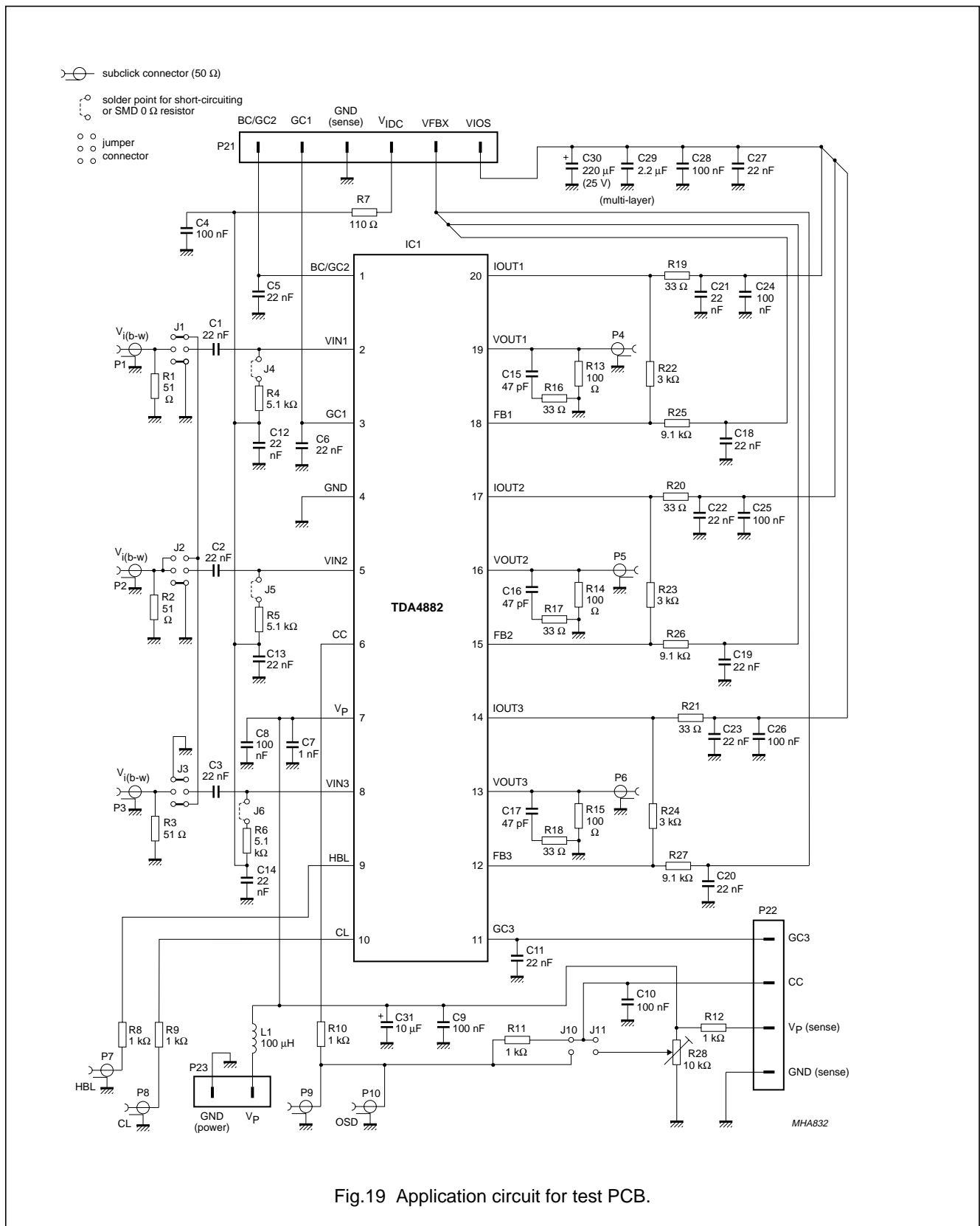
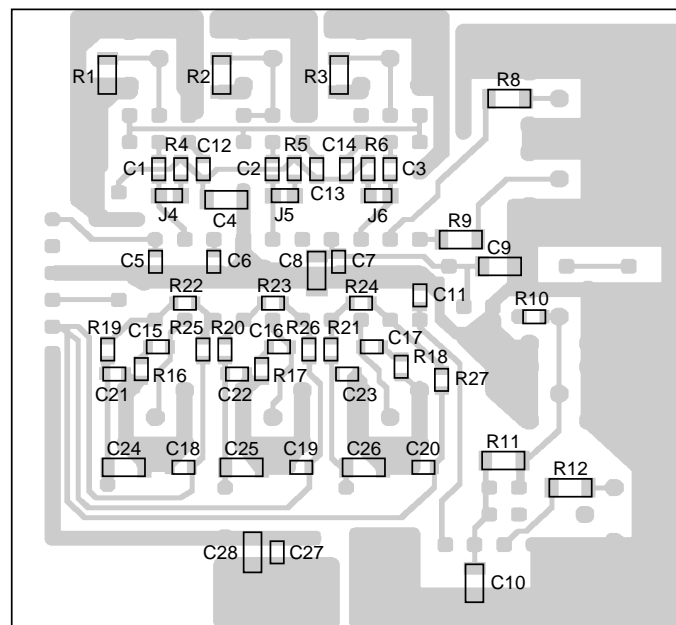
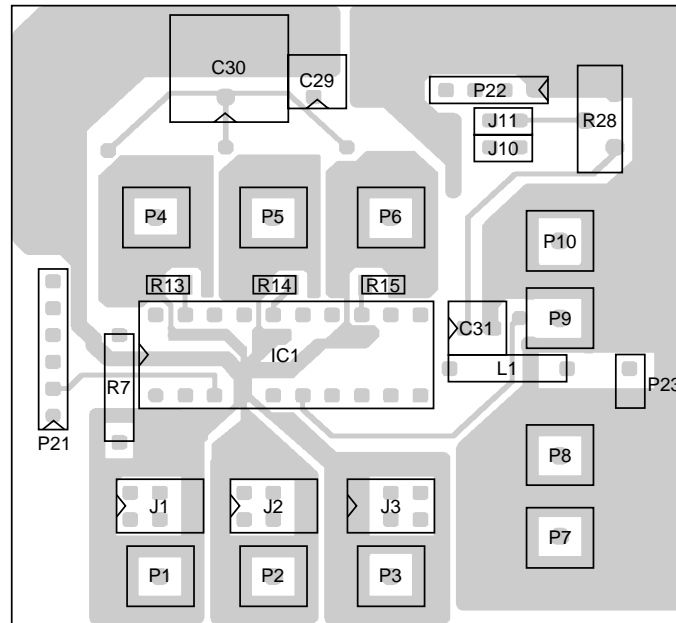


Fig.19 Application circuit for test PCB.

Advanced monitor video controller for OSD

TDA4882



MHA833

Fig.20 Double sided test PCB layout.

Advanced monitor video controller for OSD

TDA4882

12 INTERNAL PIN CONFIGURATION

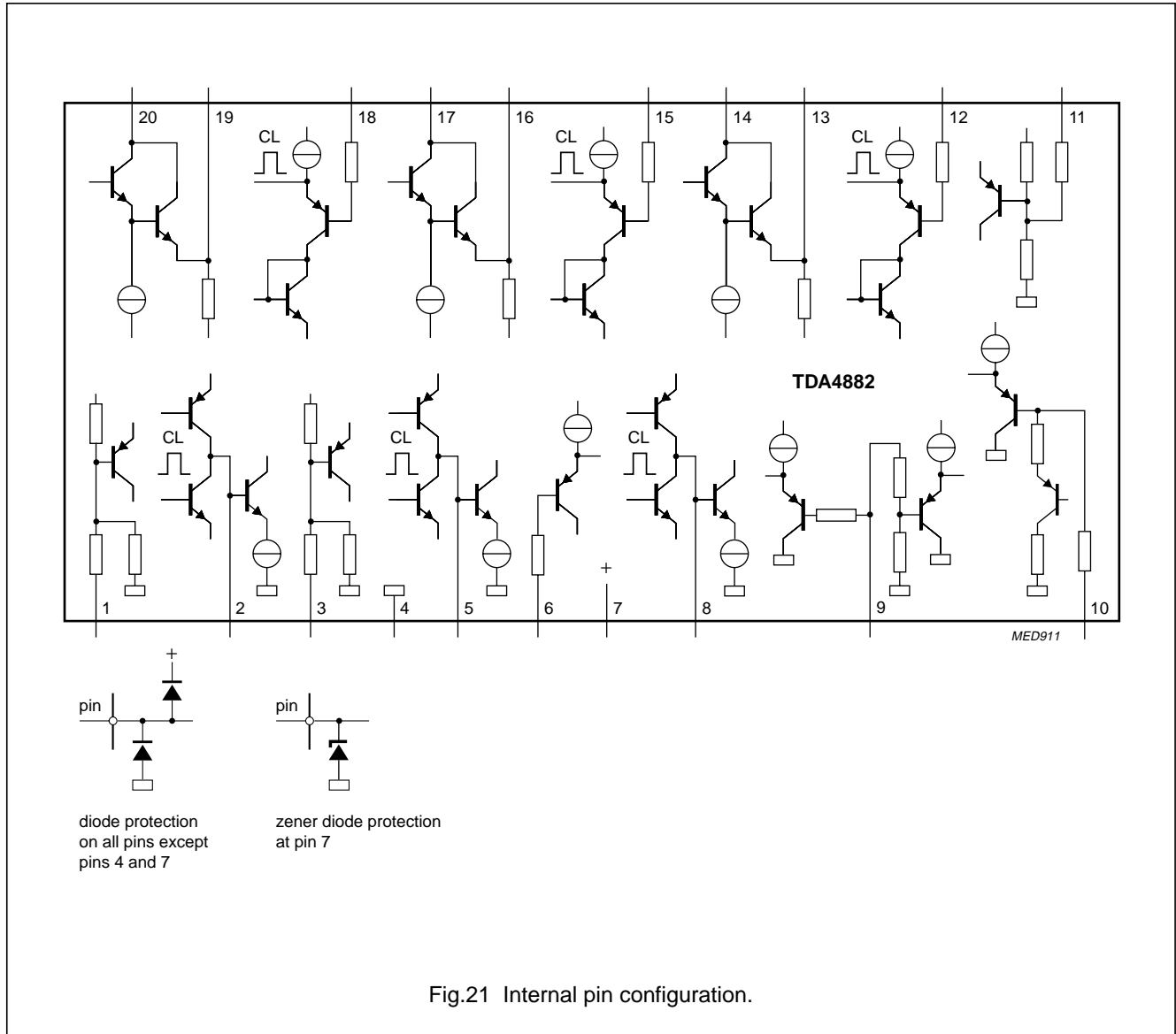


Fig.21 Internal pin configuration.

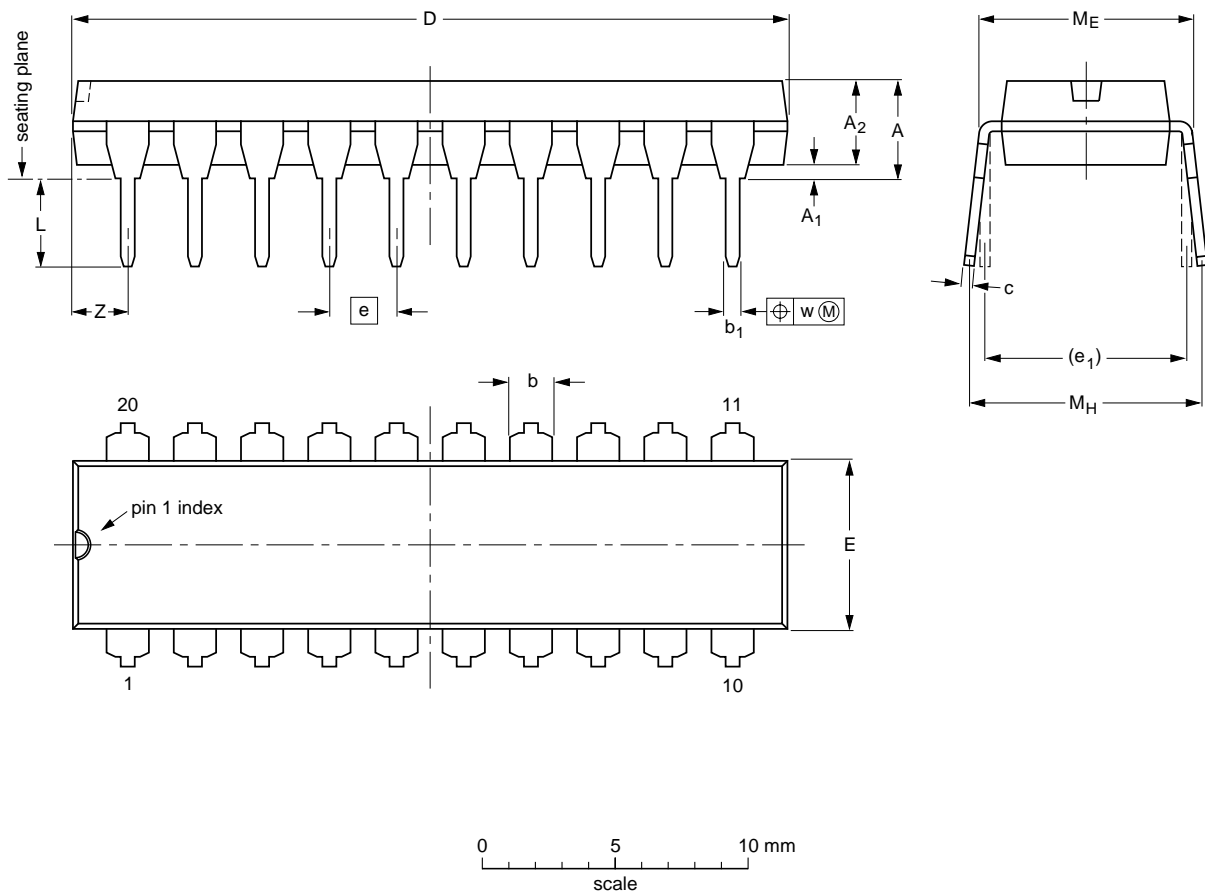
Advanced monitor video controller for OSD

TDA4882

13 PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Advanced monitor video controller for OSD

TDA4882

14 SOLDERING**14.1 Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

14.2 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Advanced monitor video controller for OSD

TDA4882

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 1997

SCA55

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

547047/1200/02/pp28

Date of release: 1997 Sep 04

Document order number: 9397 750 02268

Let's make things better.

**Philips
Semiconductors**



PHILIPS