Wireless Components

ASK/FSK Transmitter 868/433 MHz

TDA 5100 V 1.0

Specification May 1999

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide:
see our webpage at http://www.infineon.com

ABM®, AOP®, ARCOFI®, ARCOFI®-BA, ARCOFI®-SP, DigiTape®, EPIC®-1, EPIC®-S, ELIC®, FALC®54, FALC®56, FALC®-E1, FALC®-LH, IDEC®, IOM®, IOM®-1, IOM®-2, IPAT®-2, ISAC®-P, ISAC®-S, ISAC®-S TE, ISAC®-P TE, ITAC®, IWE®, MUSAC®-A, OCTAT®-P, QUAT®-S, SICAT®, SICOFI®, SICOFI®-2, SICOFI®-4, SICOFI®-4µC, SLICOFI® are registered trademarks of Infineon Technologies AG.

ACE™, ASM™, ASP™, POTSWIRE™, QuadFALC™, SCOUT™ are trademarks of Infineon Technologies AG.

Edition 03.99
Published by Infineon Technologies AG i. Gr.,
SC,
Balanstraße 73,
81541 München

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Infineon Technologies AG, may only be used in life-support devices or systems[2] with the express written approval of the Infineon Technologies AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

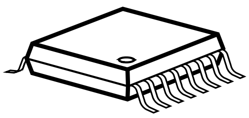
2Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

Productinfo

General Description

The TDA5100 is a single chip ASK/ FSK transmitter for the frequency bands 868-870 MHz and 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery live. Additionally features like a power down mode, a low power detect, a selectable crystal oscillator frequency and a divided clock output are implemented. The IC can be used for both ASK and FSK modulation.

Package



Features

- fully integrated frequency synthesizer
- VCO without external components
- high efficiency power amplifier
- switchable frequency range 868-870/433-435 MHz
- ASK/FSK modulation
- low supply current (typically < 7mA)
- voltage supply range 2.1 - 4 V
- power down mode
- low voltage sensor
- selectable crystal oscillator 6.78 MHz/13.56 MHz
- programmable divided clock output for µC
- low external component count

Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

Ordering Information

Type	Ordering Code	Package
TDA 5100		P-TSSOP-16

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

The TDA5100 is a single chip ASK/FSK transmitter for the frequency bands 868-870 MHz and 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery live. Additionally features like a power down mode, a low power detect, a selectable crystal oscillator frequency and a divided clock output are implemented. The IC can be used for both ASK and FSK modulation.

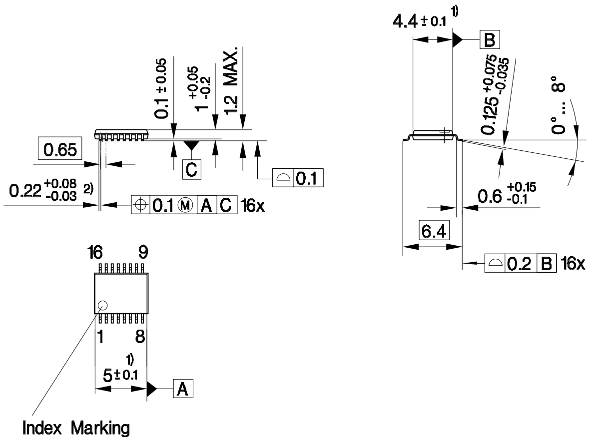
2.2 Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

2.3 Features

- fully integrated frequency synthesizer
- VCO without external components
- high efficiency power amplifier
- switchable frequency range 868-870/433-435 MHz
- ASK/FSK modulation
- low supply current (typically < 7mA)
- voltage supply range 2.1 - 4 V
- power down mode
- low voltage sensor
- selectable crystal oscillator 6.78 MHz/13.56 MHz
- programmable divided clock output for µC
- low external component count

2.4 Package Outlines



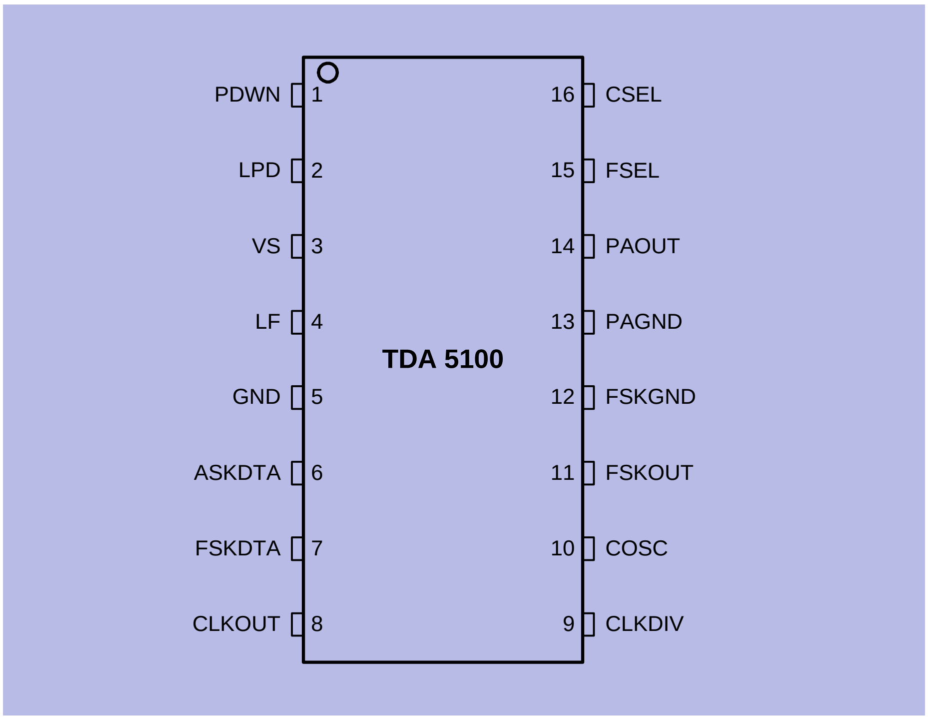
1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Figure 2-1 P-TSSOP-16

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration

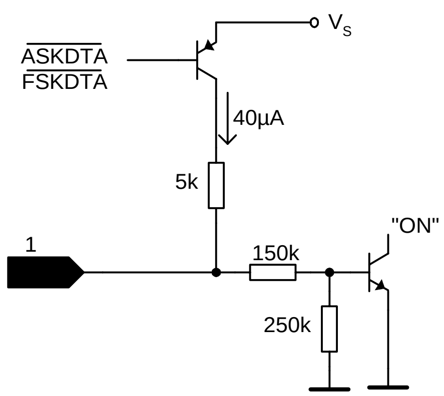
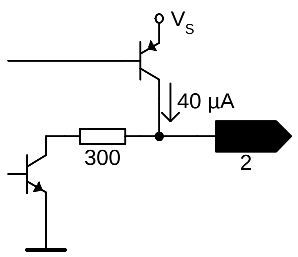
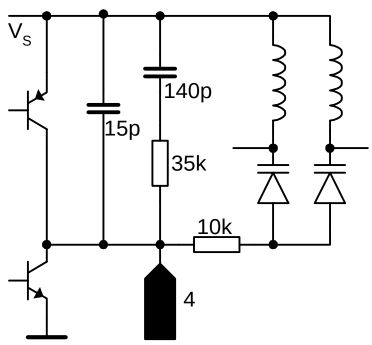


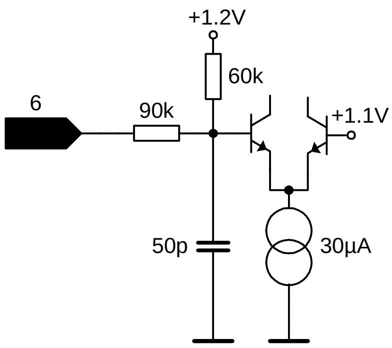
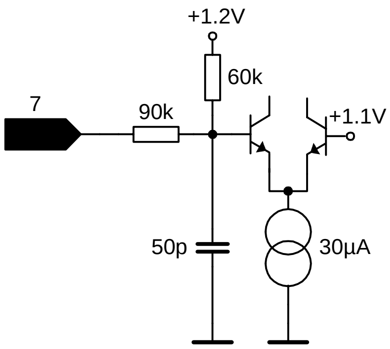
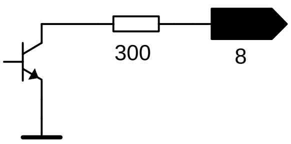
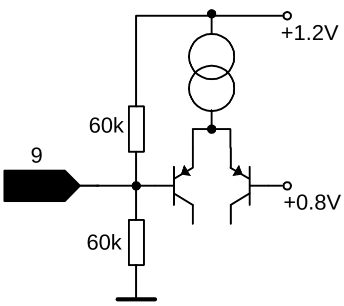
Pin_config.wmf

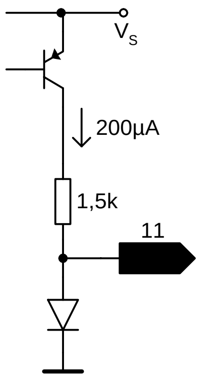
Figure 3-1 IC Pin Configuration

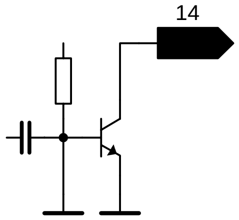
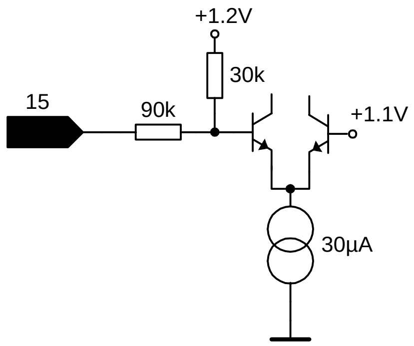
3.2 Pin Definitons and Functions

Table 3-1

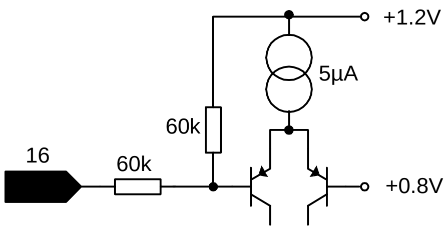
Pin No.	Symbol	Interface Schematic	Function
1	PDWN		Disable pin for transmitter circuit. PDWN < 0.7V turns off all transmitter functions. PDWN > 1.5V gives access to all transmitter functions. PDWN input will be pulled up by 40µA internally by either setting FSKDTA or ASKDTA to a logic high state.
2	LPD		This pin provides an output indicating the low-voltage state of the supply voltage VS. VS < 2.15V will set LPD to the low state.
3	VS		This pin is used to supply DC bias to the transmitter electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground as short as possible.
4	LF		Output of the charge pump and input to the VCO control. An internal loop filter has been designed for a loop bandwidth of 150kHz. The loop bandwidth may be reduced by applying an external RC network.

5	GND		General ground connection.
6	ASKDTA		Digital amplitude modulation can be imparted to the PA through this pin. ASKDTA > 1.5V or an open enables the PA. ASKDTA < 0.5V disables the PA.
7	FSKDTA		Digital frequency modulation can be imparted to the XO by this pin. The VCO varies in accordance to the frequency of the reference oscillator. FSKDTA < 0.5V closes the FSKOUT switch at pin 11. A capacitor can be switched to the XO network this way. The XO frequency will be shifted giving the designed FSK frequency deviation. FSKDTA > 1.5V or an open will set the FSKOUT switch to a high impedance state.
8	CLKOUT		Clock output to supply a external device. A external pull up resistor has to be added in accordance to the driving requirements of the external device. A clock frequency of 3.39MHz can be selected by a logic low at CLKDIV input, pin9. A logic high or a open at the CLKDIV input will result in a CLKOUT frequency of 847.5kHz.
9	CLKDIV		This pin is used to select the desired clock division for the CLKOUT signal. A logic low CLKDIV < 0.5V selects the 339MHz output signal at pin8. A logic high CLKDIV > 1.5V or an open selects the 847.5kHz output signal.

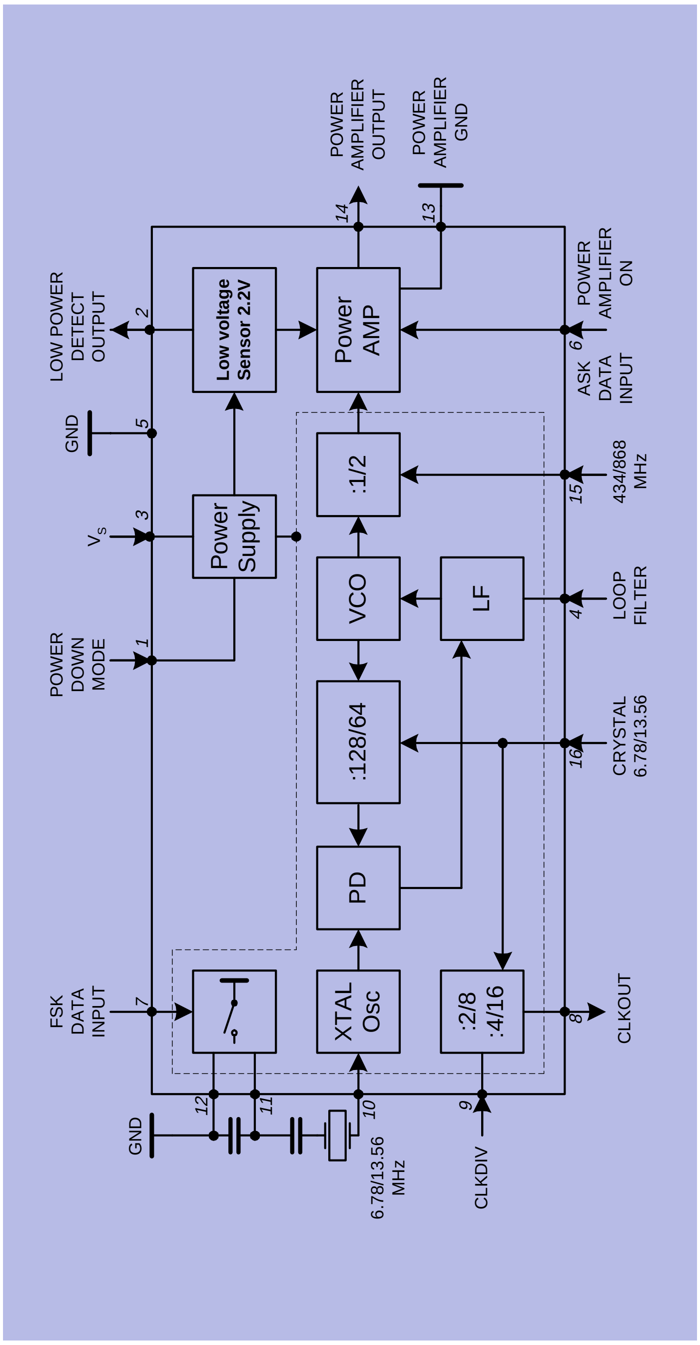
10	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator configuration is of the negative impedance converter type. It presents a negative resistor in series to an inductor at the COSC pin.
11	FSKOUT		This pin is a switch being activated by the FSKDTA signal at pin 7. The switch is closed for a logic low at the FSKDTA pin. It is open for a logic high or a open at the FSKDTA input. FSKOUT will switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the designed FSK frequency shift of the transmitter output frequency.
12	FSKGND		Ground connection for FSK modulation output FSKOUT.
13	PAGND		Ground connection for the power amplifier (PA). All the RF ground path of the power amplifier should be concentrated to this pin.

<table>
<tr><td>14</td><td>PAOUT</td><td>
</td><td>RF output pin for the transmitter. A DC path to VS has to be supplied by the antenna matching network.</td></tr>
<tr><td>15</td><td>FSEL</td><td>
</td><td>This pin is used to select the desired transmitter frequency.

FSEL < 0.5V will give access to the 434MHz frequency range.

FSEL > 1.5V or a open will put the transmitter to the 869MHz mode.</td></tr>
<tr><td>16</td><td>CSEL</td><td>
</td><td>A logic low (CSEL < 0.5V) applied to this pin sets the internal frequency divider for a reference frequency of 6.7MHz. A logic high (CSEL > 1.5V or a open) will be applied for a reference frequency of 13.5MHz.</td></tr>
</table>

3.3 Block diagram

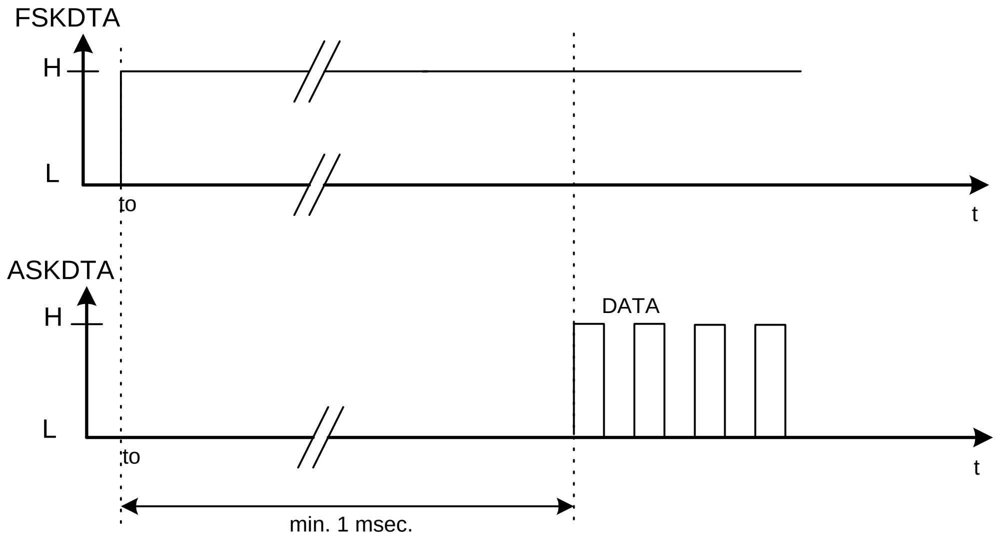


Block_diagram.wmf

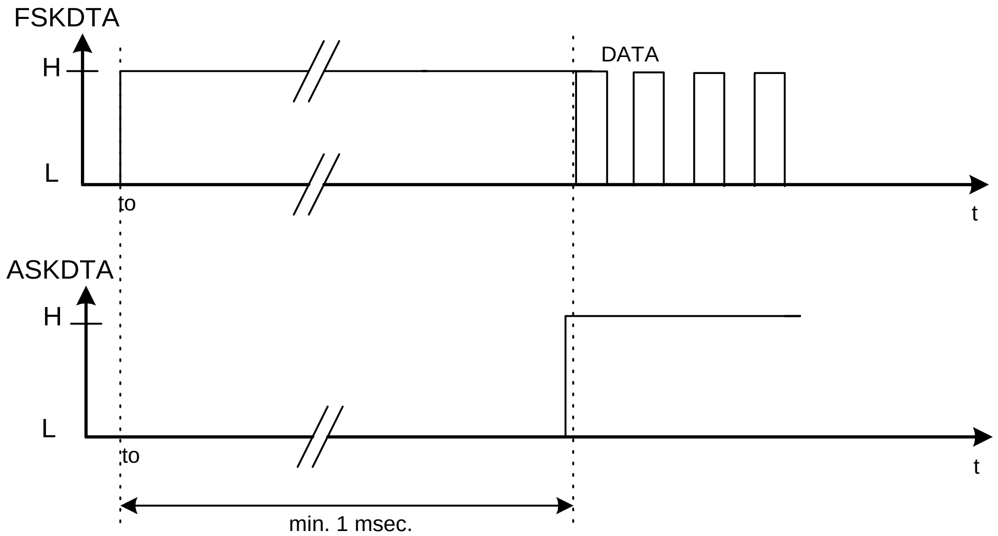
Figure 3-2 Main Block Diagram

3.4 Functional Blocks

1. PLL Synthesizer



The Phase Locked Loop synthesizer consists of a voltage controlled oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter and is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no



additional external components are necessary. The nominal center frequency of the VCO is 869 MHz. The oscillator signal is fed both to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asyncronous divider chain is 128 in case of a 6.78 MHz crystal or 64 in case of a

13.56 MHz crystal and can be selected via pin 16 (CSEL). The phase detector is a Typ IV PD with charge pump. The passive loop filter is realized on chip.

Table 3-2

CSEL	Crystal Frequency
Open	13.56 MHz
Shorted to ground	6.78 MHz

2. Crystal Oscillator

The crystal oscillator operates either at 6.78 MHz or 13.56 MHz. In case of FSK transmission the oscillator frequency can be detuned by a fixed amount determined by an external capacitor via pin 7 (FSKDTA). For both quartz frequency options 847.5 kHz or 3.39 MHz are available as a clock frequency output (CLKOUT) to drive the clock input of a micro controller. The dividing ratio is controlled by the CLKDIV pin.

Table 3-3

FSKDTA	FSKOUT Switch
Open	OFF
Shorted to ground	ON

Table 3-4

Crystal Frequency	CLKDIV	Dividing Ratio
6.78 MHz	Shorted to ground	2
13.56 MHz	Shorted to ground	4
6.78 MHz	Open	8
13.56 MHz	Open	16

3. Power Amplifier

In case of operation in the 868-870 MHz band the power amplifier is fed directly from the voltage controlled oscillator. In case of operation in the 433-435 MHz band the VCO frequency is divided by 2. This is controlled by the FSEL pin as described in the table below. In FSK transmission the power amplifier can be switched on with pin 6 (ASKDTA). In case of ASK transmission the same pin is used as the data input.
The PAOUT pin is an open collector output and requires an external pull up coil to provide bias. The coil is part of the tuning and matching LC cuircit to get best performance with the external loop antenna. To achieve the best power amplifier efficiency the high frequency voltage swing at the PAOUT pin should be two times the supply voltage.

The power amplifier has its own ground pin (PAGND) in order to reduce the amount of coupling to the other circuits.

Table 3-5

FSEL	Radiated Frequency Band
Open	869 MHz
Shorted to ground	433 MHz

4. Low Power Detect

The supply voltage is sensed by a low power detector. If the supply voltage drops below 2.15 V the power amplifier can be turned off via pin 6.

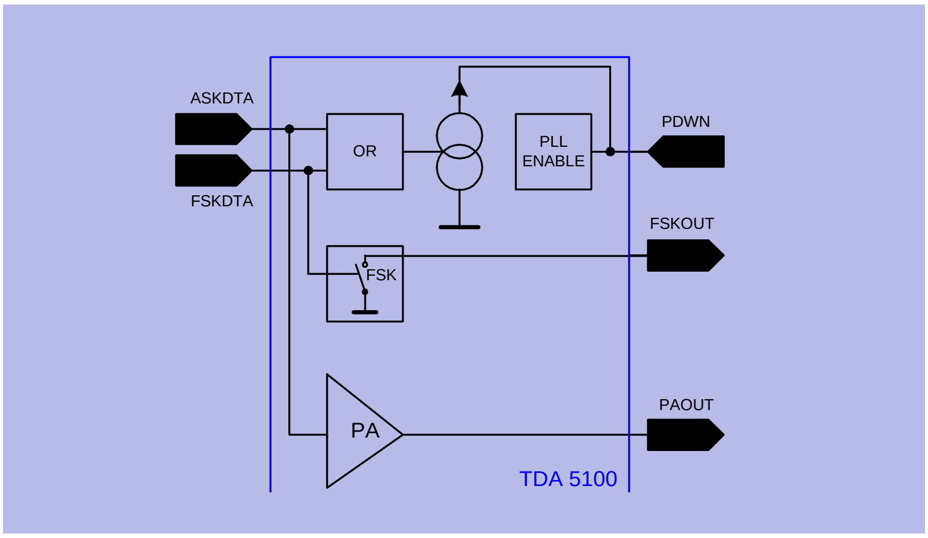
5. Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE. How to get in this modes is described in the table below.

Table 3-6

PDWN	FSKDTA	ASKDTA	
L	L	L	POWER DOWN MODE
H	L;H	L	PLL ENABLE MODE
not connected;H	H	L	PLL ENABLE MODE
not connected,H	L;H	H	TRANSMIT MODE

If ASKDTA or FSKDTA gets high, the PDWN pin is pulled up internally via a current source as shown in the diagram below. Therefore, in most applications it is not necessary and recommended to connect the PDWN pin.



Power_Mode.wmf

Figure 3-3 Power mode

6. Power Down Mode

In the POWER DOWN MODE the current consumption is less than 100nA. To switch the IC in this mode, the input pins PDWN (pin1), ASKDTA (pin6) and FSKDTA (pin7) has to be in the low state.

7. PLL Enable Mode

The turn on time of the PLL is determined by the turn on time of the crystal oscillator and is typically less than 1 msec (dependent on the crystal itself). To save current consumption and to avoid undesired power radiation during this time, the power amplifier is turned off. The current consumption at this mode is typically 3.5 mA.
To have the possibility to control the IC via two data lines from a micro processor, the ASK- and FSK Data inputs are connected via a “logical or” to pull up internally the PDWN input. In this case, it is recommended to leave thePDWN pin unconnected.

8. Transmit Enable Mode

In the TRANSMIT ENABLE MODE the power amplifier is turned on too, and the current consumption of the IC is about 7 mA. To get in this state, the ASKDTA input is to switch to a high level.

9. Recommended timing diagrams for ASK- and FSK modulation

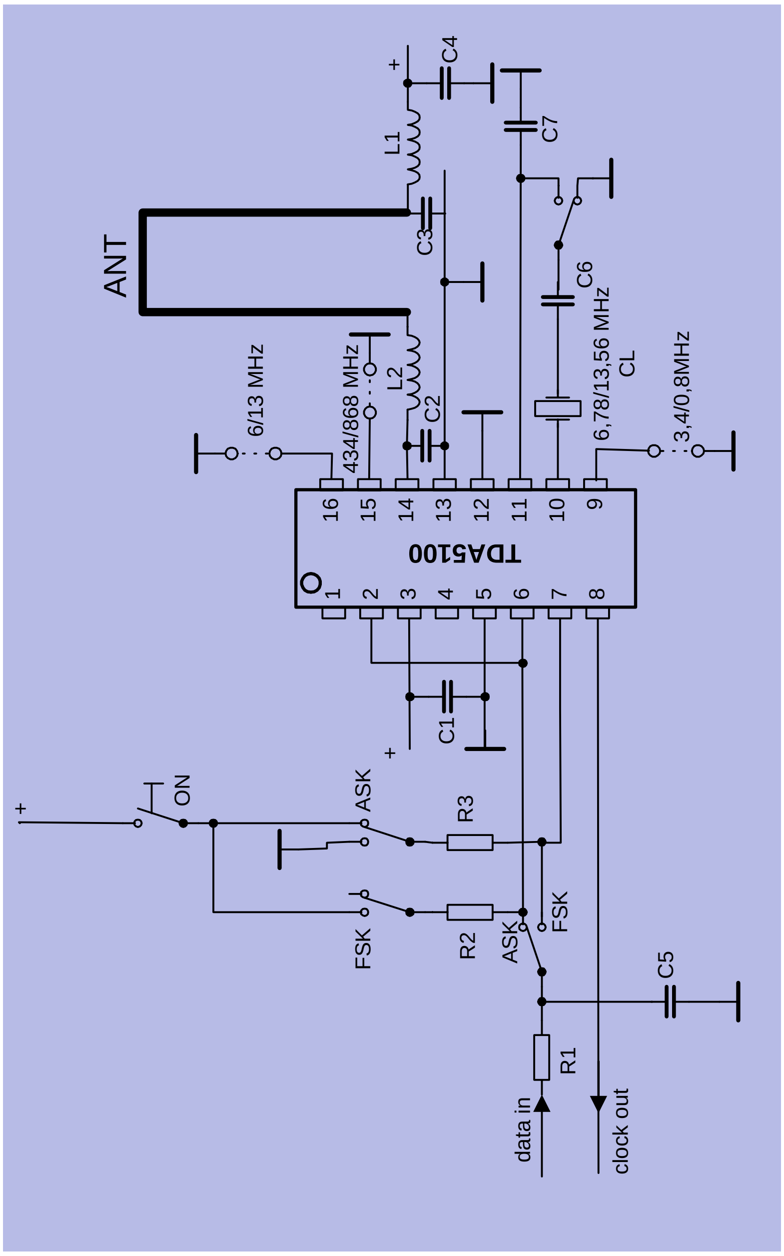
ASK Modulation :
(Pin1 (PDWN) not connected)
Figure 3-4 ASK Modulation

FSK Modulation:
(Pin1 (PDWN) not connected)
Figure 3-5 FSK Modulation

4 Applications

Contents of this Chapter

4.1 Circuits



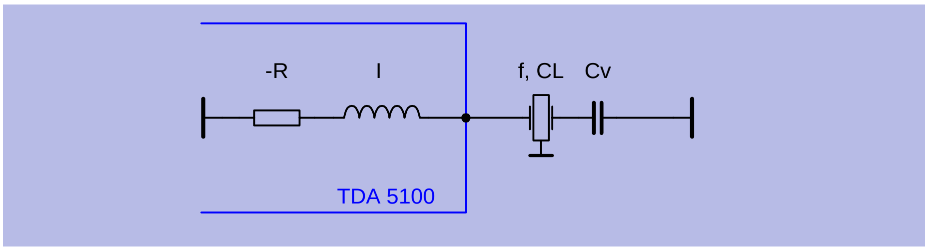
Application_Circuit.wmf

Figure 4-1 Application Circuit

4.2 Hints

1. Application Hints to the crystal oscillator

As mentioned before, the crystal oscillator achieves a turne on time less than 1 msec. To attend this, a NIC oscillator type is implemented in the TDA5100. This oscillator type has the property, that the input impedance is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.



$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 l} \qquad 1)$$

CL: crystal load capacitance for nominal frequency
ω: angular frequency
l: inductivity of the crystal oscillator

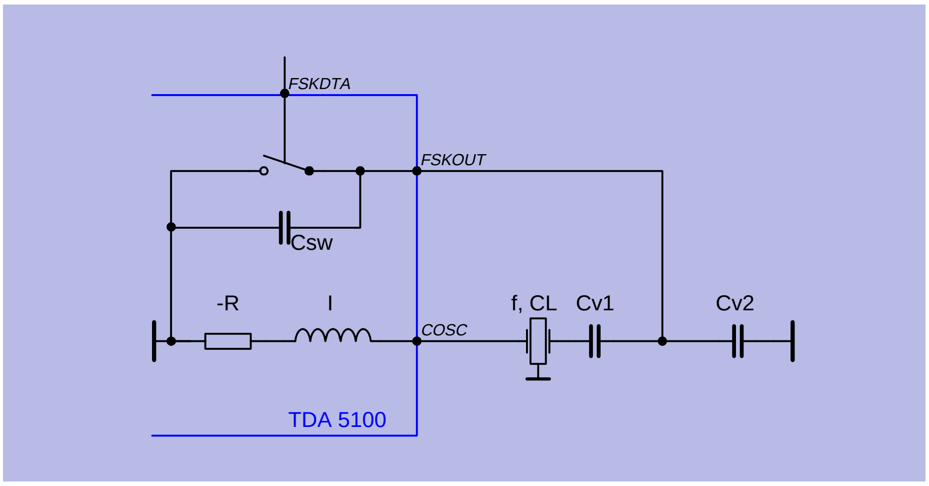
Example for the ASK-Mode:

Refering to the application circuit, in ASK-Mode the capacitance C7 is replaced by a short to ground. Assuming a crystal frequency of 13.56 MHz and a crystal load capacitance of CL=20pF. The inductance l is specified within the electrical characterisics at 13.5MHz to a value of 11uH. Therefore C6 is calculated to 7.7pF.

$$C6 = \frac{1}{\frac{1}{CL} + \omega^2 l} = Cv$$

Example for the FSK-Mode:

FSK modulation is achieved by switching the load capacitance of the crystal as shown below.



The frequency deviation of the crystal oscillator is multiplied with the divider factor N of the Phase Locked Loop to the output of the power amplifier. In case of small fequency deviations (up to +/- 1000ppm), the two desired load capacitances can be calculated with the formula below.

$$C_L \pm = \frac{C_L \mp C_0 \frac{\Delta f}{N \times f_1}\left(1 + \frac{2(C_0 + C_L)}{C_1}\right)}{1 \pm \frac{\Delta f}{N \times f_1}\left(1 + \frac{2(C_0 + C_L)}{C_1}\right)}$$

C_L: crystal load capacitance for nominal frequency
C_0: shunt capacity of the crystal
ω: angular frequency
N: divider factor of the PLL
df: peak frequency deviation

Because of the inductive part of the TDA5100 this values must be corrected by formula 1). Therefore Cv± can be calculated.

$$C_V \pm = \frac{1}{\left(\frac{1}{CL}\right) + \omega^2 l}$$

If the FSK switch is closed, Cv_ is equal to Cv1 (C6 in the application diagram). If the FSK switch is open, Cv2 (C7 in the application diagram)can be calculated.

$$Cv2 = C7 = \frac{Csw \times Cv1 - Cv + (Cv1 + Csw)}{Cv + (-Cv1)}$$

Csw: parallel capacitance of the FSK switch (3 pF)

Remark: This calculations are only approximations. The exact values must be found in the specific application board

2. Design hints to the buffered clock output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor (RL) is to connect between this pin and the supply voltage. The value of RL is dependent on the clock frequency and the load capacitance CLD (PCB board plus input capacitance of the microcontroler). RL can be calculated to:

$$RL = \frac{1}{fCLKOUT \times 2 \times CLD}$$

Table 4-1

fCLKOUT= 847 kHz		fCLKOUT= 3.39 MHz	
CL/pF	RL/kOhm	CL/pF	RL/kOhm
5	118	5	29
10	59	10	14
20	29	20	5

Remark: Because of the reason of a low current consumption and a low spurious radiation the largest possible RL should be choosen.

4.3 Bill of Materials

Table 4-2 433 Mhz

Part	ASK	FSK
R1[1)]	4.7k	4.7k
R2	---	10k
R3	10k	---
C1	47n	47n
C2[2)]	8.2p	8.2p
C3[2)]	4.7p	4.7p
C4	100p	100p
C5[1]	4.7n	4.7n
C6[3)]	8.2p	8.2p
C7[3)]	0	22p
L1[2)]	100n	100n
L2[2)]	0	0

Table 4-3 868 Mhz

Part	ASK	FSK
R1[1)]	4.7k	4.7k
R2	---	10k
R3	10k	---
C1	47n	47n
C2[2)]	1.5p	1.5p
C3[2)]	1.0p	1.0p
C4	100p	100p
C5[1]	4.7n	4.7n
C6[3)]	8.2p	8.2p
C7[3)]	0	47p
L1[2)]	27n	27n
L2[2)]	22n	22n

1) Dependent on the data rate.
2) Dependent on the antenna and the PCB layout.
3) The values of C6 and C7 depends on the crystal, the type of modulation and the desired frequency deviation (see below). The given values are for a Kyocera crystal, type KSX-36-13568KOR-MAOR, CL=20pF and a frequency deviation of ± 20 kHz.

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Range

The AC / DCcharacteristic limits are not guaranteed. The maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

Table 5-1

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_S	-40	125	°C	
Thermal Resistance	R_{thSA}		tbd.	K/W	
ESD integrity, all pins	V_{ESD}	-1	+1	kV	100pF, 1500 Ω

Ambient Temperature under bias: T_A=-25 to +85°C

5.1.2 Operating Ratings

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed

Table 5-2

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min	Max		
Supply voltage	V_S	2.1	4.0	V	
Ambient temperature	T_A	-25	85	°C	

5.1.3 AC/DC Characteristics

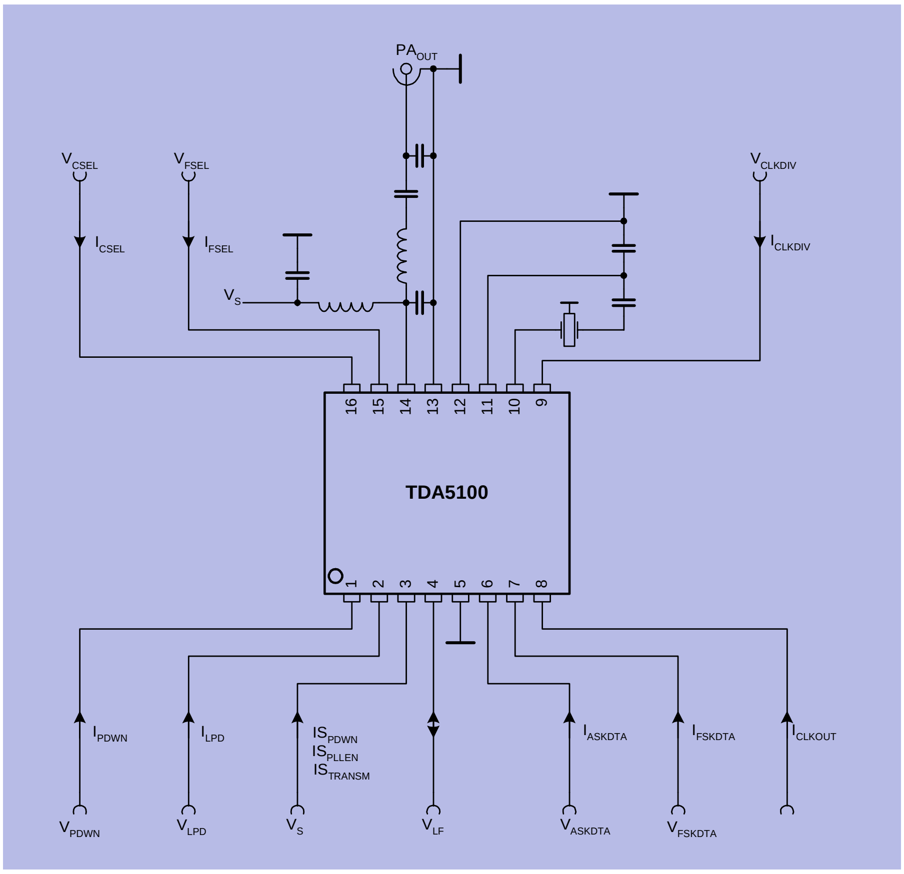
AC / DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Table 5-3 Supply Voltage V_S = 3V, Ambient temperature T_{amb} = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Current consumption						
Stand by mode	$I_{S\ PDWN}$			100	nA	Pins 6,7,9,15 and 16 =0V or N.C.
PLL enable	$I_{S\ PLL\_EN}$		3.3	4	mA	
Transmit enable	$I_{S\ TRANSM}$		7	8	mA	
Power Down Modeswitch						
Stand by mode	V_{PDWN}	0		0.7	V	V_{ASKDTA} < 0.2V V_{FSKDTA}< 0.2V
PLL enable	V_{PDWN}	1.5		Vs	V	V_{ASKDTA} < 0.5V
Transmit enable	V_{PDWN}	1.5		Vs	V	V_{ASKDTA} > 1.4V
Input bias current PDWN	I_{PDWN}			30	µA	V_S = 4V
Low Power Detect						
Internal pull up current	I_{LPD1}	30			µA	V_S = 2.25 ... 4V
Input current low voltage	I_{LPD2}	1			mA	V_S = 1.9 ... 2.05V
VCO tuning voltage	V_{LF}	Vs-1.6		Vs-0.6	V	PLL locked
ASK Modulation						
ASK Transmit disable	V_{ASKDTA}	0		0.5	V	FSK Switch disable
ASK Transmit enable	V_{ASKDTA}	1.5		Vs	V	FSK Switch disable
Input bias current ASKDTA	I_{ASKDTA}			30	µA	V_{ASKDTA} =Vs
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0V
ASK data rate	f_{ASKDTA}			20	kHz	
FSK Modulation						
FSK Switch on	V_{FSKDTA}			0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		Vs	V	
Input bias current FSKDTA	I_{FSKDTA}			30	µA	V_{FSKDAT}= Vs
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDAT}= 0V
FSK data rate	f_{FSKDTA}			20	kHz	
CLOCK driver output						
Output current	I_{CLKOUT}	1			mA	

CLOCK divider control						
Buffered clock output for f=fCRSTL/2 or f=fCRSTL/8	V_{CLKDIV}	0		0.2	V	
Buffered clock output for f=fCRSTL/4 or f=fCRSTL/16	V_{CLKDIV}	1.5		Vs	V	or pin open
Input bias current CLKDIV	I_{CLKDIV}			30	µA	V_{CLKDIV} =Vs
Input bias current CLKDIV	I_{CLKDIV}	-20			µA	V_{CLKDIV} = 0V
Crystal oscillator input						
Load capacitance	$C_{COSC-max}$			5	pF	
Serioues Resistance of the crystal				100	Ohm	f=6.78MHz
Input inductance of the COSC pin			12		µH	f=6.78MHz
Serious Resistance of the crystal				100	Ohm	f=13.56MHz
Input inductance of the COSC pin			11		µH	f=13.56MHz
FSK output switch						
On resistance	R_{FSKOUT}			160	Ohm	
On capacitance	C_{FSKOUT}			6	pF	
Off resistance	R_{FSKOUT}	100k			Ohm	
Off capacitance	C_{FSKOUT}			1.5	pF	
Power amplifier output, transformed to 50 Ohm						
Output Power	P_{PAOUT}		5		dBm	f=433 MHz
	P_{PAOUT}		1		dBm	f=868 MHz
Frequency range input						
Transmit frequency 433 MHz	V_{FSEL}	0		0.2	V	
Transmit frequency 868 MHz	V_{FSEL}	1.5		Vs	V	or pin open
Input bias current FSEL	I_{FSEL}			30	µA	V_{FRANGE} =Vs
Input bias current FSEL	I_{FSEL}	-20			µA	V_{FRANGE} = 0V
Crystal frequency switch						
Crystal frequency 6.78 MHz	V_{CSEL}	0		0.2	V	
Crystal frequency 13.56 MHz	V_{CSEL}	1.5		Vs	V	or pin open
Input bias current CSEL	I_{CSEL}			30	µA	V_{CRSTL} =Vs
Input bias current CSEL	I_{CSEL}	-20			µA	V_{CRSTL} = 0V

5.2 Test Circuit



Test_circuit.wmf

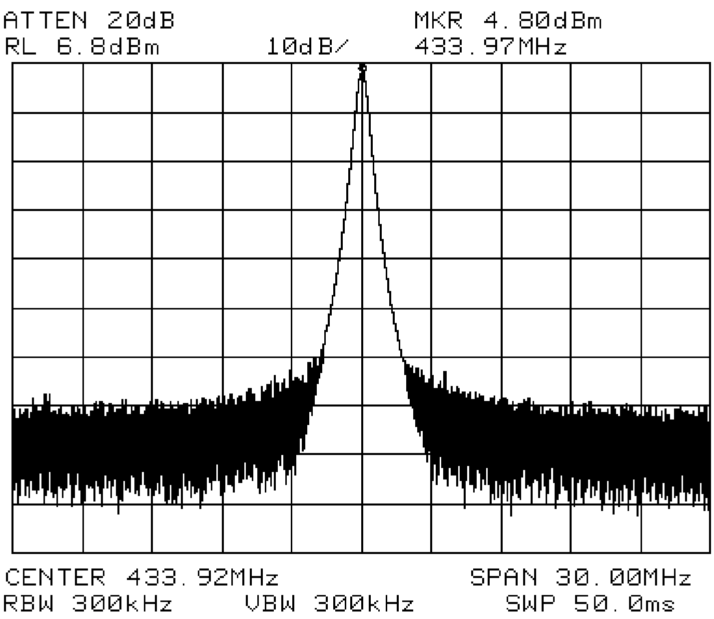
Figure 5-1 Test_Circuit

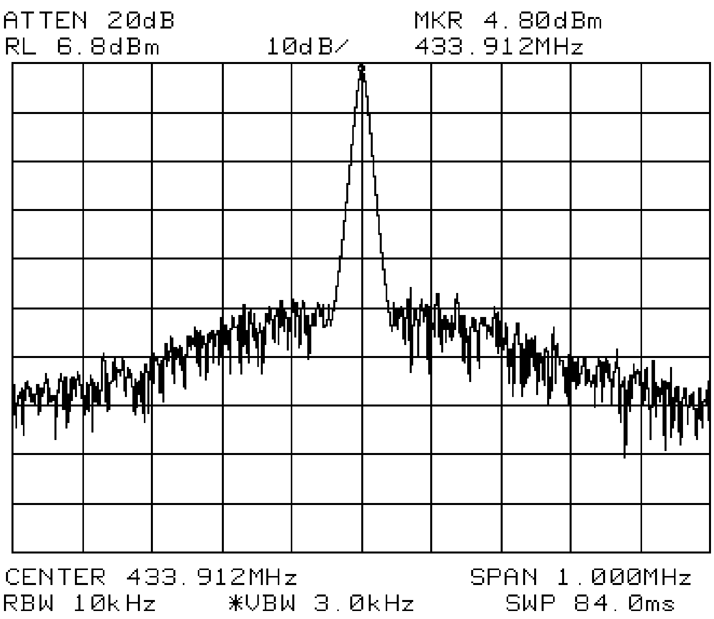
Table 5-4 Transfermin schematic to 50 Ohms

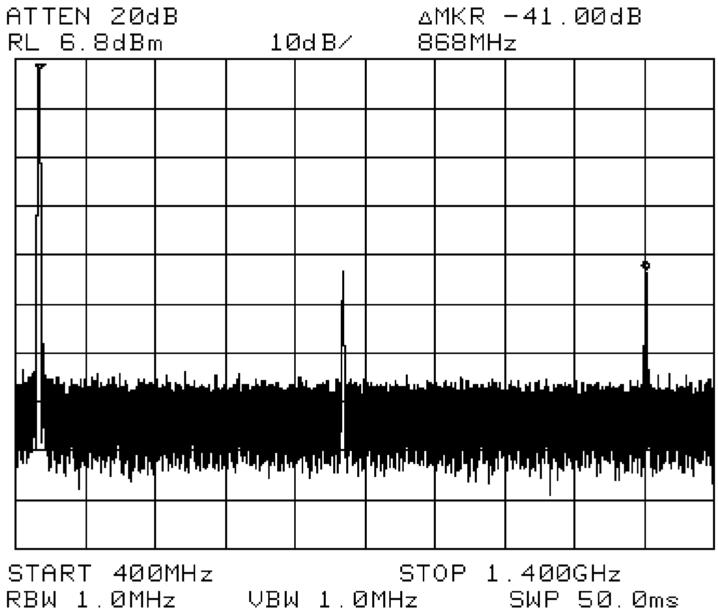
f=433 MHz		f=868 MHz	
L1	100 mH	L1	33 nH
L2	39 nH	L2	15 nH
C2	39 pF	C2	47 pF
C3	3.9 pF	C3	1.8 pF
C4	330 pF	C4	100 pF
C8	15 pF	C8	8.2 pF

5.3 Diagrams

Output spectrum at 433.92MHz at 50 Ohms






ATTEN 20dB
RL 6.8dBm
10dB/
ΔMKR -41.00dB
868MHz
START 400MHz
STOP 1.400GHz
RBW 1.0MHz
VBW 1.0MHz
SWP 50.0ms