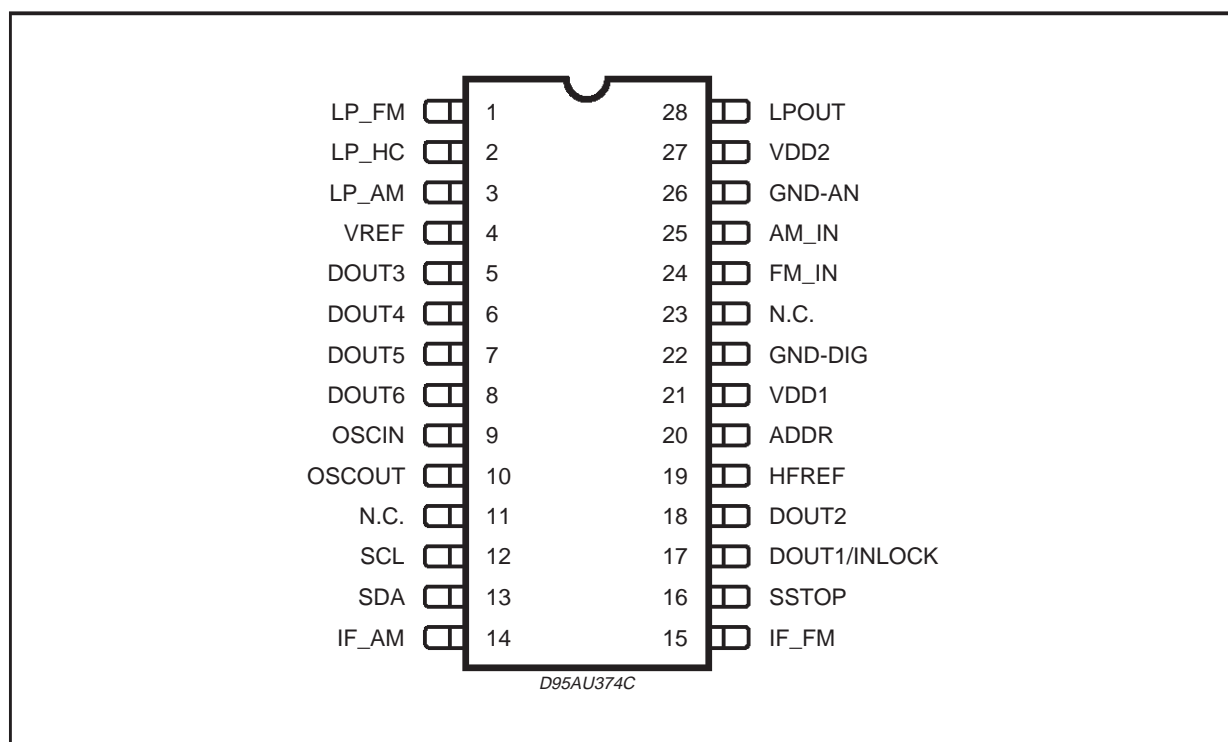


TDA7427A

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------|-------------------------|---------------|------|
| V _{DD1} | Supply Voltage | - 0.3 to + 7 | V |
| V _{DD2} | Supply Voltage | - 0.3 to + 11 | V |
| P _{tot} | Total Power Dissipation | 300 | mW |
| T _{stg} | Storage Temperature | - 55 to + 150 | °C |
| T _{amb} | Ambient Temperature | -40 to + 85 | °C |

PIN CONNECTION



THERMAL DATA

| Symbol | Parameter | TSSOP28 | SO 28 | Unit |
|-----------------------|-------------------------------------|---------|-------|------|
| R _{th j-amb} | Thermal Resistance Junction-Ambient | 160 | 65 | °C/W |

PIN DESCRIPTION

| PIN | SYMBOL | DESCRIPTION |
|-----|---------|--|
| 1 | LP_FM | Filter OPAMP input, charge pump output (FM mode) |
| 2 | LP_HC | Filter OPAMP input, charge pump output (high current mode) |
| 3 | LP_AM | Filter OPAMP input, charge pump output (AM mode) |
| 4 | VREF | OPAMP reference voltage |
| 5 | DOUT3 | Digital Output 3 (open collector) |
| 6 | DOUT4 | Digital Output 4 (open collector) |
| 7 | DOUT5 | Digital Output 5 (open collector) |
| 8 | DOUT6 | Digital Output 6 (open collector) |
| 9 | OSCIN | Reference Oscillator Input |
| 10 | OSCOU | Reference Oscillator Output |
| 11 | N.C. | Not connected |
| 12 | SCL | I ² C bus clock input |
| 13 | SDA | I ² C bus data I/O |
| 14 | IF_AM | IF counter HF input |
| 15 | IF_FM | IF counter VHF input |
| 16 | SSTOP | IF counter result output |
| 17* | DOUT1 | Digital output 1 (push-pull) |
| 17* | INLOCK | Inlock detector output |
| 18 | DOUT2 | Digital Output 2 (open collector) |
| 19 | HF-REF | HF reference pin |
| 20 | ADDR | I ² C bus address pin |
| 21 | VDD1 | Supply Voltage |
| 22 | GND-DIG | Digital ground |
| 23 | N.C. | Not connected |
| 24 | FM_IN | High frequency input FM |
| 25 | AM_IN | High frequency input AM |
| 26 | GND-AN | Analog ground |
| 27 | VDD2 | Supply Voltage |
| 28 | LP_OUT | Filter OPAMP output |

* Pin function is selectable by software (see software specification)

TDA7427A

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$; $V_{DD1} = 5\text{V}$; $V_{DD2} = 10\text{V}$; $f_{osc} = 4\text{MHz}$; unless otherwise specified).

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|--|---------------------------------------|-------|------|------|------------------|
| V_{DD1} | Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| V_{DD2} | Supply Voltage | | | 9.0 | 11.0 | V |
| I_{DD1} | Supply Current | no output load | 2 | 4 | 6 | mA |
| I_{DD2} | Supply Current | PLL locked | 1 | 2 | 3 | mA |
| $I_{DD1\ STB}$ | Supply Current | Standby mode | | | 1 | μA |
| RF INPUT (AM_IN, FM_IN) | | | | | | |
| f_{iAM} | Input Frequency AM | $V_i = 100\text{mV}_{rms}$ sinusoidal | 0.5 | | 64 | MHz |
| f_{iFM} | Input Frequency FM | $V_i = 100\text{mV}_{rms}$ sinusoidal | 30 | | 200 | MHz |
| V_{iMIN} | Min Input Voltage AM | 0.5 to 16MHz range sinusoidal | | | 30 | mVrms |
| V_{iMAX} | Max Input Voltage AM | 0.6 to 16MHz range sinusoidal | 600 | | | mVrms |
| V_{iMIN} | Min Input Voltage FM | 70 to 120MHz range sinusoidal | | | 30 | mVrms |
| V_{iMAX} | Max Input Voltage FM | 70 to 120MHz range sinusoidal | 600 | | | mVrms |
| Z_{in} | Input Impedance FM input | | 3 | 4 | 5 | $\text{K}\Omega$ |
| Z_{in} | Input Impedance AM input | | 3 | 4 | 5 | $\text{K}\Omega$ |
| IF COUNTER (IF_AM, IF_FM) | | | | | | |
| f_{iAM} | Input Frequency range AM | $V_i = 100\text{mV}_{rms}$ | 0.400 | | 11 | MHz |
| f_{iAM} | Input Frequency range FM | $V_i = 100\text{mV}_{rms}$ | 10 | | 11 | MHz |
| V_{iMIN} | Min Input Voltage AM IF pin | $f_{in} = 455\text{kHz}$ | | | 30 | mVrms |
| V_{iMIN} | Min Input Voltage FM IF pin | $f_{in} = 10.7\text{MHz}$ | | | 30 | mVrms |
| V_{iMAX} | Max Input Voltage AM IF pin | $f_{in} = 455\text{kHz}$ | 600 | | | mVrms |
| V_{iMAX} | Max Input Voltage FM IF pin | $f_{in} = 10.7\text{MHz}$ | 600 | | | mVrms |
| Z_{in} | Input Impedance FM IF pin | | 3 | 4 | 5 | $\text{K}\Omega$ |
| Z_{in} | Input Impedance AM IF pin | | 3 | 4 | 5 | $\text{K}\Omega$ |
| BUS INTERFACE | | | | | | |
| T_j | Noise Suppression Time Constant on SCL, SDA Input | | | 50 | | ns |
| f_{SCL} | SCL Clock Frequency | | | | 400 | kHz |
| t_{AA} | SCL Low to SDA Data Valid | | 300 | | | ns |
| t_{buf} | Time the bus must be free for the new transmission | | 4.7 | | | μs |
| $t_{HD-START}$ | START Condition hold time | | 4.0 | | | μs |
| t_{LOW} | Clock Low Period | | 4.7 | | | μs |
| t_{HIGH} | Clock High Period | | 4.0 | | | μs |
| t_{SU-SDA} | Start Condition Setup Time | | 4.7 | | | μs |
| $t_{HD-DATA}$ | Data Input Hold Time | | | | 1 | μs |
| $t_{SU-DATA}$ | Data Input Setup Time | | 250 | | | ns |
| t_R | SDA & SCL Rise Time | | | | 1 | μs |
| t_F | SDA & SCL Full Time | | | 0.3 | | μs |
| $t_{SU-STOP}$ | Stop Condition Setup Time | | 4.7 | | | μs |
| t_{DH} | DATA OUT Time | | 300 | | | ns |

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|--|--------------------------------------|---|-----------------------|------|-----------------|------------------|
| V _{IL} | Input Low Voltage | | | | 1 | V |
| V _{IH} | Input High Voltage | | 3 | | | V |
| I _{IN} | Input Current | | -5 | | +5 | μA |
| V _{OUT} | Output Voltage SDA acknowledge | I _O = 1.6mA | | 0.15 | 0.4 | V |
| OSCILLATOR | | | | | | |
| t _{bu} | Build Up Time | f _{out} = 4MHz | | | 100 | ms |
| C _{in} | Internal Capacitance | | | 20 | | pF |
| C _{OUT} | Internal Capacitance | f _{osc} = 4MHz | | 20 | | pF |
| Z _{in} | Input Impedance | f _{osc} = 4MHz | | | 100 | KΩ |
| V _{in} | Input Voltage (for Slave Mode) | f _{IN} = 4 to 13MHz (Sinus) capacitance coupling | 300 | | V _{DD} | mV _{pp} |
| f _{in} | Max Input frequency (for Slave Mode) | V _{IN} = 600mV _{PP} (Sinus) | 30 | | | MHz |
| LOOP FILTER (LP_FM, LP_AM, LP_HC, LP_OUT) | | | | | | |
| I _{IN} | Input Leakage Current (*) | V _{IN} = GND; PD _{out} = Tristate (1) | -1 | 0.1 | 1 | μA |
| I _{IN} | Input Leakage Current (*) | V _{IN} = V _{DD1} ; PD _{out} = Tristate (1) | -1 | 0.1 | 1 | μA |
| V _{OL} | Output Voltage Low | I _{IN} = -0.2mA | | 0 | 0.5 | V |
| V _{OH} | Output Voltage High | I _{OUT} = 0.2mA | 9.5 | 10 | | V |
| I _{OUT} | Output Current Sink | | 10 | 30 | | mA |
| I _{OUT} | Output Current Source | V _{out} = 0.5 to 9.5V | 10 | 30 | | mA |
| DOUT1/SSTOP (push-pull outputs) | | | | | | |
| V _{OL} | Output Voltage Low | I _{OUT} = -0.1mA | | 0.1 | 0.2 | V |
| V _{OH} | Output Voltage High | I _{OUT} = 0.1mA | V _{DD1} *0.2 | 4.9 | | V |
| DOUT2 to 6 (open collector outputs) | | | | | | |
| I _{OUT} | Output leakage Current | V _{OUT} = 10V | -1 | 0.1 | 1 | mA |
| V _{OL} | Output Voltage Low | I _{OUT} = -1mA | | 0.2 | 0.5 | V |
| I _{OUT} | Output Current Sink | V _{out} = 0.5 to 9.5V | | 3 | 5 | mA |

1) PD = Phase Detector

(*) LP_FM and LP_HC pins only

GENERAL DESCRIPTION

This circuit contains a frequency synthesiser and a loop filter for use in FM/AM radio tuning systems. Only a VCO is required to build a complete PLL system. For auto search/stop operation an IF counter system is available.

For FM and SW AM application, the counter works in a two-stage configuration. The first stage is a swallow counter with a two modulus (:32/33) precounter. The second stage is an 11-bit programmable counter.

For LW and MW application, a 16-bit programmable counter is available.

The circuit receives the scaling factors for the programmable counters and the values of the reference frequencies via a I²C bus interface.

The reference frequency is generated by an internal XTAL oscillator followed by the reference divider. The device can operate with XTAL oscillator between 4 and 13MHz either in master mode and in slave mode.

The reference and step frequencies are free selectable. (XTAL frequency divided by an integer value). The outputs signals of the phase detector are switching the programmable current sources. The loop filter integrates their currents to a DC voltage.

Values of the current sources are programmable by 6 bits also received via the I²C bus.

To minimize the noise induced by the digital part of the system, a separate power supply supplies the internal loop filter amplifier. The loop gain can be set for different conditions by setting the current values of the charge/pump generator.

IF COUNTER SYSTEM

Two separate inputs are available for AM and FM IF signals. The level of integration is adjustable by six different measuring cycle times.

The tolerance of the accepted count value is adjustable, to reach an optimum compromise for search speed and precision of the evaluation.

For the FM range the center frequency of the measured count value is adjustable in 32 steps, to get the possibility of fitting the IF filter tolerance. In the AM range an IF frequency of 448 to 479KHz (10.684 to 10.715MHz for AM up-conversion) with 1KHz steps is available.

PLL FREQUENCY SYNTHESIZER

Input Amplifiers

The signals applied on AM and FM inputs are amplified to get a logic level in order to drive the frequency dividers.

The typical input impedance for FM and AM inputs is 4kΩ.

Table 1. Address Organization

| FUNCTION | SUBAD | MSB | | | | | | | LSB | |
|-----------------|-------|---------|--------|-------|-------|-------|-------|-------|-------|--|
| | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| PLL CHARGE PUMP | 00H | LPIN1/2 | CURRH | B1 | B0 | A3 | A2 | A1 | A0 | |
| PLL COUNTER | 01H | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 | |
| PLL COUNTER | 02H | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | |
| PLL REF COUNTER | 03H | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | |
| PLL REF COUNTER | 04H | RC15 | RC14 | RC13 | RC12 | RC11 | RC10 | RC9 | RC8 | |
| PLL LOCK DETECT | 05H | LDENA | INLOCK | D3 | D2 | D1 | D0 | PM1 | PM0 | |
| IFC REF COUNTER | 06H | IRC7 | IRC6 | IRC5 | IRC4 | IRC3 | IRC2 | IRC1 | IRC0 | |
| IFC REF COUNTER | 07H | IFCM1 | IFCM0 | IRC13 | IRC12 | IRC11 | IRC10 | IRC9 | IRC8 | |
| IFC CONTROL | 08H | IFENA | - | - | - | - | EW2 | EW1 | EW0 | |
| IFC CONTROL | 09H | IFS2 | IFS1 | IFS0 | CF4 | CF3 | CF2 | CF1 | CF0 | |
| OSC ADJUST | 0AH | - | - | - | OSC4 | OSC3 | OSC2 | OSC1 | OSC0 | |
| PORT EXTENSION | 0BH | - | - | DOUT3 | DOUT4 | DOUT5 | DOUT6 | DOUT2 | DOUT1 | |

Figure 1. FM and AM (SW) operation (swallow mode)

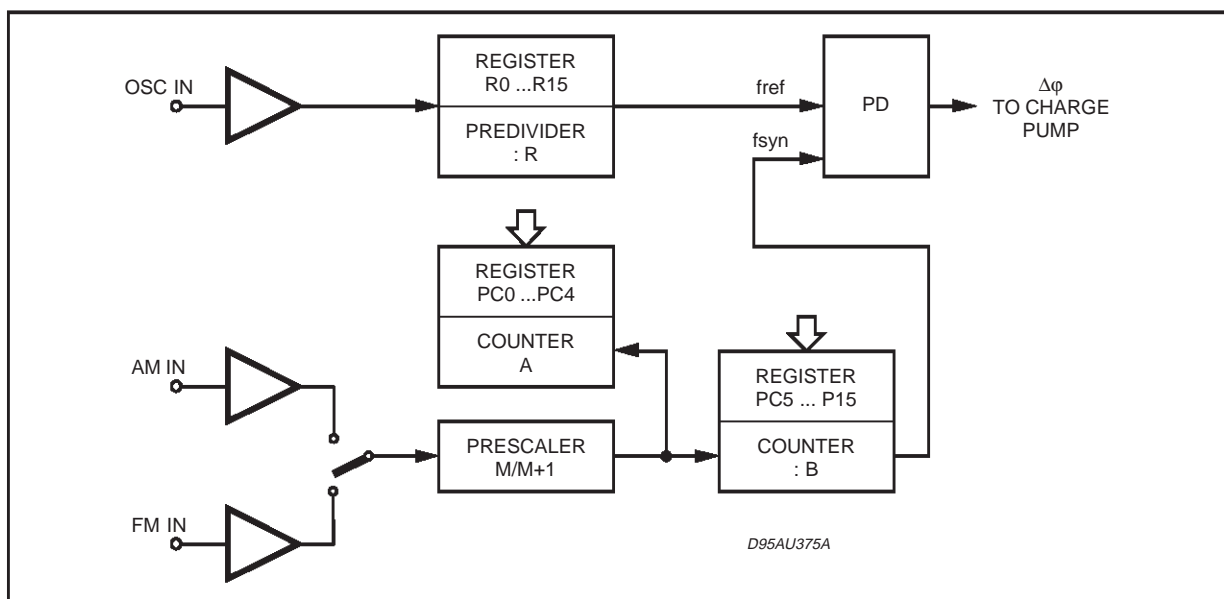
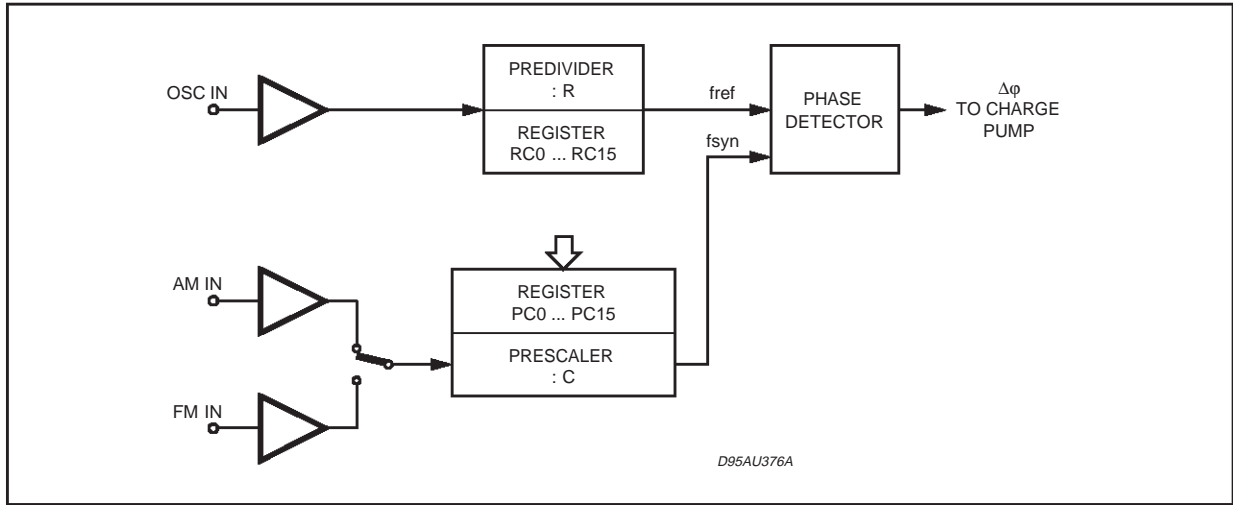


Table 2. Control Register Functions.

| REGISTER NAME | FUNCTION |
|---------------|--|
| PC | Programmable counter for VCO frequency |
| RC | Reference counter PLL |
| IRC | Reference counter IF |
| IFCM | IF counter mode selector |
| EW | Frequency error window IF counter |
| IFENA | Enable IFRC |
| CF | Center frequency IF counter |
| IFS | Sampling time IF counter |
| PM | Stby, FM, AM, AM swallow mode selector |
| D | Programmable delay and phase error for lock detector |
| LPIN1/2 | Loop filter input select |
| PLLSTOP | PLL stop |
| A | Charge pump high current |
| B | Charge pump low current |
| LDENA | Lock detector enable |
| CURRH | Set current high |
| OSC | Oscillator adjust |
| DOUT1 | Push pull output 5V |
| DOUT2...6 | Open collector output |
| INLOCK | Lock detector output |

Figure 2. AM direct mode operation for SW, MW and LW



DIVIDER FROM VCO FREQUENCY TO REFERENCE FREQUENCY

This divider provides a low frequency f_{SYN} which phase is compared with the reference frequency f_{REF} . It is controlled by the registers PC0 to PC4 and PC5 to PC15

OPERATING MODES

Four operating modes are available for PLL; they are user programmable with the Mode PM registers (see table below).

| PM0 | PM1 | Operating Mode |
|-----|-----|----------------|
| 0 | 0 | Standby |
| 1 | 0 | AM (swallow) |
| 0 | 1 | AM (direct) |
| 1 | 1 | FM |

- **Standby mode:** in this mode all device functions are stopped. This allows low current consumption without loss of information in all registers. The pin LP-OUT is forced to 0V, and all data registers are set to EFH. The oscillator keeps running.

- **FM and AM (SW) Swallow Mode (SW):** in this mode the FM or AM signal is applied to a 32/33 prescaler, which is controlled by a 5 bit divider 'A'. The 5 bit register (PC0 to PC4) controls this divider. In parallel the output of the prescaler is connected to a 11 bit divider 'B'. (PC5 to PC15).

$$f_{OSC} = (R+1) \cdot f_{REF}$$

Dividing range calculation :

$$f_{VCO} = [33 \cdot A + (B + 1 - A) \cdot 32] \cdot f_{REF}$$

$$f_{VCO} = (32 \cdot B + A + 32) \cdot f_{REF}$$

Important: for correct operation $A \leq 32$, $B \geq A$, with A and B variable values of the dividers).

- **AM direct mode:** the AM signal is applied directly to the 16 bit static divider 'C'. (PC0 to PC15)

$$f_{OSC} = (R + 1) \cdot f_{REF}$$

Dividing range:

$$f_{VCO} = (C + 1) \cdot f_{REF}$$

THREE STATE PHASE COMPARATOR

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF} . This phase error signal drives the charge pump current generator (fig. 3)

CHARGE PUMP CURRENT GENERATOR

This stage generates signed pulses of current. The phase error signal decides the duration and polarity of those pulses.

The current absolute values are programmable by A0, A1, A2 registers for high current and B0, B1, registers for low current.

LOW NOISE CMOS OP-AMP

An internal voltage divider at pin VREF connects the positive input of the low noise Op-Amp. The charge pump output connects the negative input. This internal amplifier in cooperation with external components can provide an active filter.

Figure 3. Phase comparator waveforms

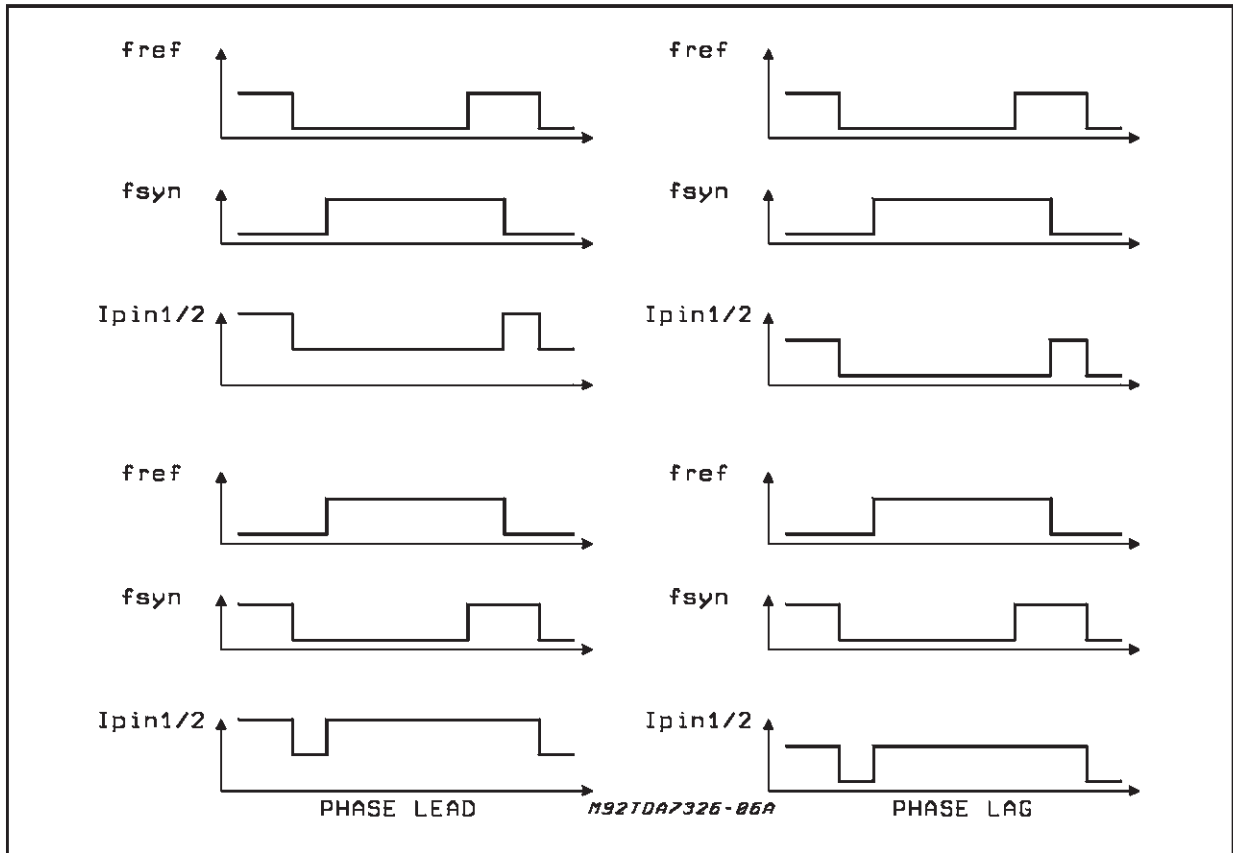
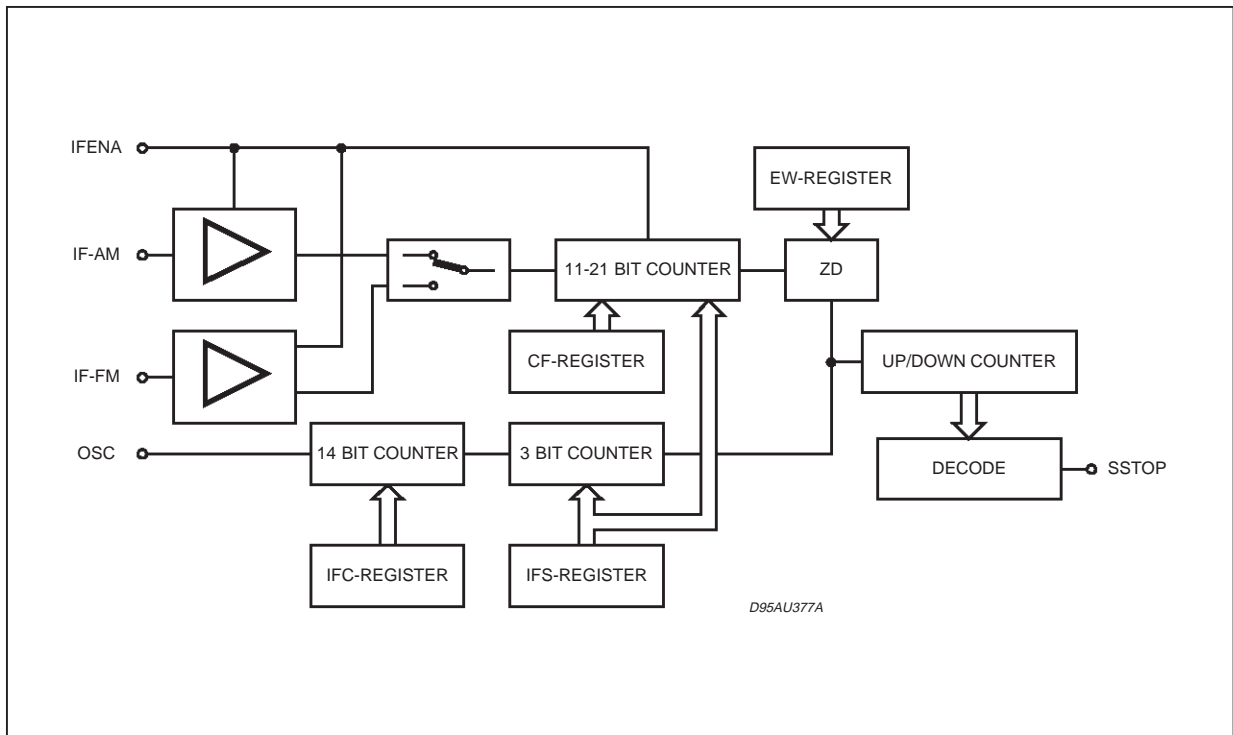


Figure 4. IF Counter internal block diagram



The negative input is switchable to three input pins (LPIN 1, LPIN 2 and LPIN 3) to increase the flexibility in application. This feature allows two separate active filters for different applications

A logical "1" in the LPIN 1/2 register activates pin LPIN 1, otherwise pin LPIN 2 is active. While the high current mode is activated LPIN 3 is switched on.

INLOCK DETECTOR

The charge pump can be switched in low current mode either via software or automatically by the inlock detector by setting bit LDENA to "1".

The charge pump is forced in low current mode when a phase difference of 10-40 µsec is reached.

A phase difference larger then the programmed values will switch the charge pump immediately in the high current mode.

Programmable delays are available for inlock detection.

IF COUNTER SYSTEM (AM/FM/AM - UPC MODES)

The if counter works in modes controlled by IFCM register (see table):

| IFCM1 | IFCM0 | FUNCTION |
|-------|-------|-------------------------------|
| 0 | 0 | NOT USED |
| 0 | 1 | FM MODE |
| 1 | 0 | AM MODE |
| 1 | 1 | 10.7MHz AM UP CONVERSION MODE |

Typical input impedance for IF inputs is 4KΩ.

A sample timer to generate the gate signal for the main counter is build with a 14-bit programmable counter to have the possibility to use any crystal oscillator frequency. In FM mode 6.25KHz in AM

mode a 1KHz signal is generated. This is followed by an asynchronous divider to generate different sampling times (see fig. 4).

Intermediate Frequency Main Counter

This counter is a 11/21 bits synchronous autoreload down-counter. Four bits are programmable to have the possibility for an adjust to the frequency of the CF filter. The counter length is automatically adjusted to the chosen sampling time and the counter mode (AM, FM, AM-UPC).

At the start the counter will be loaded with a defined value which is an equivalent to the divider value ($t_{sample} \cdot f_{IF}$).

If a correct frequency is applied to the IF counter frequency inputs IF-AM IF-FM, at the end of the sampling time the main counter is changing its state from 0 H to 1FFFFFFH.

This is detected by a control logic. The frequency range inside which a successful count results is detected is adjustable by bits EW 0,1,2.

Adjustment of the Measurement Sequence Time

The precision of the measurements is adjustable by controlling the discrimination window .

This is adjustable by programming the control registers EW0...EW2.

The measurement time per cycle is adjustable by setting the Register IFS0 - IFS2.

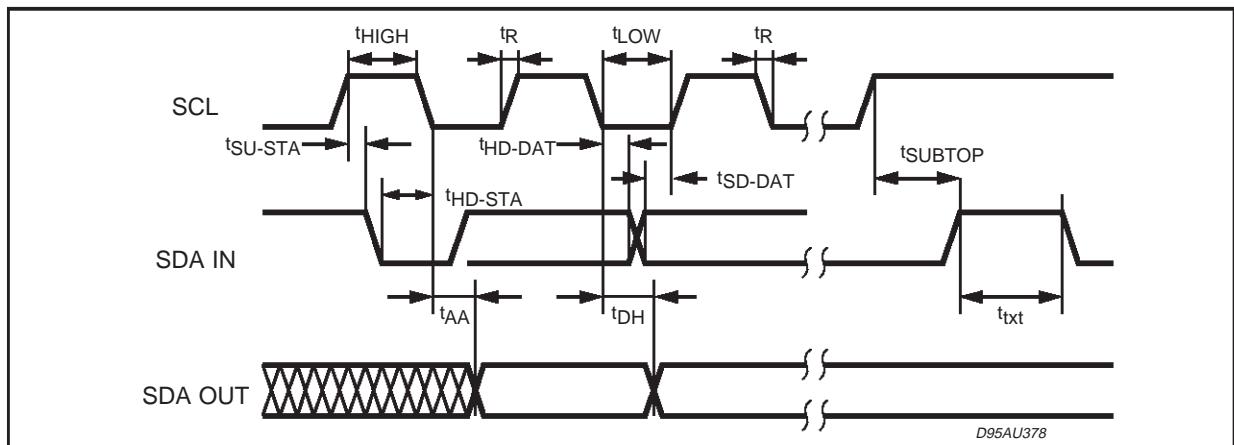
Adjust of the Frequency Value

The center frequency of the discrimination window is adjustable by the control register "CF0" to "CF4". (see data byte specification).

Port Extension and additional functions

Five digital open collector outputs and one digital push-pull output are available in application mode. This digital ports are controlled by the data bits DOUT1-DOUT6.

Figure 5. I²C Bus timing diagram



I²C BUS INTERFACE DESCRIPTION

The TDA7427A supports the I²C bus protocol. This protocol defines any device that sends data into the bus as a transmitter and the receiving device as the receiver. The device that controls the transfer is the master and the device being controlled is the slave. The master always initiates data transfer and provides the clock to transmit or receive operations.

Data Transition

Data transition on the SDA line must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as START or STOP condition.

Start Condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The TDA7427A continuously monitors the SDA and SCL lines for a valid START and will not respond to any command if this condition has not been met.

Stop Condition

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminate the communication between the devices and forces the bus interface of the TDA7427A into the initial condition.

Acknowledge

Indicates a successful data transfer. The transmit-

ter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it has receive the eight bits of data correctly.

Data transfer

During data transfer the TDA7427A samples the SDA line on the leading edge of the SCL clock. Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

Device Addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device it is addressing. The most significant 6 bits of the slave address are the device type identifier.

The TDA7427A frequency synthesizer device type is fixed as "110001"

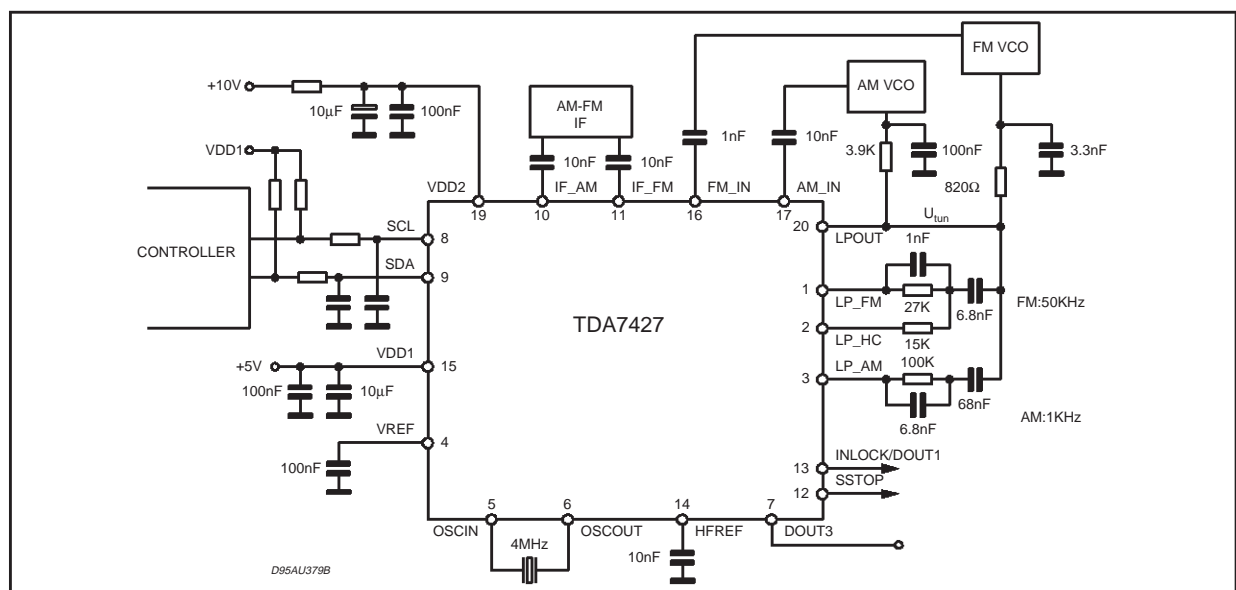
The next significant bit is used to address a particular device of the previous defined type connected to the bus. The state of the hardwired A0 pin defines the state of this address bit. So up to two devices could be connected on the same bus. The last bit of the instruction defines the type of operation to be performed:

- When set to "1", a read operation is selected
- When set to "0", a write operation is selected

The chip selection is accomplished by setting the bit of the chip address to the corresponding status of the A0 input.

All TDA7427A connected to the bus will compare their own hardwired address with the slave ad-

Figure 6. Application with two loop filters



Data Byte Specification

CHARGE PUMP CONTROL

| MSB | | | | LSB | | | | FUNCTION |
|---------|-------|----|----|-----|----|----|----|--------------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | | | | 0 | 0 | 0 | 0 | High current = 0mA |
| | | | | 0 | 0 | 0 | 1 | High current = 0.5mA |
| | | | | 0 | 0 | 1 | 0 | High current = 1.0mA |
| | | | | 0 | 0 | 1 | 1 | High current = 1.5mA |
| | | | | 0 | 1 | 0 | 0 | High current = 2.0mA |
| | | | | 0 | 1 | 0 | 1 | High current = 2.5mA |
| | | | | 0 | 1 | 1 | 0 | High current = 3.0mA |
| | | | | 0 | 1 | 1 | 1 | High current = 3.5mA |
| | | | | 1 | 0 | 0 | 0 | High current = 4.0mA |
| | | | | 1 | 0 | 0 | 1 | High current = 4.5mA |
| | | | | 1 | 0 | 1 | 0 | High current = 5.0mA |
| | | | | 1 | 0 | 1 | 1 | High current = 5.5mA |
| | | | | 1 | 1 | 0 | 0 | High current = 6.0mA |
| | | | | 1 | 1 | 0 | 1 | High current = 6.5mA |
| | | | | 1 | 1 | 1 | 0 | High current = 7.0mA |
| | | | | 1 | 1 | 1 | 1 | High current = 7.5mA |
| | | 0 | 0 | | | | | Low current = 0µA |
| | | 0 | 1 | | | | | Low current = 50µA |
| | | 1 | 0 | | | | | Low current = 100µA |
| | | 1 | 1 | | | | | Low current = 150µA |
| | 0 | | | | | | | Select low Current |
| | 1 | | | | | | | Select high Current |
| 1 | | | | | | | | Select loop filter LP_FM |
| 0 | | | | | | | | Select loop filter LP_AM |
| LPIN1/2 | CURRH | B1 | B0 | A3 | A2 | A1 | A0 | Subaddress = 00H |

PLL COUNTER 1 (LSB)

| MSB | | | | LSB | | | | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|---------------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LSB = 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | LSB = 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | LSB = 2 |
| | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | LSB = 252 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | LSB = 253 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | LSB = 254 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | LSB = 255 |
| PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 | Bit name Subaddress = 01H |

TDA7427A

PLL COUNTER 2 (MSB)

| MSB | | | | | | | LSB | | FUNCTION |
|------|------|------|------|------|------|-----|-----|--|----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MSB = 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | MSB = 256 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | MSB = 512 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | MSB = 64768 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | MSB = 65024 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | MSB = 65280 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | MSB = 65536 | |
| PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | Bit name Subaddress = 02H | |

Swallow mode: $fvco/fsyn = LSB + MSB + 32$

Direct mode: $fvco/fsyn = LSB + MSB + 1$

PLL REFERENCE COUNTER 1 (LSB)

| MSB | | | | | | | LSB | | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|--|----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LSB = 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | LSB = 1 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | LSB = 2 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | LSB = 252 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | LSB = 253 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | LSB = 254 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | LSB = 255 | |
| RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | Bit name Subaddress = 03H | |

PLL REFERENCE COUNTER 2 (MSB)

| MSB | | | | | | | LSB | | FUNCTION |
|------|------|------|------|------|------|-----|-----|--|----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MSB = 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | MSB = 256 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | MSB = 512 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | MSB = 64768 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | MSB = 65024 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | MSB = 65280 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | MSB = 65536 | |
| RC15 | RC14 | RC13 | RC12 | RC11 | RC10 | RC9 | RC8 | Bit name Subaddress = 04H | |

$f_{osc}/f_{REF} = LSB + MSB + 1$

LOCK DETECTOR & PLL MODE CONTROL

| MSB | | | | | | | LSB | | FUNCTION |
|-------|--------|----|----|----|----|-----|-----|--|----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| | | | | | | 0 | 0 | PLL standby mode | |
| | | | | | | 0 | 1 | PLL AM swallow mode | |
| | | | | | | 1 | 0 | PLL AM direct mode | |
| | | | | | | 1 | 1 | PLL FM mode | |
| | | | | 0 | 0 | | | PD phase difference threshold 10ns | |
| | | | | 0 | 1 | | | PD phase difference threshold 20ns | |
| | | | | 1 | 0 | | | PD phase difference threshold 30ns | |
| | | | | 1 | 1 | | | PD phase difference threshold 40ns | |
| | | 0 | 0 | | | | | Not used in application mode | |
| | | 0 | 1 | | | | | Activation delay = 4 · fref | |
| | | 1 | 0 | | | | | Activation delay = 6 · fref | |
| | | 1 | 1 | | | | | Activation delay = 8 · fref | |
| | 0 | | | | | | | Digital output 1 at pin "dout1/inlock" | |
| | 1 | | | | | | | Inlock information at pin "dout1/inlock" | |
| 0 | | | | | | | | No lock detector controlled chargepump | |
| 1 | | | | | | | | Lock detector controlled chargepump | |
| LDENA | INLOCK | D3 | D2 | D1 | D0 | PM1 | PM0 | Bit name Subaddress = 05H | |

IF COUNTER REFERENCE CONTROL 1 (LSB)

| MSB | | | | | | | LSB | | FUNCTION |
|------|------|------|------|------|------|------|------|---------------------------|----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LSB = 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | LSB = 1 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | LSB = 2 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | LSB = 252 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | LSB = 253 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | LSB = 254 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | LSB = 255 | |
| IRC7 | IRC6 | IRC5 | IRC4 | IRC3 | IRC2 | IRC1 | IRC0 | Bit name Subaddress = 06H | |

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IF COUNTER REFERENCE CONTROL 2 (MSB) AND IF COUNTER MODE SELECT

| MSB | | | | | | | | LSB | | FUNCTION |
|-------|-------|-------|-------|-------|-------|------|------|---|------------------|----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MSB = 0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | MSB = 256 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | MSB = 512 | | |
| | | 1 | 1 | 1 | 1 | 0 | 1 | MSB = 15616 | | |
| | | 1 | 1 | 1 | 1 | 1 | 0 | MSB = 15872 | | |
| | | 1 | 1 | 1 | 1 | 1 | 1 | MSB = 16128 | | |
| 0 | 0 | | | | | | | NOT USED IN APPLICATION MODE | | |
| 0 | 1 | | | | | | | IF counter FM mode | | |
| 1 | 0 | | | | | | | IF counter AM mode | | |
| 1 | 1 | | | | | | | IF counter AM 10.7MHz upconversion mode | | |
| IFCM1 | IFCM0 | IRC13 | IRC12 | IRC11 | IRC10 | IRC9 | IRC8 | Bit name | Subaddress = 07H | |

$f_{osc}/f_{tim} = LSB + MSB + 1$

IF COUNTER CONTROL 1

| MSB | | | | | | | | LSB | | FUNCTION |
|------|-----|-----|-----|-----|-----|-----|-----|--|------------------|----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | |
| | | | | | 0 | 0 | 0 | don't use | | |
| | | | | | 0 | 0 | 1 | don't use | | |
| | | | | | 0 | 1 | 1 | EW delta f = $\pm 6.25\text{kHz}$ (FM); $\pm 1\text{kHz}$ (AM; AM-UPC) | | |
| | | | | | 1 | 0 | 0 | EW delta f = $\pm 12.5\text{kHz}$ (FM); $\pm 2\text{kHz}$ (AM; AM-UPC) | | |
| | | | | | 1 | 0 | 1 | EW delta f = $\pm 25\text{kHz}$ (FM); $\pm 4\text{kHz}$ (AM; AM-UPC) | | |
| | | | | | 1 | 1 | 0 | EW delta f = $\pm 50\text{Hz}$ (FM); $\pm 8\text{kHz}$ (AM; AM-UPC) | | |
| | | | | | 1 | 1 | 1 | EW delta f = $\pm 100\text{kHz}$ (FM); $\pm 16\text{kHz}$ (AM; AM-UPC) | | |
| | X | X | X | X | | | | don't use | | |
| 0 | | | | | | | | IF counter disabled / stand by | | |
| 1 | | | | | | | | IF counter enabled | | |
| FENA | FR3 | FR2 | FR1 | FR0 | EW2 | EW1 | EW0 | Bit name | Subaddress = 08H | |

IF COUNTER CONTROL 2

| MSB | | | | LSB | | | | FUNCTION |
|------|------|------|-----|-----|-----|-----|-----|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | | | 0 | 0 | 0 | 0 | 0 | fcenter = 10.60000MHz (FM) 448KHz (AM) 10.688MHz (AM UPC) |
| | | | 0 | 0 | 0 | 0 | 1 | fcenter = 10.60625MHz (FM) 449KHz (AM) 10.689MHz (AM UPC) |
| | | | 0 | 0 | 0 | 1 | 0 | fcenter = 10.61250MHz (FM) 450KHz (AM) 10.690MHz (AM UPC) |
| | | | 0 | 0 | 0 | 1 | 1 | fcenter = 10.61875MHz (FM) 451KHz (AM) 10.691MHz (AM UPC) |
| | | | 0 | 0 | 1 | 0 | 0 | fcenter = 10.62500MHz (FM) 452KHz (AM) 10.692MHz (AM UPC) |
| | | | 0 | 0 | 1 | 0 | 1 | fcenter = 10.63125MHz (FM) 453KHz (AM) 10.693MHz (AM UPC) |
| | | | 0 | 0 | 1 | 1 | 0 | fcenter = 10.63750MHz (FM) 454KHz (AM) 10.694MHz (AM UPC) |
| | | | 0 | 0 | 1 | 1 | 1 | fcenter = 10.64375MHz (FM) 455KHz (AM) 10.695MHz (AM UPC) |
| | | | 0 | 1 | 0 | 0 | 0 | fcenter = 10.65000MHz (FM) 456KHz (AM) 10.696MHz (AM UPC) |
| | | | 0 | 1 | 0 | 0 | 1 | fcenter = 10.65625MHz (FM) 457KHz (AM) 10.697MHz (AM UPC) |
| | | | 0 | 1 | 0 | 1 | 0 | fcenter = 10.66250MHz (FM) 458KHz (AM) 10.698MHz (AM UPC) |
| | | | 0 | 1 | 0 | 1 | 1 | fcenter = 10.66875MHz (FM) 459KHz (AM) 10.699MHz (AM UPC) |
| | | | 0 | 1 | 1 | 0 | 0 | fcenter = 10.67500MHz (FM) 460KHz (AM) 10.700MHz (AM UPC) |
| | | | 0 | 1 | 1 | 0 | 1 | fcenter = 10.68125MHz (FM) 461KHz (AM) 10.701MHz (AM UPC) |
| | | | 0 | 1 | 1 | 1 | 0 | fcenter = 10.68750MHz (FM) 462KHz (AM) 10.702MHz (AM UPC) |
| | | | 0 | 1 | 1 | 1 | 1 | fcenter = 10.69375MHz (FM) 463KHz (AM) 10.703MHz (AM UPC) |
| | | | 1 | 0 | 0 | 0 | 0 | fcenter = 10.70000MHz (FM) 464KHz (AM) 10.704MHz (AM UPC) |
| | | | 1 | 0 | 0 | 0 | 1 | fcenter = 10.70625MHz (FM) 465KHz (AM) 10.705MHz (AM UPC) |
| | | | 1 | 0 | 0 | 1 | 0 | fcenter = 10.71250MHz (FM) 466KHz (AM) 10.706MHz (AM UPC) |
| | | | 1 | 0 | 0 | 1 | 1 | fcenter = 10.71875MHz (FM) 467KHz (AM) 10.707MHz (AM UPC) |
| | | | 1 | 0 | 1 | 0 | 0 | fcenter = 10.72500MHz (FM) 468KHz (AM) 10.708MHz (AM UPC) |
| | | | 1 | 0 | 1 | 0 | 1 | fcenter = 10.73125MHz (FM) 469KHz (AM) 10.709MHz (AM UPC) |
| | | | 1 | 0 | 1 | 1 | 0 | fcenter = 10.73750MHz (FM) 470KHz (AM) 10.710MHz (AM UPC) |
| | | | 1 | 0 | 1 | 1 | 1 | fcenter = 10.74375MHz (FM) 471KHz (AM) 10.711MHz (AM UPC) |
| | | | 1 | 1 | 0 | 0 | 0 | fcenter = 10.75000MHz (FM) 472KHz (AM) 10.712MHz (AM UPC) |
| | | | 1 | 1 | 0 | 0 | 1 | fcenter = 10.75625MHz (FM) 473KHz (AM) 10.713MHz (AM UPC) |
| | | | 1 | 1 | 0 | 1 | 0 | fcenter = 10.76250MHz (FM) 474KHz (AM) 10.714MHz (AM UPC) |
| | | | 1 | 1 | 0 | 1 | 1 | fcenter = 10.76875MHz (FM) 475KHz (AM) 10.715MHz (AM UPC) |
| | | | 1 | 1 | 1 | 0 | 0 | fcenter = 10.77500MHz (FM) 476KHz (AM) 10.716MHz (AM UPC) |
| | | | 1 | 1 | 1 | 0 | 1 | fcenter = 10.78125MHz (FM) 477KHz (AM) 10.717MHz (AM UPC) |
| | | | 1 | 1 | 1 | 1 | 0 | fcenter = 10.78750MHz (FM) 478KHz (AM) 10.718MHz (AM UPC) |
| | | | 1 | 1 | 1 | 1 | 1 | fcenter = 10.79375MHz (FM) 479KHz (AM) 10.719MHz (AM UPC) |
| 1 | 1 | 1 | | | | | | tsample = 160µs (FM mode); 1ms (AM; AM-UPC) |
| 1 | 1 | 0 | | | | | | tsample = 320µs (FM mode); 2ms (AM; AM-UPC) |
| 1 | 0 | 1 | | | | | | tsample = 640µs (FM mode); 4ms (AM; AM-UPC) |
| 1 | 0 | 0 | | | | | | tsample = 1.280ms (FM mode); 8ms (AM; AM-UPC) |
| 0 | 1 | 1 | | | | | | tsample = 2.560ms (FM mode); 16ms (AM; AM-UPC) |
| 0 | 1 | 0 | | | | | | tsample = 5.120ms (FM mode); 32ms (AM; AM-UPC) |
| 0 | 0 | 1 | | | | | | tsample = 10.240ms (FM mode); 64ms (AM; AM-UPC) |
| 0 | 0 | 0 | | | | | | tsample = 20.480ms (FM mode); 128ms (AM; AM-UPC) |
| IFS2 | IFS1 | IFS0 | CF4 | CF3 | CF2 | CF1 | CF0 | bit same Subaddress = 09H |

TDA7427A

OSCILLATOR ADJUST

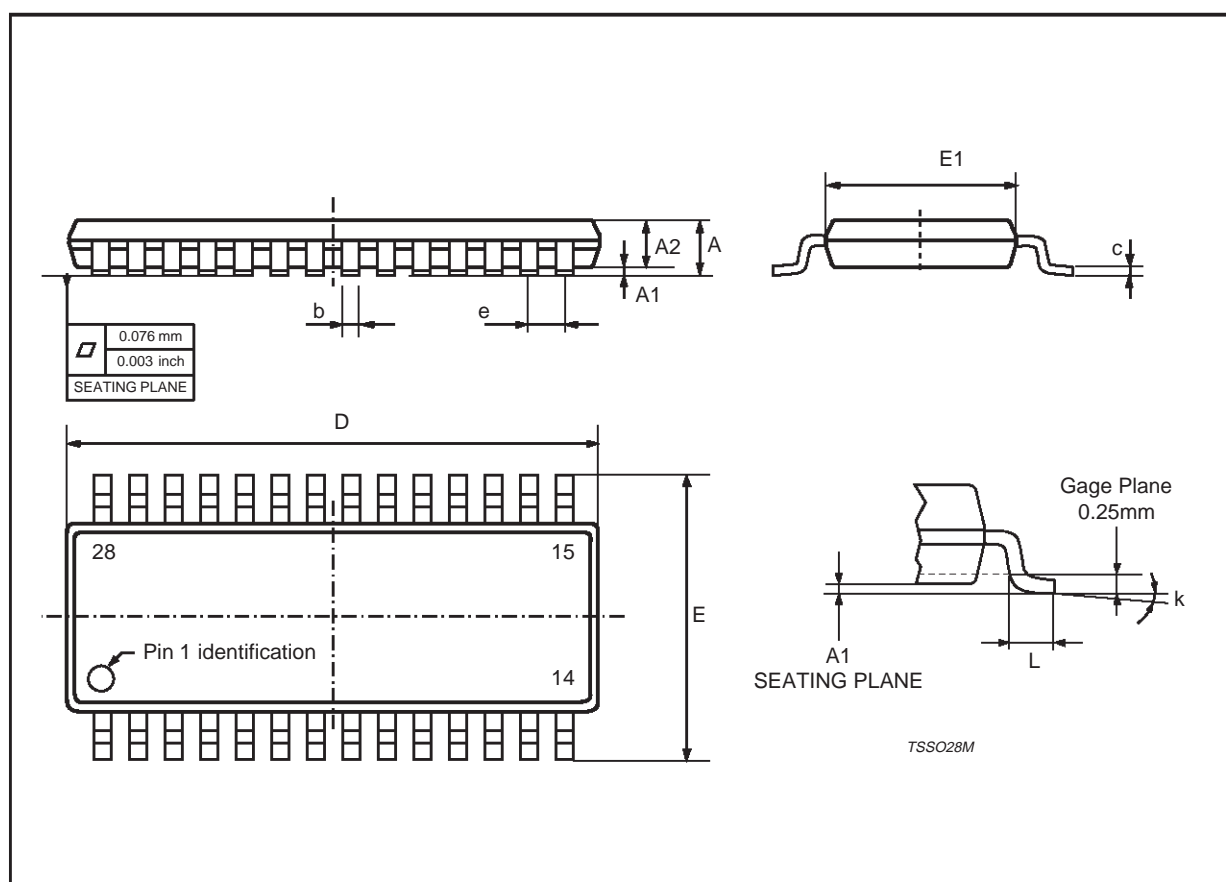
| MSB | | | | | | | | LSB | FUNCTION |
|-----|----|----|------|------|------|------|------|---------------------|------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| X | X | X | 0 | 0 | 0 | 0 | 0 | Cload 1,2 = 3pF | |
| X | X | X | 0 | 0 | 0 | 0 | 1 | Cload 1,2 = 4.25pF | |
| X | X | X | 0 | 0 | 0 | 1 | 0 | Cload 1,2 = 5.5pF | |
| X | X | X | 0 | 0 | 0 | 1 | 1 | Cload 1,2 = 6.75pF | |
| X | X | X | 0 | 0 | 1 | 0 | 0 | Cload 1,2 = 8pF | |
| X | X | X | 0 | 0 | 1 | 0 | 1 | Cload 1,2 = 9.25pF | |
| X | X | X | 0 | 0 | 1 | 1 | 0 | Cload 1,2 = 10.5pF | |
| X | X | X | 0 | 0 | 1 | 1 | 1 | Cload 1,2 = 11.75pF | |
| X | X | X | 0 | 1 | 0 | 0 | 0 | Cload 1,2 = 13pF | |
| X | X | X | 0 | 1 | 0 | 0 | 1 | Cload 1,2 = 14.25pF | |
| X | X | X | 0 | 1 | 0 | 1 | 0 | Cload 1,2 = 15.5pF | |
| X | X | X | 0 | 1 | 0 | 1 | 1 | Cload 1,2 = 16.75pF | |
| X | X | X | 0 | 1 | 1 | 0 | 0 | Cload 1,2 = 18pF | |
| X | X | X | 0 | 1 | 1 | 0 | 1 | Cload 1,2 = 19.25pF | |
| X | X | X | 0 | 1 | 1 | 1 | 0 | Cload 1,2 = 20.5pF | |
| X | X | X | 0 | 1 | 1 | 1 | 1 | Cload 1,2 = 21.75pF | |
| X | X | X | 1 | 0 | 0 | 0 | 0 | Cload 1,2 = 23pF | |
| X | X | X | 1 | 0 | 0 | 0 | 1 | Cload 1,2 = 24.25pF | |
| X | X | X | 1 | 0 | 0 | 1 | 0 | Cload 1,2 = 25.5pF | |
| X | X | X | 1 | 0 | 0 | 1 | 1 | Cload 1,2 = 26.75pF | |
| X | X | X | 1 | 0 | 1 | 0 | 0 | Cload 1,2 = 28pF | |
| X | X | X | 1 | 0 | 1 | 0 | 1 | Cload 1,2 = 29.25pF | |
| X | X | X | 1 | 0 | 1 | 1 | 0 | Cload 1,2 = 30.5pF | |
| X | X | X | 1 | 0 | 1 | 1 | 1 | Cload 1,2 = 31.75pF | |
| X | X | X | 1 | 1 | 0 | 0 | 0 | Cload 1,2 = 33pF | |
| X | X | X | 1 | 1 | 0 | 0 | 1 | Cload 1,2 = 34.25pF | |
| X | X | X | 1 | 1 | 0 | 1 | 0 | Cload 1,2 = 35.5pF | |
| X | X | X | 1 | 1 | 0 | 1 | 1 | Cload 1,2 = 36.75pF | |
| X | X | X | 1 | 1 | 1 | 0 | 0 | Cload 1,2 = 38pF | |
| X | X | X | 1 | 1 | 1 | 0 | 1 | Cload 1,2 = 39.25pF | |
| X | X | X | 1 | 1 | 1 | 1 | 0 | Cload 1,2 = 40.5pF | |
| X | X | X | 1 | 1 | 1 | 1 | 1 | Cload 1,2 = 41.75pF | |
| - | - | - | OSC4 | OSC3 | OSC2 | OSC1 | OSC0 | Bit name | Subaddress = 0AH |

PORT EXTENSION CONTROL

| MSB | | | | | | | | LSB | FUNCTION |
|-----|----|-------|-------|-------|-------|-------|-------|----------------------------------|------------------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| | | | | | | | 0 | CMOS push-pull DOUT1 low | |
| | | | | | | | 1 | CMOS push-pull DOUT1 high | |
| | | | | | | | 0 | NPN opencollector DOUT2 inactive | |
| | | | | | | | 1 | NPN opencollector DOUT2 active | |
| | | | | | | | 0 | NPN opencollector DOUT6 inactive | |
| | | | | | | | 1 | NPN opencollector DOUT6 active | |
| | | | | | | | 0 | NPN opencollector DOUT5 inactive | |
| | | | | | | | 1 | NPN opencollector DOUT5 active | |
| | | | | | | | 0 | NPN opencollector DOUT4 inactive | |
| | | | | | | | 1 | NPN opencollector DOUT4 active | |
| | | | | | | | 0 | NPN opencollector DOUT3 inactive | |
| | | | | | | | 1 | NPN opencollector DOUT3 active | |
| 0 | 0 | | | | | | | always "0" in application mode | |
| - | - | DOUT3 | DOUT4 | DOUT5 | DOUT6 | DOUT2 | DOUT1 | Bit name | Subaddress = 0BH |

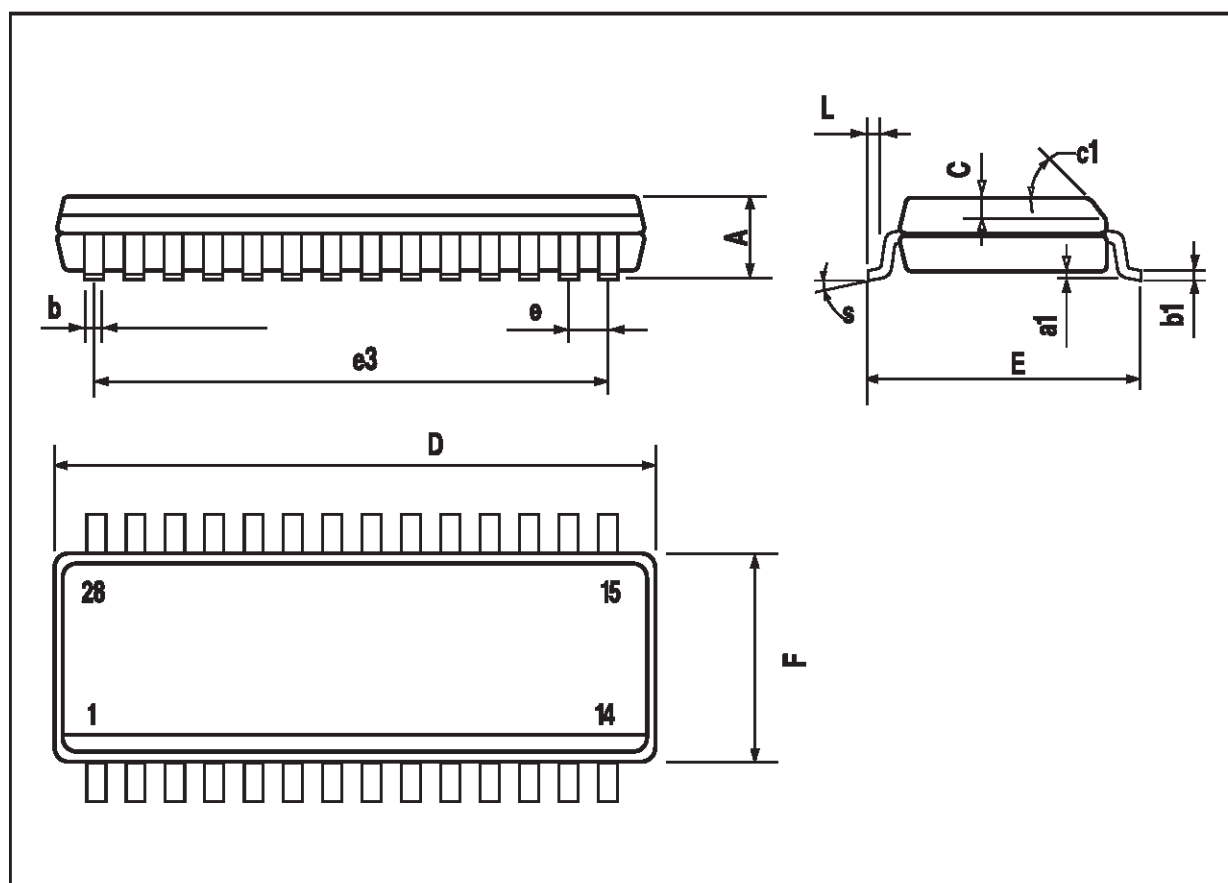
TSSOP28 PACKAGE MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|---------------------|------|------|--------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.20 | | | 0.048 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.008 |
| D | 9.60 | 9.70 | 9.80 | 0.378 | 0.382 | 0.386 |
| E | | 6.40 | | | 0.252 | |
| e | | 0.65 | | | 0.026 | |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| S | 0° (min.) 8° (max.) | | | | | |



SO28 PACKAGE MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|------------|-------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.3 | 0.004 | | 0.012 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.013 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 17.7 | | 18.1 | 0.697 | | 0.713 |
| E | 10 | | 10.65 | 0.394 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 16.51 | | | 0.65 | |
| F | 7.4 | | 7.6 | 0.291 | | 0.299 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| S | 8° (max.) | | | | | |



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