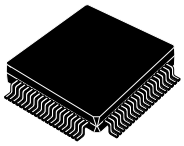
TDA7550R

DIGITAL SIGNAL PROCESSING IC FOR SPEECH AND AUDIO APPLICATIONS

- 24-BIT, FIXED POINT, 45 MIPS DSP CORE
- LARGE ON-BOARD PROGRAM RAM AND DATA RAM (16Kw-24 BIT DATA RAM AND 16Kw-24 BIT PROGRAM RAM)
- INTEGRATED STEREO, 16-BIT SIGMA-DELTA A/D AND D/A CONVERTERS
- PROGRAMMABLE CODEC SAMPLE RATE FROM 4 TO 48 kHz
- ON-BOARD PLL FOR CORE CLOCK AND CONVERTERS
- MANAGEMENT OF EXTERNAL FLASH / SRAM / DRAM MEMORY BANK
- I^2C OR SPI SERIAL INTERFACE FOR EXTERNAL CONTROL
- 80-PIN TQFP, 0.65 mm PITCH
- AUTOMOTIVE GRADE (FROM -40° C to +85°C)



TQFP80

ORDERING NUMBER: TDA7550R

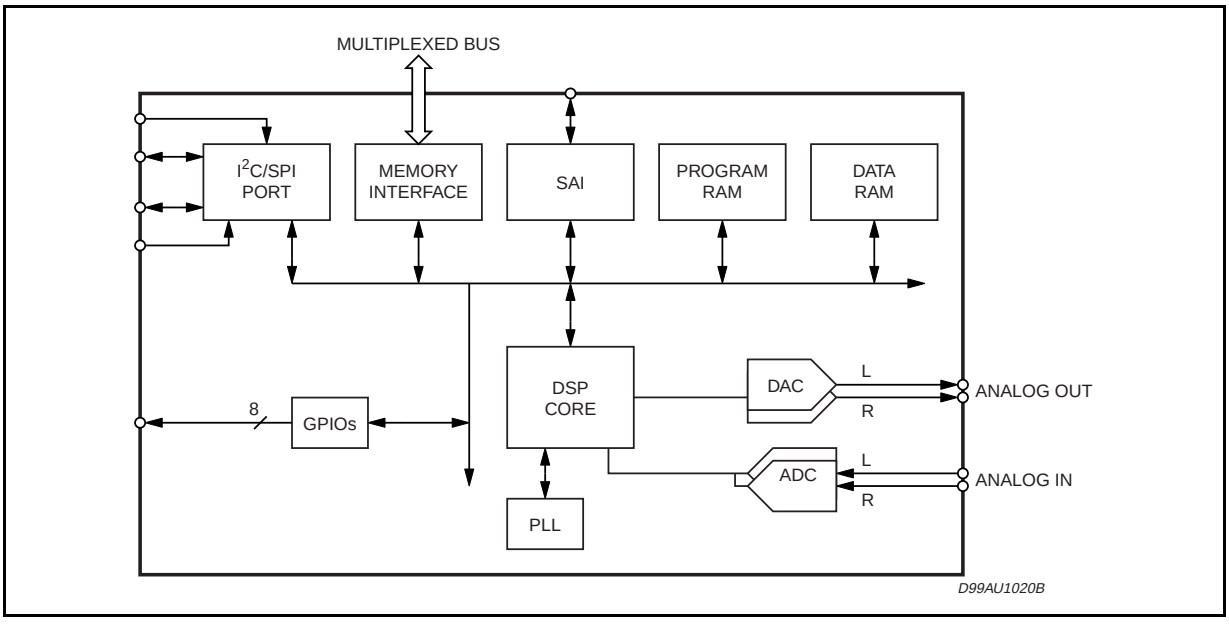
DESCRIPTION

The TDA7550R is a high performances, fully programmable 24-bit, 45 MIPS Digital Signal Processor (DSP), designed to support several speech and audio applications, as Automatic Speech Recognition, Speech Synthesis, Speaker Verification, Echo and Noise Cancellation. Software for these applications is licenced by Lernout & Hauspie and BIT Innovation Technologies.
It offers an effective solution for this kind of applications because of the A/D and D/A converters and the big amount of memory integrated on chip.

APPLICATIONS

Real time digital speech and audio processing: speech recognition, speech synthesis, speech compression, echo canceling, noise canceling, speaker verification.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

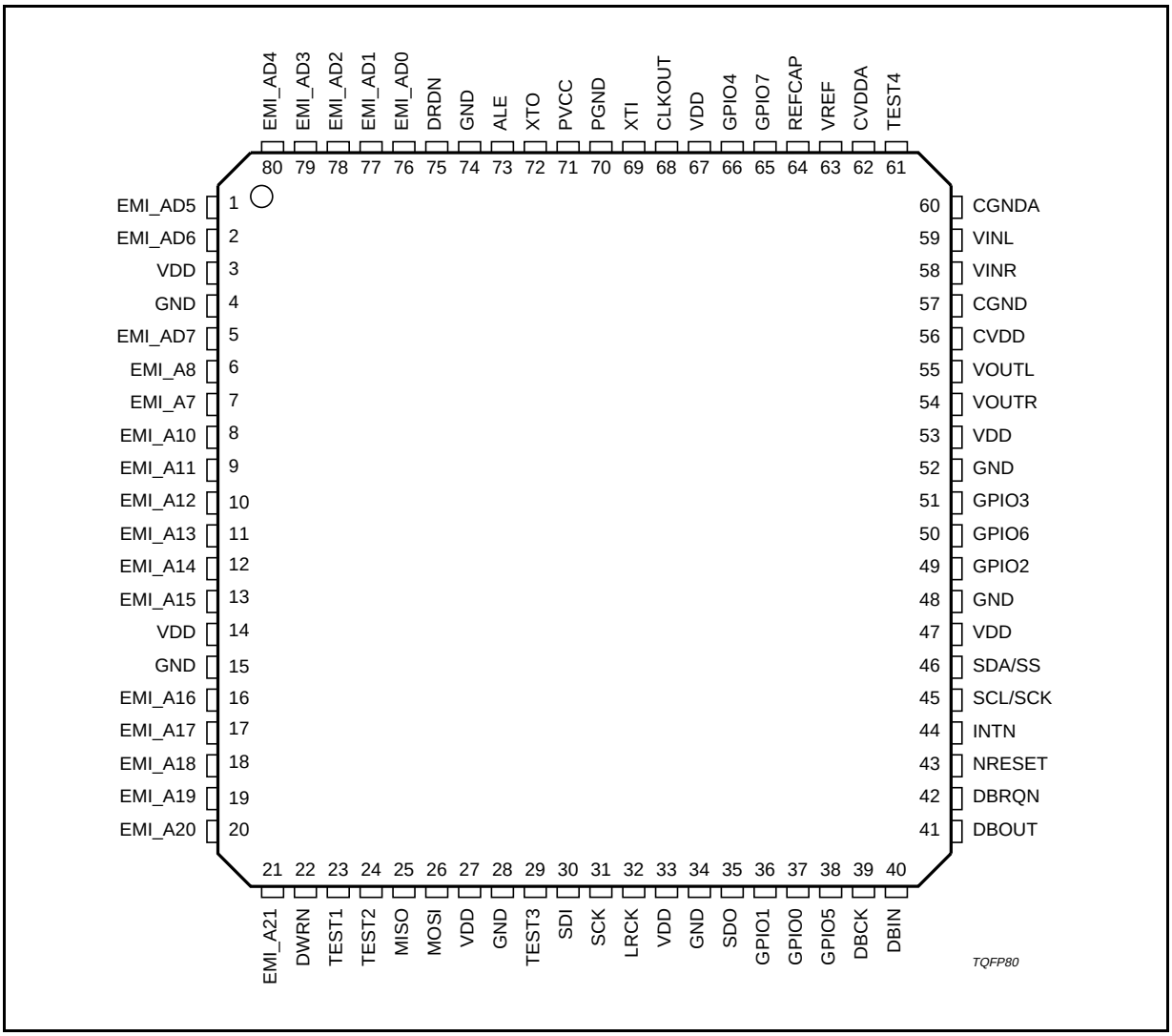
Symbol	Parameter	Value	Unit
Vdd	3.3V Power Supply Voltage	-0.5 to 4	V
	Input or Output Voltage	-0.5 to (Vdd +0.5V)	V
	Input or Output Voltage (Note 1)	-0.5 to 5.5	V

Note 1: For 5V tolerant inputs and 5V tolerant output buffers in tri-state mode.

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction pins	Max.	55	°C/W

PIN CONNECTION



PIN FUNCTIONS

N.	Name	Type	Description
1	EMI_AD5	I/O	EMI Multiplexed Address/Data Line 5. these pin acts as the EMI multiplexed address and data line 5. In DRAM mode acts as Address 1.
2	EMI_AD6	I/O	EMI Multiplexed Address/Data Line 6. these pin acts as the EMI multiplexed address and data line 6. In DRAM mode acts as Address 2.
3	VDD	I	Digital power supply
4	GND	I	Ground
5	EMI_AD7	I/O	EMI Multiplexed Address/Data Line 7. these pin acts as the EMI multiplexed address and data line 7. In DRAM mode acts as Address 3.
6	EMI_A8	O	EMI Address Line 8. these pin acts as the EMI address line 8. The interface is designed to address up to 4 Mbytes of External Flash, EPROM or SRAM. In DRAM mode acts as Address 4.
7	EMI_A9	O	EMI Address Line 9. these pin acts as the EMI address line 9. In DRAM mode acts as Address 5.
8	EMI_A10	O	EMI Address Line 10. these pin acts as the EMI address line 10. In DRAM mode acts as Address 6.
9	EMI_A11	O	EMI Address Line 11. these pin acts as the EMI address line 11. In DRAM mode acts as Address 7.
10	EMI_A12	O	EMI Address Line 12. these pin acts as the EMI address line 12. In DRAM mode acts as Address 8.
11	EMI_A13	O	EMI Address Line 13. these pin acts as the EMI address line 13. In DRAM mode acts as Address 9.
12	EMI_A14	O	EMI Address Line 14. these pin acts as the EMI address line 14. In DRAM mode acts as Address 10.
13	EMI_A15	O	EMI Address Line 15. these pin acts as the EMI address line 15. In DRAM mode acts as Address 11.
14	VDD	I	Digital power supply
15	GND	I	Ground
16	EMI_A16	O	EMI Address Line 16. these pin acts as the EMI address line 16. In DRAM mode acts as Address 12.
17	EMI_A17	O	EMI Address Line 17. these pin acts as the EMI address line 17.
18	EMI_A18	O	EMI Address Line 18. these pin acts as the EMI address line 18.
19	EMI_A19	O	EMI Address Line 19. these pin acts as the EMI address line 19.
20	EMI_A20	O	EMI Address Line 20. these pin acts as the EMI address line 20.
21	EMI_A21	O	EMI Address Line 21. these pin acts as the EMI address line 21. In DRAM mode acts as Row address Strobe.
22	DWRN	O	EMI Write Enable. This pin serves as the write enable for the EMI
23	TEST1	I	Test 1. Used for test: set to LOW for normal operation
24	TEST2	I	Test 2. Used for test: set to HIGH for normal operation
25	MISO	I/O	SPI Master Input Slave Output Serial Data. Serial Data Input for SPI type serial Port when in SPI master Mode and Serial Data Output when in SPI Slave Mode
26	MOSI	I/O	SPI Master Output Slave Input Serial Data. Serial Data Output for SPI type serial Port when in SPI master Mode and Serial Data Input when in SPI Slave Mode
27	VDD	I	Digital Power Supply
28	GND	I	Ground
29	TEST3	I	Test 3. Used for test: set to LOW for normal operation
30	SDI	I	SAI Data Input
31	SCK	I/O	SAI Bit Clock
32	LRCK	I/O	SAI Left/Right Clock

PIN FUNCTIONS (continued)

N.	Name	Type	Description
33	VDD	I	Digital power supply
34	GND	I	Ground
35	SDO	O	SAI Data Output
36	GPIO1	I/O	General Purpose I/O
37	GPIO0	I/O	General Purpose I/O
38	GPIO5	I/O	General Purpose I/O
39	DBCK	I/O	Debug port Bit Clock/Chip Status 1. The serial clock for the Debug Port is provided. May also be used as GPIO9.
40	DBIN	I/O	Debug port Serial Input/Chip Status 0. The serial data input for the Debug Port is provided. May also be used as GPIO11.
41	DBOUT	I/O	Debug Port Serial Output. This pin is the serial Data output for the Debug port. May also be used as GPIO10.
42	DBRQN	I	Debug Port Request Input. This pin is used to request Debug Mode operation to Euterpe
43	NRESET	I	System Reset. A low level applied to RESET input initializes the IC.
44	INTN	I	External interrupt line. When this line is asserted low the DSP may be interrupted.
45	SCL/SCK	I/O	I^2C Serial Clock Line. Clock line for I^2C bus. Schmitt trigger input.
		I/O	SPI Bit Clock. If SPI interface is enabled, it behaves as SPI bit clock.
46	SDA/SS	I/O	I^2C Serial Data Line. Data line for I^2C bus. Schmitt trigger input.
		I	SPI Slave Select. If SPI interface is enabled, it behaves as Slave select line for SPI bus.
47	VDD	I	Digital Power Supply
48	GND	I	Ground
49	GPIO2	I/O	General Purpose I/O
50	GPIO6	I/O	General Purpose I/O
51	GPIO3	I/O	General Purpose I/O
52	GND	I	Ground
53	VDD	I	Digital Power Supply
54	VOUTR	O	Single-ended right channel analogue output from DAC
55	VOUTL	O	Single-ended left channel analogue output from DAC
56	CVDD	I	Digital Power supply for the internal CODEC cell
57	CGND	I	Ground for the internal CODEC cell
58	VINR	I	Single-ended right channel analogue input to ADC
59	VINL	I	Single-ended left channel analogue input to ADC
60	CGNDA	I	Ground for the internal CODEC cell
61	TEST4	O	Connect a 22K pull-down resistor
62	CVDDA	I	Power Supply for the internal CODEC cell
63	VREF	O	Voltage Reference from the CODEC cell
64	REFCAP	O	Voltage Reference Capacitor Bypass
65	GPIO7	I/O	General Purpose I/O
66	GPIO4	I/O	General Purpose I/O
67	VDD	I	Digital power supply
68	CLKOUT	O	Clock Output. Output Clock divided down from PLL
69	XTI	I	Crystal Oscillator Input. Crystal Oscillator Input drive

PIN FUNCTIONS (continued)

N.	Name	Type	Description
70	PGND	I	PLL Ground Input. Ground connection for Oscillator circuit
71	PVCC	I	PLL Power Supply Positive. Supply for PLL Clock Oscillator
72	XTO	O	Crystal Oscillator Output. Crystal Oscillator Output drive
73	ALE	O	EMI Address Latch Enable. This pin acts as the EMI Address Latch Enable for the External Memory Interface. In DRAM mode acts as Column Address Strobe.
74	GND	I	Ground
75	DRDN	O	EMI Read Enable. This pin serves as the read enable for the EMI
76	EMI_AD0	I/O	EMI Multiplexed Address/Data Line 0. these pin acts as the EMI multiplexed address and data line 0 In DRAM mode acts as Data 0.
77	EMI_AD1	I/O	EMI Multiplexed Address/Data Line 1. these pin acts as the EMI multiplexed address and data line 1 In DRAM mode acts as Data 1.
78	EMI_AD2	I/O	EMI Multiplexed Address/Data Line 2. these pin acts as the EMI multiplexed address and data line 2 In DRAM mode acts as Data 2.
79	EMI_AD3	I/O	EMI Multiplexed Address/Data Line 3. these pin acts as the EMI multiplexed address and data line 3. In DRAM mode acts as Data 3.
80	EMI_AD4	I/O	EMI Multiplexed Address/Data Line 4. these pin acts as the EMI multiplexed address and data line 4. In DRAM mode acts as Address 0.

All digital pins are TTL Schmitt Trigger, 5V tolerant.

POWER DISSIPATION

Power consumption depends on application running and DSP clock frequency.

Medium consumption running a typical application like Echo and Noise cancellation:

DSP clock freq. = 43MHz

V = 3.3

Idd = 145mA

Ptot = 478mW

Max consumption with high stress test program:

DSP clock freq. = 43MHz

V = 3.3

Idd = 230mA

Ptot = 759mW

KEY PARAMETERS

Table 1.

Symbol	Parameter	Min.	Typ.	Max.	Unit
GENERAL					
f_{osc}	Crystal frequency			40	MHz
V_{dd}	Operating voltage	3.15	3.3	3.6	V
I_{DD}	Supply current		140	230	mA
T_{amb}	Operating temperature	-40		85	°C
DSP CORE					
f_{dsp}	DSP clock frequency		45	48.2	MHz
	Data bus width		24		bit
	Accumulator width		56		bit
	Multiplication unit		24x24		bit
CODEC					
SNR	Signal to noise ratio ADC		-70		dBr A weighted
SNR	Signal to noise ratio DAC		-71		dBr A weighted

ELECTRICAL CHARACTERISTICS FOR I/O PINS:

Table 2. Recommended DC Operating Conditions

Symbol	Parameter	Value	Unit
Vdd	Power Supply Voltage	3.15 to 3.6 (*)	V
Tj	Operating Junction Temperature	-40 to +125	°C

(*) All the specifications are valid only within these recommended operating conditions.

Table 3. General Interface Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Iil	Low level Input Current Without pullup device [1]	Vi = 0V			1	µA
Iih	High Level Input Current Without pulldown device [1]	Vi = Vdd			1	µA
Ioz	Tri-state Output leakage Without pull up/down device [1]	Vo = 0V or Vdd			1	µA
IozFT	Five Volt tolerant Tri-state Output leakage Without pull up/down device [1]	Vo = 0V or Vdd			1	µA
		Vo = 5.5V		1	3	µA
I latchup	I/O Latch-up current	V < 0V, V < Vdd	200			mA
Vesd	Electrostatic Protection [2]	leakage < 1µA	2000			V

Note 1. The leakage currents are generally are generally very small, <1nA. The value given here, 1mA, is a maximum that can occur after an Electrostatic Stress on the pin.

Note 2. Human Body Model.

Table 4. Low Voltage TTL Interface DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vil	Low Level Input Voltage [1]				0.8	V
Vih	High Level Input Voltage [1]		2			V
Vilhyst	Low level threshold input falling[1]		0.9		1.35	V
Vihhyst	High level threshold input falling[1]		1.3		1.9	V
Vhyst	Schmitt trigger hysteresis [1]		0.4		0.7	V
Vol	Low level output Voltage [1],[2],[3]	Iol = XmA			0.4	V
Voh	High level output Voltage [1],[2],[3]	Iol = XmA	2.4			V

Note 1. TTL specifications only apply to the supply voltage range Vdd = 3.15V to 3.6V.

Note 2. Takes into account 200mV voltagedrop in both supply lines.

Note 3. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

24 BIT DSP CORE

The DSP Core is a general purpose 24-bit DSP. The main feature of the DSP Core are listed below:

- 45MHz Operating Frequency (45 MIPS)
- Single cycle multiply and accumulate
- 2x56-bit Accumulators
- Double precision multiply
- Convergent rounding
- Scaling and saturation arithmetic
- 48-bit or 2x24-bit parallel moves
- 21 programmable interrupt sources
- Fast or long interrupts possible
- Programmable interrupt priorities and masking
- 8 each Address Registers, Address Offset Registers and Address Modulo Registers
- Linear, Reverse Carry, Multiple Buffer Modulo, Multiple Wrap-around Modulo address arithmetic
- Post-increment or decrement by 1 or by offset, Index by offset, predecrement address
- Repeat instruction and zero overhead DO loops
- Hardware stackcapable of nesting 7 DO loops or 15 interrupts/subroutines
- Bit manipulation instructions possible on all registers and memory locations. Also Jump on bit test.
- Data Arithmetic Logic Unit (DALU)
- Address Generation Unit (AGU)
- Program Control Unit (PCU)
- Three Data Buses
- Three Address Buses
- Internal Data Bus Switch
- bit Manipulation Unit
- Debug Logic

Memories

16384x24-bit Program RAM used for storing the program code.

16384x24-bit Total Data RAM used for storing Data.

DSP peripherals

- **Serial Audio Interface (SAI)**
  The SAI is used to deliver digital audio to the DSP from an external source and to deliver digital audio from the DSP to an external DAC. It allows using an external CODEC. The main features of this block are listed below:
  – One Data Transmission Line
  – One Data Reception Line
  – Master and Slave Operating Modes
  – Reference clock for transmission supplied
  – Transmit and Receive Interrupt Logic modified to trigger on Left/Right data pairs
  – Receive and Transmit Data Registers have two locations to hold left and right data

- **I^2C interface/SPI**
  The inter integrated-circuit bus is a simple bi-directional two-wire bus used for efficient inter IC control. All I^2C bus compatible devices incorporate an on-chip interface which allows them communicate directly with each via the I^2C bus. Every component hoocked up to the I^2C bus has it's own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and/or transmitter depending on it's functionality.
  The Serial Peripheral Interface (SPI) can be enabled instead of the I^2C interface. During an SPI transfer, data is trasmitted and received simulaneously. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device. When an SPI transfer occurs an 8-bit word is shifted out one data pin while another 8-bit character is simultaneously shifted in a second data pin. The central element in the SPI system is the shift register and the read data buffer. The system is single buffered in the trasmit direction and double buffered in the receive direction.

EMI

- The External Memory Interface is viewed as a memory mapped peripheral. Data transfers are performed by moving data into/from data registers and the control is exercised by polling status flags in the control/status register or by servicing interrupts. An external memory write is executed by writing data into the Data Write register. An external memory read operation is executed by either writing to the Offset register or reading the Data read register, depending on the configuration.
  The main features of the EMI are listed below:
  – Data bus width fixed at 4 bits for DRAM and 8 bits for SRAM
  – 22 bit address bus multiplexed with an 8 bit data bus
  – Three choices of data word lenghths, 8, 16 or 24 bits
  – SRAM relative addressing modes
  – 2^{22}=4MBytes addressable SRAM
  – Four SRAM Timing choices

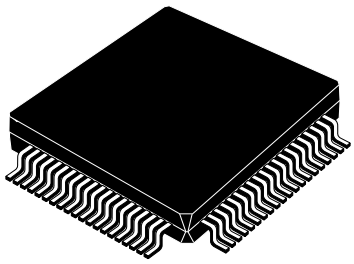
– Two Read Offset Register

- **PLL**
  The Euterpe clock system generates the following clocks:
  – DCLK the DSP core clock
  – MCLK CODEC master clock
  – LRCLK left/right clock for the SAI and the CODEC
  – SCLK shift serial clock for the SAI and the CODEC
  The output of the PLL operates from 70 to 140 MHz. The DSP core can operate with a clock up to 48.2 MHz.
  The audio clock are derived from the VCO output.

- **CODEC CELL**
  The main features of the CODEC cell are listed below:
  – one 16-bit Delta Sigma Stereo ADC
  – 80 dB Dynamic Range
  – Oversampling Ratio: 128
  – one 16-bit Delta Sigma Stereo DAC
  – 80 dB Dynamic Range
  – Interpolating Ratio: 128
  – Sampling rates of 4kHz to 48kHz
  – Signal Noise Ratio: 80 dB Typ.
  The analog interface is in the form of differential signals for each channel. The interface on the digital side has the form of an SAI interface and can interface directly to an SAI channel and then to the DSP core.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.35			0.295	
e		0.65			0.0256	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.35			0.486	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	3.5°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP80 (14x14x1.40mm)