DATA SHEET

TDA8051
QPSK Receiver

Preliminary specification
File under Integrated Circuits, IC02

1998 Jan 08

Philips
Semiconductors

PHILIPS

QPSK Receiver TDA8051

FEATURES

- High operating input sensitivity
- gain controlled amplifier
- PLL controlled carrier frequency
- Low crosstalk between I and Q channel outputs
- 3 wire transmission bus
- 5 V supply voltage

APPLICATIONS

- BPSK/QPSK demodulation

GENERAL DESCRIPTION

This circuit is a monolithic bipolar IC customed for QPSK demodulation. It includes a Low Noise RF Amplifier, a Gain Controlled RF Amplifier, a pair of matched Mixers, a symmetrical VCO with 0-90 degrees signal generator which frequency is controlled by an integrated PLL.

A pair of matched amplifiers (for output base-band active filtering) and output buffers complete the circuit.

The gain control is produced by an output level detection compared with an external pre-fixed reference.

The PLL consists of a divide by four preamplifier, a 12-bit programmable main divider, a crystal oscillator and its 8-bit programmable reference divider, a phase/frequency detector combined with a charge pump which drives the tuning amplifier, including 30 V output.

QUICK REFERENCE DATA

All AC Units are rms values, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP.	MAX.	UNIT
V_{cc}	functional supply voltage range	4.75	5.00	5.25	V
T_{amb}	operating ambient temperature	0	–	+70	°C
$f_{I(LNA)}$	input carrier frequency at LNA input	44	–	130	MHz
$V_{I(LNA)}$	input level at LNA input	–30	–	0	dBmV
$\Delta\Phi_{I-Q}$	phase error between I and Q channels	–	±3	–	deg.
ΔG_{I-Q}	gain error between I and Q channels	–	±1	–	dB
$\alpha_{CT(I-Q)}$	crosstalk between I and Q channels	–	–30	–	dBc
IM3	3rd oder intermodulation distorsion in I and Q channels (0dBmV at LNA_IN)	–	–	–45	dBc
V_o	voltage output on pin I_OUT and Q_OUT	–	48	–	dBmV
f_{step}	frequency step at output	50	–	250	kHz
f_{xtal}	crystal frequency	1	–	4	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8051T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

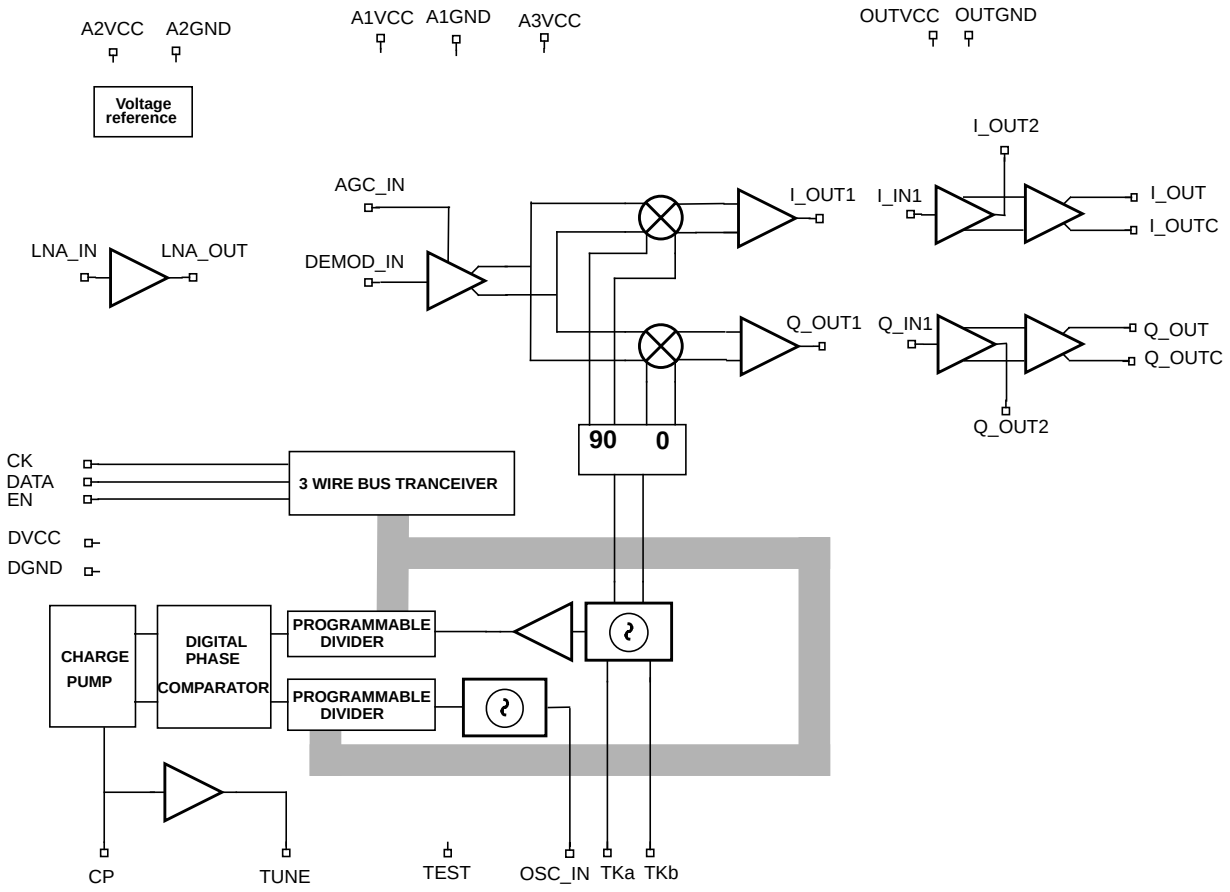


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I_OUT	1	I data bufferised balanced output
I_OUTC	2	I data bufferised balanced output
I_OUT2	3	I data filtered output
I_IN1	4	input to active filter amplifier for I data
I_OUT1	5	I data raw output
A1VCC	6	analog DC supply
DEMOD_IN	7	demodulator RF input
LNA_OUT	8	low noise amplifier RF output
LNA_IN	9	low noise amplifier RF input
A1GND	10	analog DC ground
AGC_IN	11	AGC control voltage input
OSC_IN	12	oscillator input
DVCC	13	digital DC supply
CK	14	3 wire bus serial control Clock
DATA	15	3 wire bus serial control Data
EN	16	3 wire bus serial control Enable (active low)
TEST	17	test pin: do not connect
CP	18	charge pump output for PLL loop filter
TUNE	19	tuning voltage output
DGND	20	digital DC ground
TKb	21	VCO tank circuit input
TKa	22	VCO tank circuit input
A2VCC	23	analog DC supply
A2GND	24	analog DC ground
A3VCC	25	analog DC supply
OUTGND	26	output amplifiers DC ground
OUTVCC	27	output amplifiers DC supply
Q_OUT1	28	Q data raw output
Q_IN1	29	input to active filter amplifier for Q data
Q_OUT2	30	Q data filtered output
Q_OUTC	31	Q data bufferised balanced output
Q_OUT	32	Q data bufferised balanced output

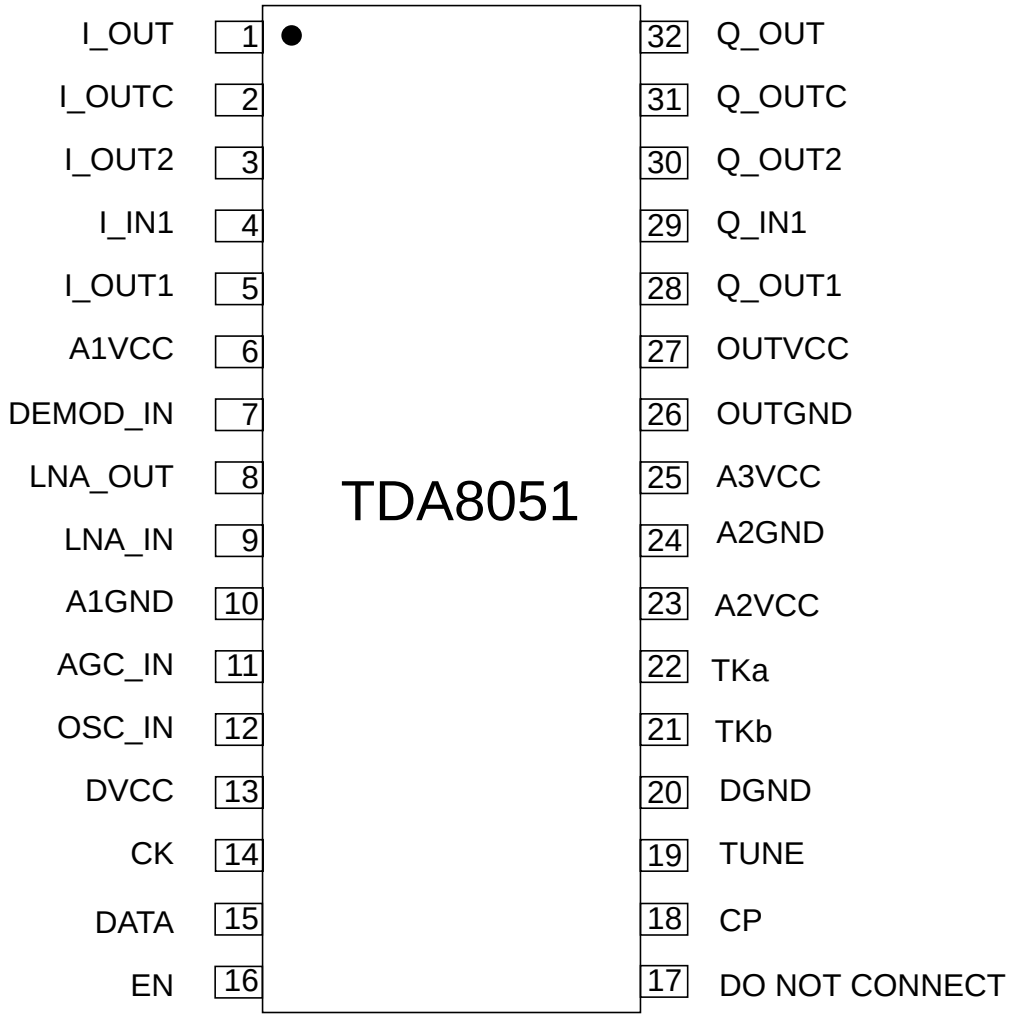


Fig.2 SO32 package, pin configuration

FUNCTIONAL DESCRIPTION

The QPSK modulated signal is applied to the input under the form of an asymmetrical RF signal within the 44 to 130 MHz band. The spectrum extension of this waveform must be limited by a band-pass filter located ahead of the IC.

The RF input is either the LNA input, if the level is -30 to +0 dBmVrms, or directly the DEMOD input if the level is -20 to +10 dBmVrms.

This amplified RF signal is then mixed with two clocks in quadrature to provide the base-band demodulated In-phase and Quad-phase signals.

As the 0-90 degrees clocks are generated by a divider by 2, the VCO has to operate at twice the RF carrier frequency: on the 88 MHz up to 260 MHz bandwidth (over an octave).

This VCO frequency is programmable thanks to the internally implemented PLL which tunes the external LC tank circuit.

The I and Q so generated are raw signals with many spikes. Each signal is then applied to a third order active low-pass filter (RC cell + Sallen-Key structure) which cut-off frequency is set by external components.

Finally, the filtered datas are amplified to provide bufferised balanced outputs.

The data sent to the PLL is loaded in bursts framed by the signal $\overline{EN}$. Programming clock edges, together with their appropriate data bits, are ignored until $\overline{EN}$ becomes active (low). The internal latches are updated with the latest programming data when $\overline{EN}$ returns inactive (high). Only the last 14 bits are retained within the programming register. No check is made on the number of clock pulses received during the time that programming is enabled. $\overline{EN}$ going high while CLOCK is still low, generates an active clock edge causing a shift of the data bits. The main divider ratio and the reference divider ratio are provided via the serial bus. (Table 1)

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{cc}	supply voltage pins		–0.3	6.0	V
V_{max}	voltage on all pins		–0.3	Vcc	V
t_{sc}	maximum short circuit duration on outputs		–	10	s
T_{stg}	IC Storage temperature		–40	+150	°C
T_j	maximum junction temperature		–	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
$V_{CC(tune)}$	tuning voltage supply		–0.3	30	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	65	K/W

CHARACTERISTICS

Measured in application circuit with the following conditions:
Vcc=5V, Tamb=25 ºC unless otherwise specified.
All AC Units are rms values, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA1}	analog supply voltage		4.75	5	5.25	V
I_{CCA1}	analog supply current		–	23	–	mA
V_{CCA2}	analog supply voltage		4.75	5	5.25	V
I_{CCA2}	analog supply current		–	18	–	mA
V_{CCA3}	analog supply voltage		4.75	5	5.25	V
I_{CCA3}	analog supply current		–	29	–	mA
$V_{CC(OUT)}$	output supply voltage		4.75	5	5.25	V
$I_{CC(OUT)}$	output supply current		–	17	–	mA
V_{CCD}	digital supply voltage		4.75	5	5.25	V
I_{CCD}	digital supply current		–	13	–	mA
$V_{CC(TUNE)}$	tuning supply voltage		–	–	30	V
Low Noise Amplifier: Rs=75 Ω / Rl= 75 Ω unless otherwise specified.						
$V_{I(DC)}$	DC input level	(Internally set)	–	0.85	–	V
V_I	input level		–30	–	0	dBmV
f_I	input carrier frequency		44	–	130	MHz
R_I	input resistance		–	75	–	Ω
C_I	input capacitance			2.5		pF
RL_I	input return loss			–15		dB
$NF_{(LNA)}$	noise figure			8		dB
$V_{leak(LO)}$	LO leakage on pin at LNA_IN	f_{N*LO} = 140 - 860 MHz pin LNA_OUT connected to DEMOD_IN			–15	dBmV
		$f_{LO/2}$ = 70 - 130 MHz pin LNA_OUT connected to DEMOD_IN		–5		dBmV
G_{LNA}	LNA gain	f = 100 MHz $V_{I(LNA)}$ = 0 dBmV	8	10	12	dB
V_o	output level		–20		+10	dBmV
ΔV_o	output flatness	in 1 MHz bandwidth $V_{I(LNA)}$ = 0 dBmV 44 MHz to 70 MHz $V_{I(LNA)}$ = 0 dBmV 70 MHz to 130 MHz $V_{I(LNA)}$ = 0 dBmV		0.25 1 1		dB dB dB
$IM3_{(LNA)}$	third order intermodulation	2 carriers at + 10 dBmV each at pin LNA_IN at 103 MHz / 105 MHz		–60		dBc
$V_{o(DC)}$	DC output level			1.3		V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_o	output resistance			75		Ω
Quadrature demodulator: Rs=75 Ω / Rl= 20 kΩ unless otherwise specified.						
$V_{I(DC)}$	DC input level	internally set		1		V
V_I	input level		–20		+10	dBmV
f_I	input carrier frequency		44		130	MHz
R_I	input resistance			75		Ω
C_I	input capacitance			2.5		pF
RL_I	input Return Loss			–10		dB
$V_{o(I,Q)}$	output level on pin I_OUT1 or Q_OUT1			22		dBmV
$BW_{o(I,Q)}$	output 3 dB bandwidth	LO = 200 MHz RF = 100 MHz to 130 MHz		20		MHz
C/N	carrier to noise ratio at 500 kHz on pin at I_OUT1 or Q_OUT1	V_I = – 20 dBmV $V_{o(I,Q)}$ = 22 dBmV		88		dBc/Hz
		V_I = 10 dBmV $V_{o(I,Q)}$ = 22 dBmV		88		dBc/Hz
$V_{leak(LO)}$	LO leakage on pin DEMOD_IN	f_{LO} = 140 - 260 MHz $f_{LO/2}$ = 70 - 130 MHz		–15		dBmV
AGC_R	AGC range	f_{LO} = 200 MHz f_{RF} = 100.25 MHz at –20 to +10 dBmV f_{BF} = 250 kHz at 22 dBmV	30			dB
AGC_S	AGC slope maximum	f_{LO} = 200 MHz f_{RF} = 100.25 MHz at –20 to +10 dBmV f_{BF} = 250 kHz at 22 dBmV		30		dB/V
V_{AGC}	gain control voltage at AGC_IN		10% AVCC		90% AVCC	V
G_{max}	Max conversion gain	f_{LO} = 260 MHz f_{RF} = 130.25 MHz at –20 dBmV V_{AGC} = 4.5 V	42			dB
G_{min}	Min conversion gain	f_{LO} = 140 MHz f_{RF} = 70.25 MHz at 10 dBmV V_{AGC} = 0.5 V			12	dB
$\Delta\Phi_{I-Q}$	phase error between I and Q channels	f_{LO} = 140 - 260 MHz f_{RF} = 70.25 - 130.25 MHz f_{BF} = 250 kHz at 22 dBmV over specified input range		± 3		deg.
ΔG_{I-Q}	gain error between I and Q channels	f_{LO} = 140 - 260 MHz f_{RF} = 70.25 - 130.25 MHz f_{BF} = 250 kHz at 22 dBmV over specified input range		±1		dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta\Phi_{I-Q}$	phase error between I and Q channels	f_{LO} = 88 - 140 MHz f_{RF} = 44.25 - 70.25 MHz f_{BF} = 250 kHz at 22 dBmV over specified input range		± 3		deg.
ΔG_{I-Q}	gain error between I and Q channels	f_{LO} = 88 - 140 MHz f_{RF} = 44.25 - 70.25 MHz f_{BF} = 250 kHz at 22 dBmV over specified input range		±1		dB
IM3	third order intermodulation in I and Q channels	Fig.3			–35	dBc
IM2	second order intermodulation in I and Q channels	Fig.3			–35	dBc
AM_REJ	AM rejection at I and Q channels	Fig.4 guaranted by design			–35	dBc
$\Delta V_{o(I,Q)}$	output flatness at I and Q outputs	in 1 MHz bandwidth f = 40 to 70 MHz f = 70 to 130 MHz		0.25 3 3		dB
$V_{o(DC)}$	DC output level			2.5		V
R_o	output resistance			400		Ω
Output Section: Rs = 400 Ω / Rl = 4 kΩ/ R on pin I_OUT2 or Q_OUT2 = 20 kΩ unless otherwise specified.						
$V_{I(DC)}$	DC input voltage			3.6		V
V_i	input level			22		dBmV
R_i	input resistance			17.5		kΩ
C_i	input capacitance			0.4		pF
G_O	gain from I-Q_IN1 to I-Q_OUT2	f_{BF} = 1 MHz at 22 dBmV		4		dB
$\Delta V_{o(I-Q\_out2)}$	output flatness on pin I_OUT2 and Q_OUT2	f_{BF} = 0 to 1.5 MHz f_{BF} = 0 to 6 MHz at 22 dBmV input		0.25 1		dB dB
$DC_{o(I-Q\_out2)}$	DC output level at filter output			2.6		V
$R_{o(\overline{IQ}\_out2)}$	output resistance	f < 20 MHz				Ω
$H2_{(I-Q\_OUT)}$	2nd harmonic	f_{BF} = 1 MHz at 48 dBmV output		–35		dBc
$H3_{(I-Q\_OUT)}$	3rd harmonic	f_{BF} = 1 MHz at 48 dBmV output		–35		dBc
$IM3_{(I-Q\_OUT)}$	third order intermodulation at I_OUT, Q_OUT	Fig.5		–45		dBc
$\alpha_{CT(I-Q)}$	crosstalk between I and Q channels	Fig.6 f = 5 MHz		–30		dBc
$N_{o(IQ\_OUT)}$	output noise poweatr at 500 kHz from carrier	Fig.7		–56		dBmV/Hz
$G_{(I-Q\_OUT)}$	gain from I-QIN1 to I-Q_OUT	f_{BF} = 1 MHz at 22 dBmV input		27		dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$DC_{o(I\text{-}Q\_out)}$	DC output level on pin I-Q_OUT output			3.1		V
$R_{o(\overline{IQ}\_out)}$	output differential resistance			460		Ω
Overall: Rs = 75 Ω / Rl = 4 kΩ unless otherwise specified.						
V_o	voltage output on pin I_OUT and Q_OUT	Fig.8		48		dBmV
LO_{lev}	LO level on pin I_OUT, Q_OUT	Fig.8		−20		dBc
S_o	spurious emission on pin I_OUT,Q_OUT	Fig.8 f = 0 to 5 MHz		−40		dBc
$\Delta G_{I\text{-}Q}$	gain error on pin I_OUT,Q_OUT	Fig.8		±1		dB
$AM\_REJ_{(I,Q)}$	Am rejection in I and Q channels	Fig.9 guaranteed by design			−35	dBc
$IM3_{(I\text{-}Q)}$	third order Intermodulation	Fig.10 guaranteed by design			−45	dBc
Voltage Controlled Oscillator:						
$f_{vco(min)}$	min. oscillation freq.	note 1		88		MHz
$f_{vco(max)}$	max. oscillation freq.	note 1		260		MHz
Φ_{osc}	oscillator phase noise	at 10 kHz at 100 kHz		−75 −95		dBc/Hz dBc/Hz
Phase looked loop						
Step	step size	at pin VCO output	100		500	KHz
RD	Fix. ref. divider ratio			2		
RDR	Ref. divider ratio		2		80	
ND	Fix main divider ratio			4		
NDR	main divider ratio		128		2600	
I_{CP}	charge pump current			300		µA
Crystal oscillator						
f_{xtal}	crystal frequency		1		4	MHz
Z_I	input impedance	f_{xtal} = 4 MHz	600	1200		Ω
$V_{I(DC)}$	DC input level			2.9		V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_I	input level			tbd		V
3 wire bus						
V_{IL}	input Low level	guaranteed by design			0.8	V
V_{IH}	input High level	guaranteed by design	2.4			V
f_{ck}	clock frequency	guaranteed by design		330		kHz
t_{su}	input data to CK set-up time	guaranteed by design		2		µs
t_h	input data to CK hold time	guaranteed by design		1		µs
t_{start}	delay to rising clock edge	guaranteed by design		3		µs
t_{end}	delay from last clock edge	guaranteed by design		3		µs

Notes

1. The frequency range of the receiver is 44 to 130 MHz. The LO operates at twice the output frequency (88 to 260 MHz). The control of the frequency made by the varicap diodes allows a variation over an octave.
2. Crystal oscillator
   the crystal oscillator uses a 4 MHz, 2 MHz or 1 MHz crystal in serie with a capacitor. The crystal is parallel resonant with load capacitance of 18 to 20 pF. The connection to V_{CC} is prefered but it might also be to GND.

NOTE TO CHARACTERISTICS

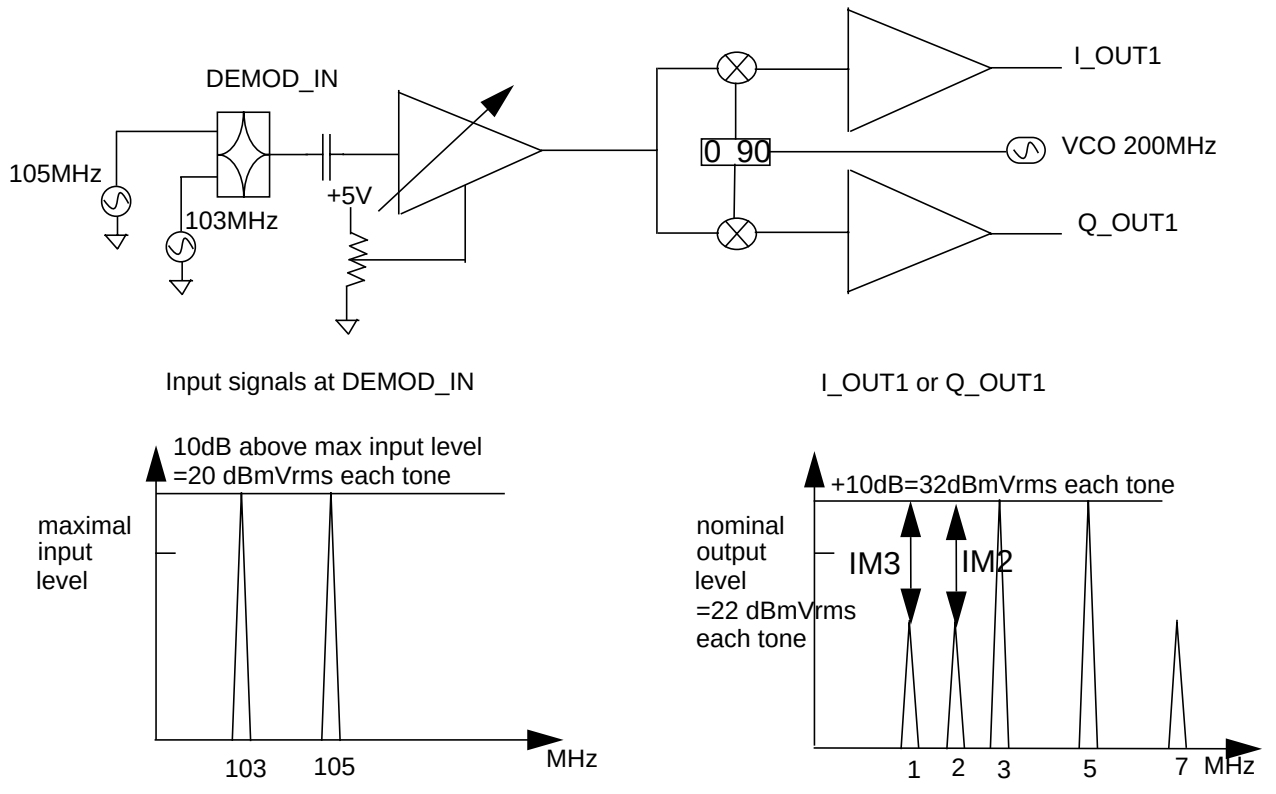


Fig.3 IM2 and IM3 measurement of the demodulator

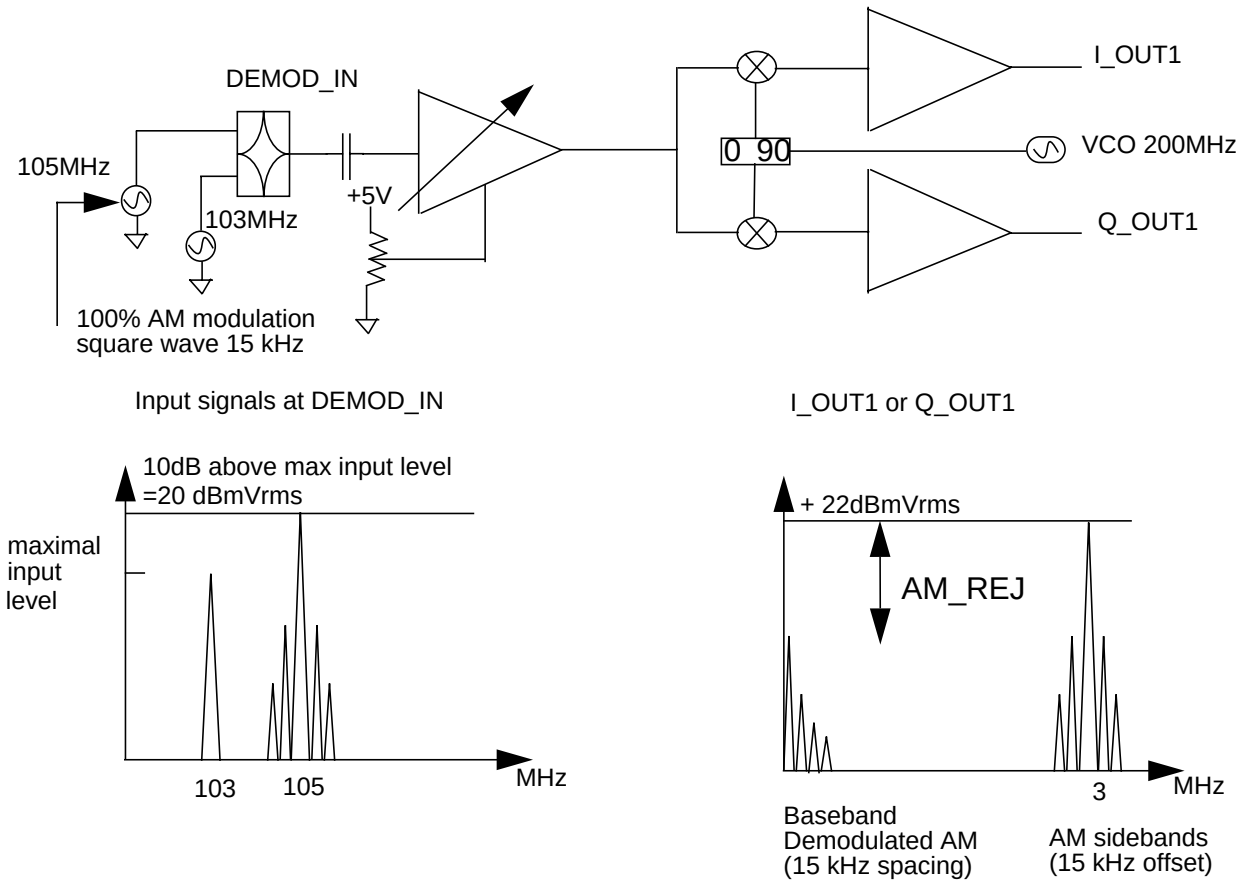


Fig.4 AM rejection test

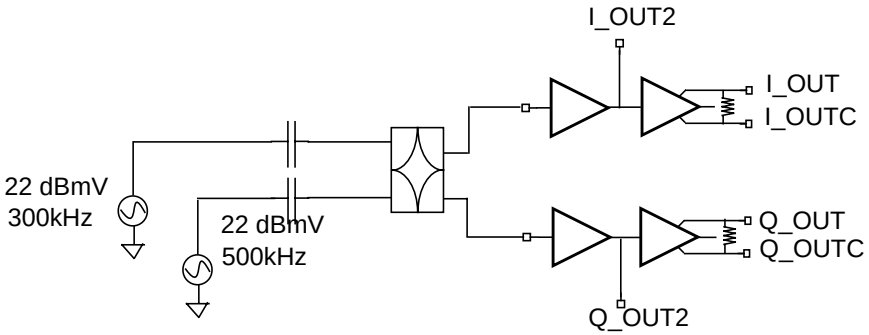
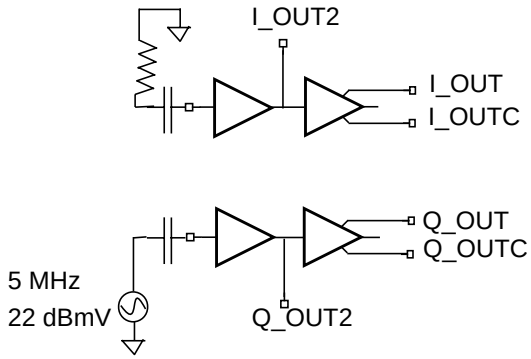


Fig.5 IM3 measurement of the output section



(1) Measure I & Q, α is the difference between the two carriers.

Fig.6 Crosstalk measurement

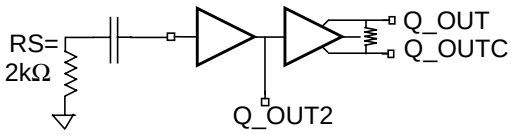


Fig.7 Noise measurement

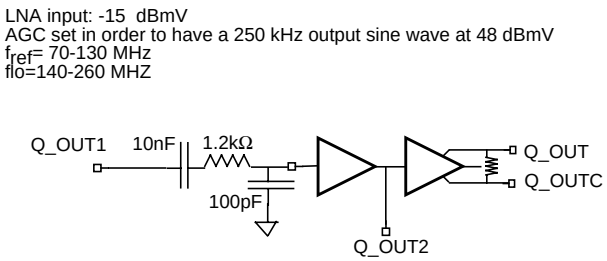


Fig.8 LO level, spurious, I/Q gain error, V_o measurements

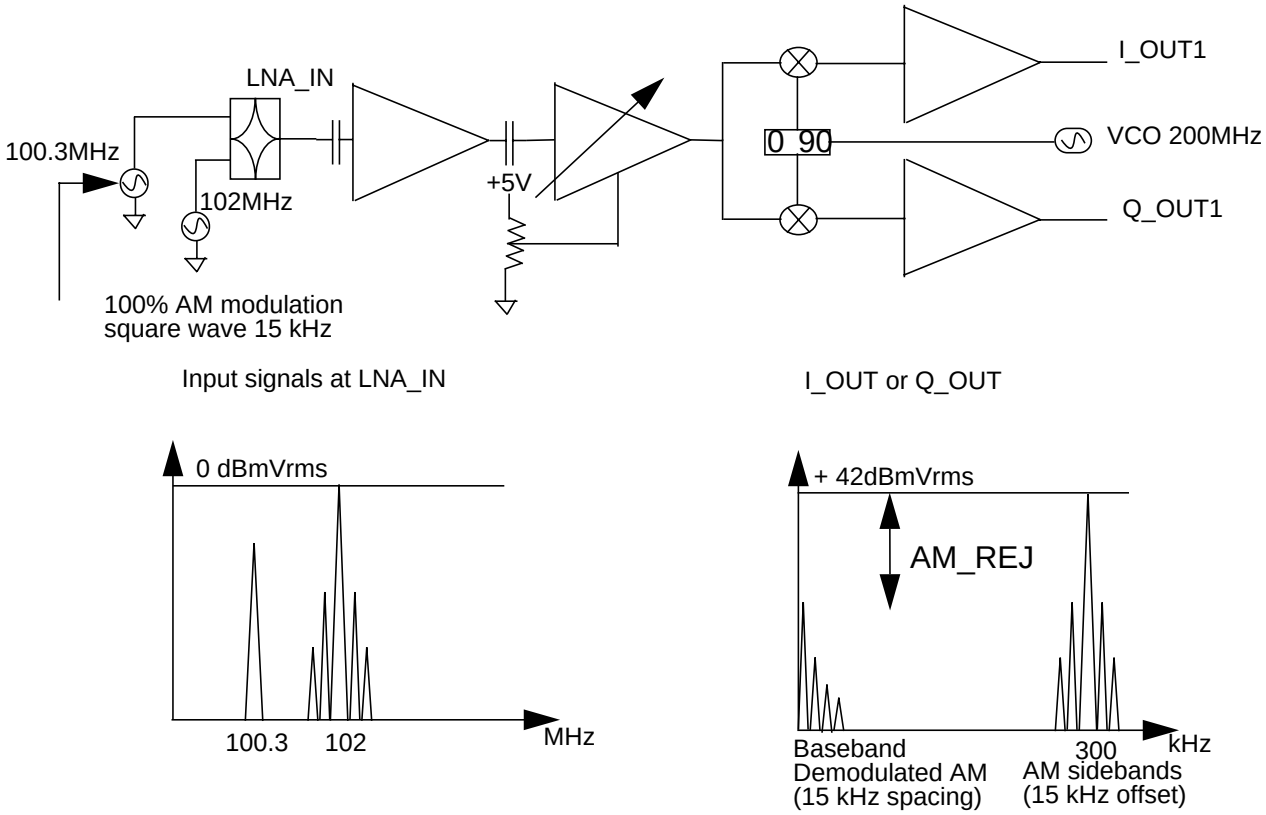


Fig.9 Overall AM Rejection measurement

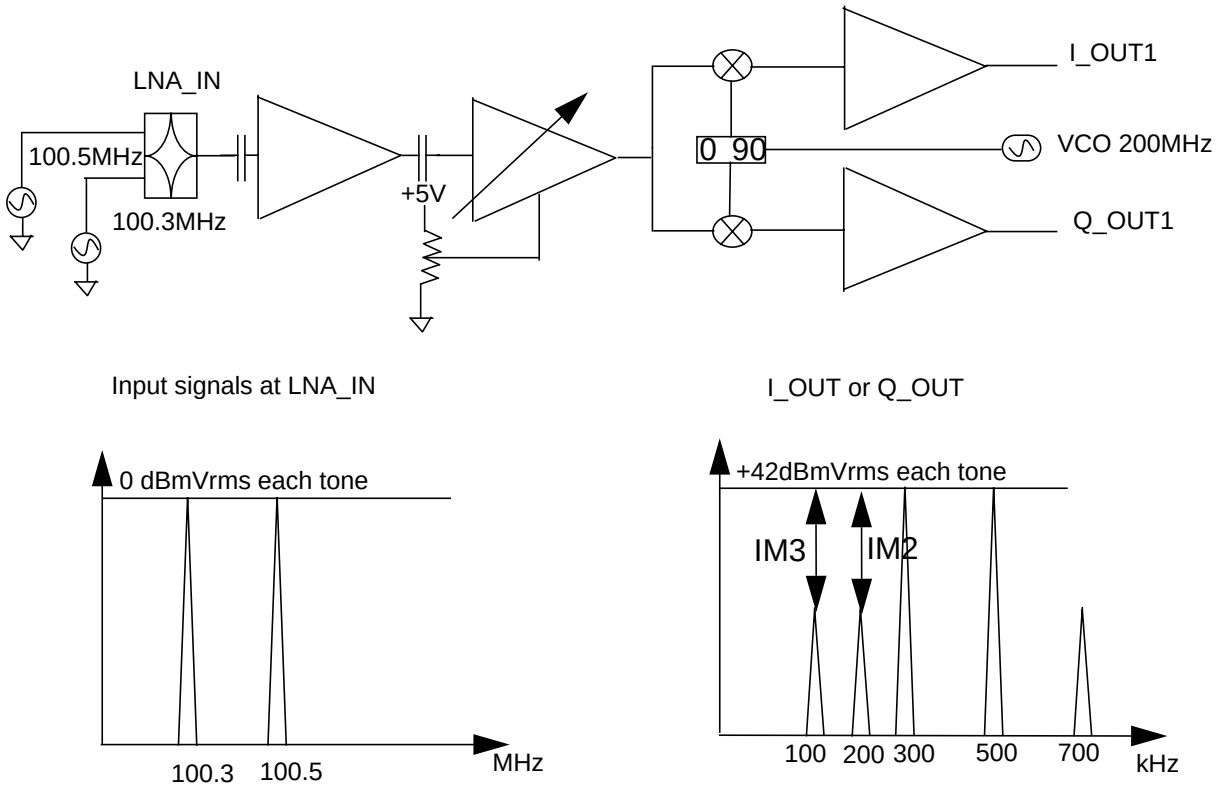


Fig.10 Overall IM3 measurement

TIMING CHARACTERISTICS

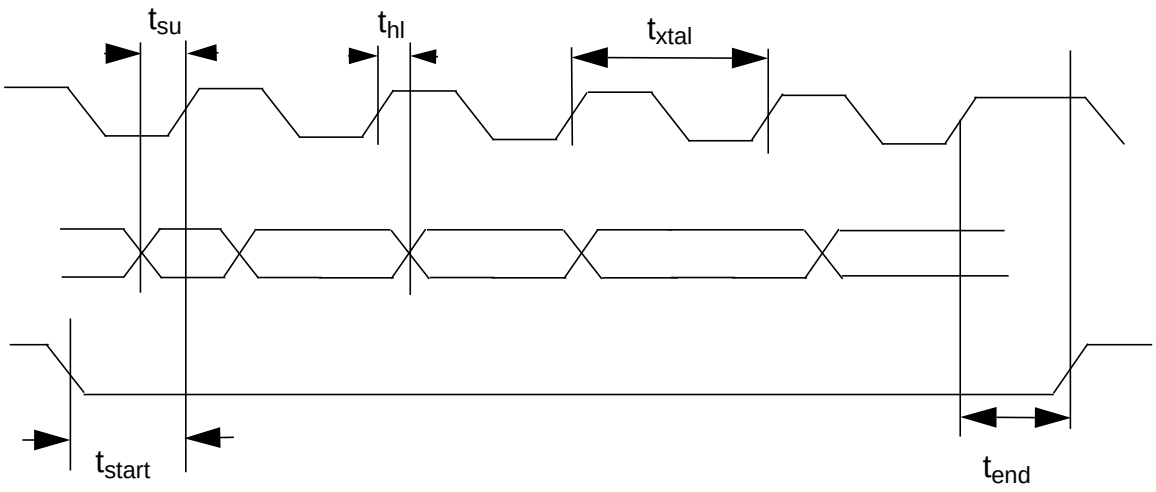


Fig.11 Logic interface signals

DATA FORMAT

Table 1

First													**Last**
DATA													
d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	ad1	ad0
REFERENCE RATIO													
x	x	x	x	r7	r6	r5	r4	r3	r2	r1	r0	0	1
PRINCIPAL RATIO													
p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0	1	1

APPLICATION INFORMATION

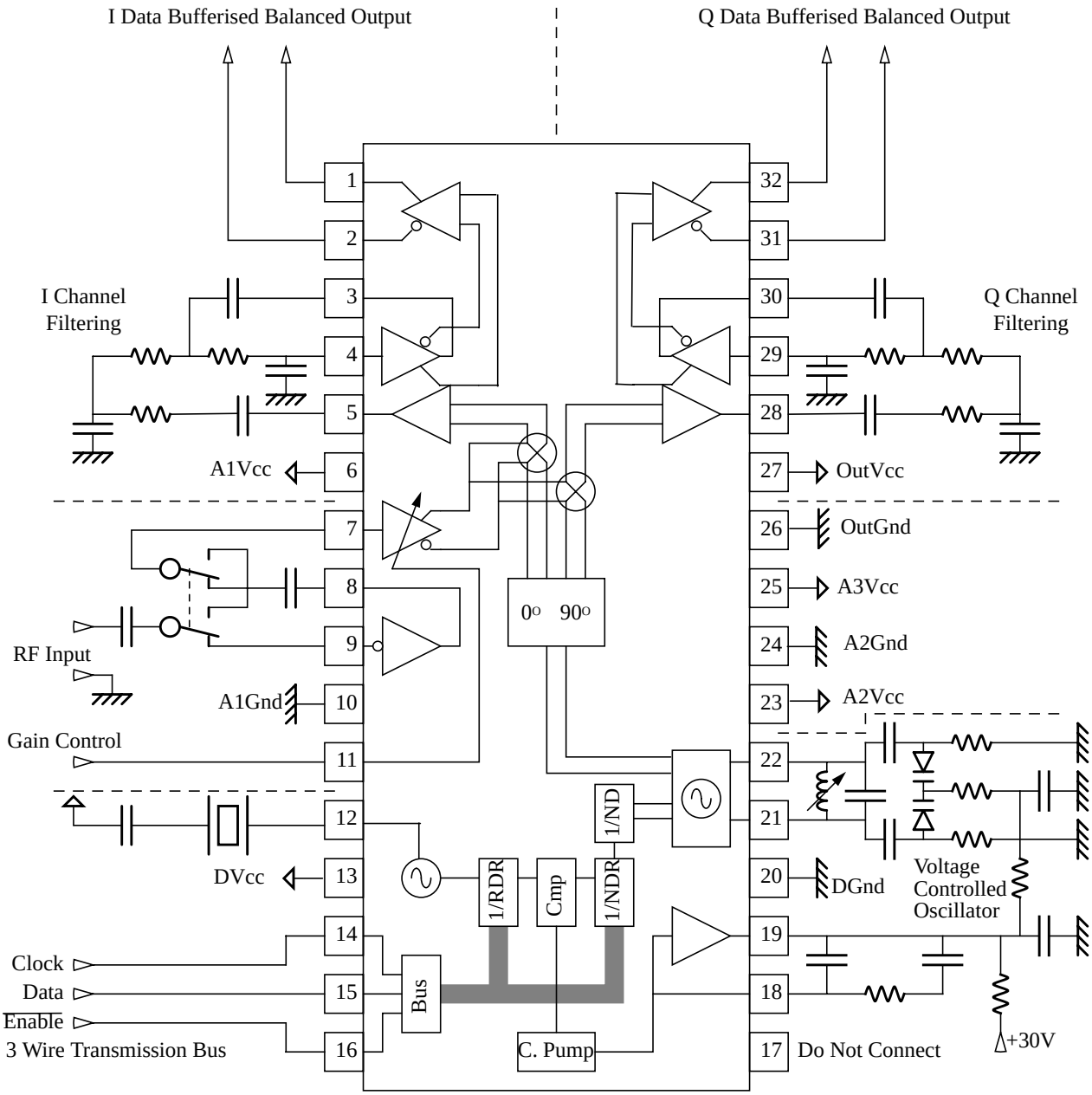
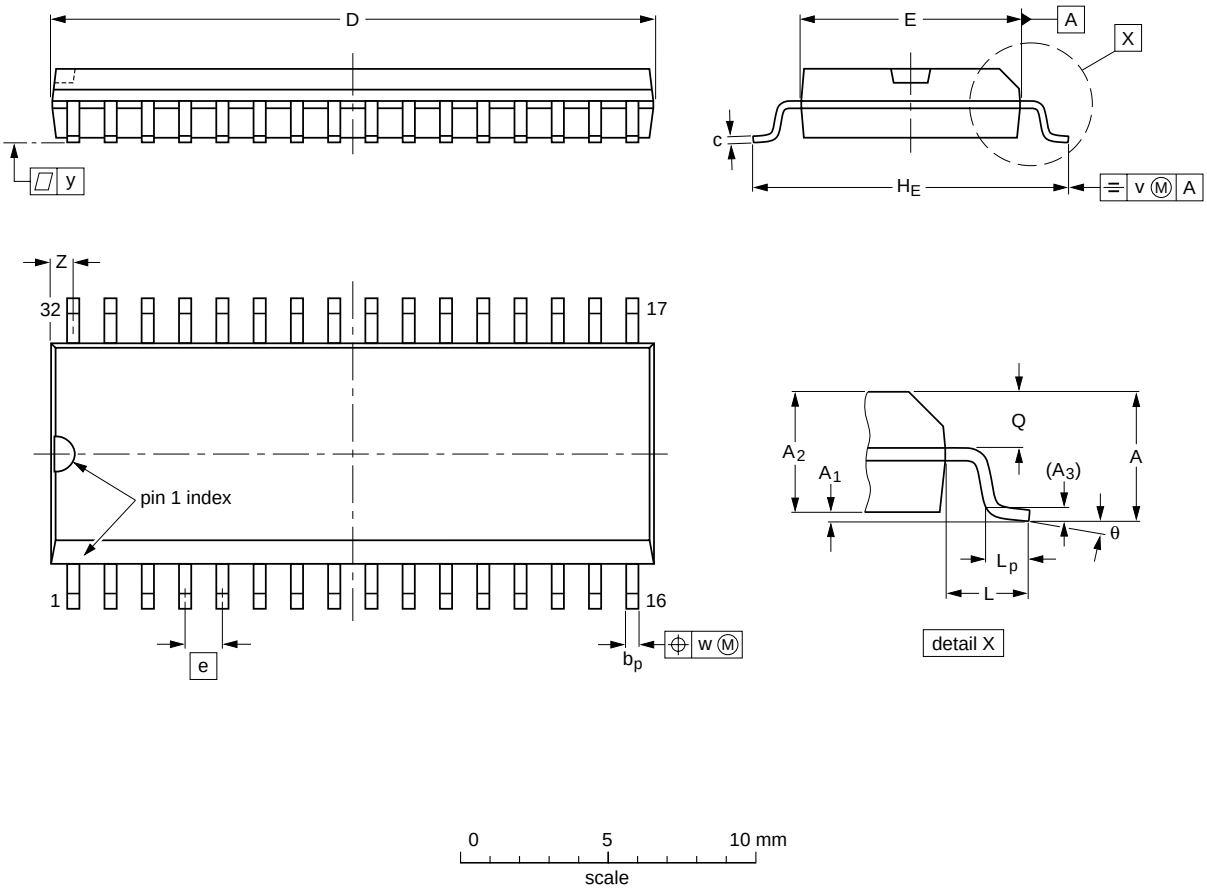


Fig.12 Application Diagram

PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 547047/1200/01/pp24 Date of release: 1998 Jan 08 Document order number: 9397 750 03147

Let's make things better.

Philips Semiconductors

PHILIPS