DATA SHEET

TDA8732
NICAM-728 demodulator (NIDEM)

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

NICAM-728 demodulator (NIDEM) TDA8732

FEATURES

- 5 V supplies for analog and digital circuitry
- Low cost application
- Improved noise behaviour
- Limiting amplifier for QPSK input
- Suitable with PAL B, G and I NICAM-728 systems.

APPLICATIONS

- NICAM-728 systems.

GENERAL DESCRIPTION

The NIDEM is a dedicated device providing a DQPSK (Differential Quadrature Phase Shift Keying) demodulator for a NICAM-728 system.
The device interfaces with NICAM-728 decoders and provides data synchronized to a 728 kHz clock (either supplied externally or by the on-board clock).
The device consists of a costas loop quadrature demodulator, a bit-rate clock recovery and differential decoder with parallel-to-serial conversion.
The Voltage Controlled Oscillator (VCO) used in the costas loop is achieved with a single-pin crystal oscillator.
A second single-pin crystal oscillator with a divider chain provides signals at 5.824 MHz and at 728 kHz.
The NIDEM is suitable for PAL B and G (carrier oscillator crystal at 11.7 MHz) and PAL I (carrier oscillator crystal at 13.104 MHz).

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5	5.5	V
V_{CCD}	digital supply voltage	4.5	5	5.5	V
V_{CCA}	analog supply voltage	4.5	5	5.5	V
$V_{CCA}–V_{CCD}$	differential supply voltage	–0.5	–	0.5	V
I_{CCA}	analog supply current	–	12.5	–	mA
I_{CCD}	digital supply current	–	14.5	–	mA
V_3	QPSK input level (peak-to-peak value)	30	100	300	mV
R_I	input resistance	1.75	2.5	3.25	kΩ
C_I	input capacitance	–	2	–	pF
f_{CAROSC}	carrier oscillator frequency	11.5	–	13.5	MHz
f_{XTAL}	crystal frequency				
	PAL B, G	–	11.7	–	MHz
	PAL I	–	13.104	–	MHz
f_{CLKOSC}	clock oscillator frequency	–	11.648	–	MHz
f_{C5M}	C5M output frequency	–	5.824	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8732	20	DIL	plastic	SOT146[1]

Note

1. SOT146-1; 1996 December 3.

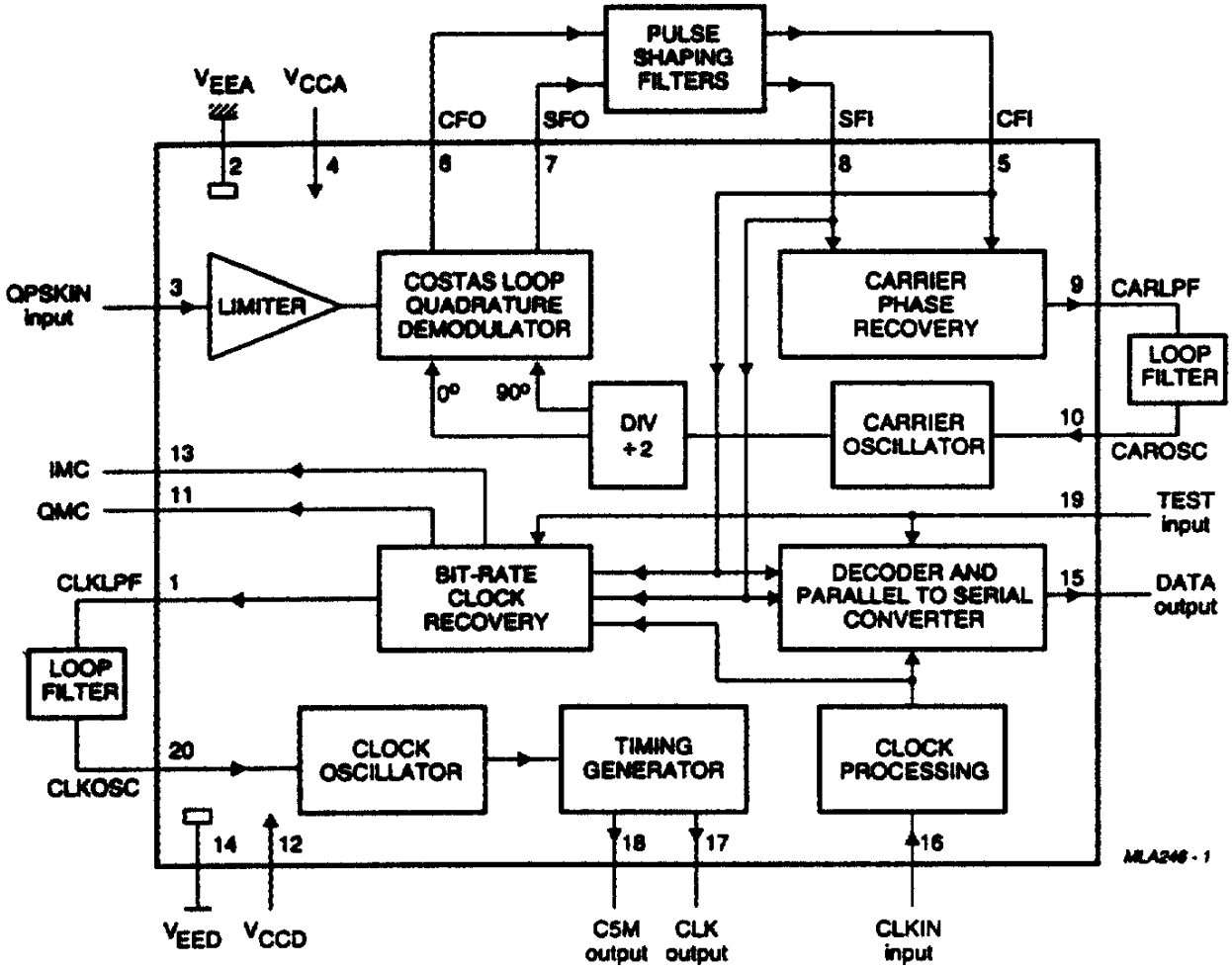


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLKLPF	1	transconductance output for bit-rate loop low-pass filter
V_{EEA}	2	ground for analog circuitry
QPSKIN	3	QPSK modulated data input
V_{CCA}	4	power supply for analog circuitry
CFI	5	baseband cosine channel input after filtering
CFO	6	demodulated cosine channel output to low-pass filter
SFO	7	demodulated sine channel output to low-pass filter
SFI	8	baseband sine channel input after filtering
CARLPF	9	transconductance output for carrier loop low-pass filter
CAROSC	10	crystal input for carrier oscillator (frequency is 11.7 MHz or 13.104 MHz)
QMC	11	monostable components connection for quadrature data transition detector
V_{CCD}	12	power supply for digital circuitry
IMC	13	monostable components connection for in-phase data transition detector
V_{EED}	14	ground for digital circuitry
DATA	15	728 kbit/s demodulated and differentially decoded serial data output
CLKIN	16	bit-rate clock input at 728 kHz, phase-locked to the data
CLK	17	output clock frequency at 728 kHz
C5M	18	reference frequency output at 5.824 MHz (8 x CLK)
TEST	19	input for test purpose (grounded for normal operation)
CLKOS	20	crystal input for clock oscillator (frequency is 11.648 MHz)

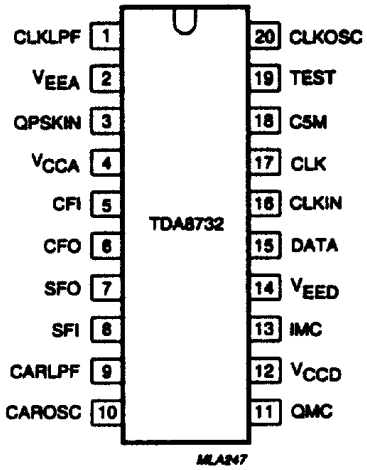


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

QPSK demodulator

The DQPSK signal input to the demodulator (QPSKIN) is limited and fed into the costas loop demodulator. A single-pin carrier oscillator (CAROSC), at twice the carrier frequency, supplies a differential signal to the divider circuitry, which drives the demodulators with both 0° and 90° phase shift. This produces cosine and sine signals which are required for the carrier recovery. Cosine (in-phase) and sine (in Quadrature) channel baseband filters are then provided externally between pins CFO and CFI, and SFO and SFI respectively. The two filtered baseband signals are then processed to provide an error signal, the magnitude and which of which bear a fixed relationship to the phase error of the carrier, regardless of which of the four rest-states the signal occupies. The carrier recovery loop is closed with the aid of a single pin loop filter connection at CARLPF, which filters the error voltage signal to control the 728 kHz as shown in application diagrams Fig.4 and 5.

Bit-rate clock recovery loop

The CFI and SFI channels are processed using edge detectors and monostables, with externally derived time constants (see Fig.3), to generate a signal with a coherent component at the data bit symbol rate. This signal is compared with the clock derived from CLKIN and used to produce an error signal at the transconductance output CLKLPF. This error signal is loop-filtered and used to control the clock generator (at CLKOSC if the on-board clock is used; see Fig.5).

Clock oscillator and timing generator

A voltage-controlled oscillator on-board the NIDEM operates at 11.648 MHz and is divided down to produce a 728 kHz (bit-rate) clock output (CLK) which is phase locked to the pulse stream and may be used as an alternative clock input for NIDEM. A reference clock at 5.824 MHz is provided at pin C5M (TTL levels).

Differential decoder and parallel-to-serial converter

The recovered symbol-rate clocking-signal (364 kHz) produced internally is passed to the demodulator where it samples the sliced raised cosine pulse stream. The recovered bit-rate clocking-signal is passed to the decoder and is used to differentially decode the demodulated data signal and reform it into a serial bit-stream.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	–0.3	6	V
V_{CCD}	digital supply voltage	–0.3	6	V
QPSKIN	modulated data input voltage	–0.3	5.5	V
CFI	baseband cosine channel input voltage	–0.3	V_{CCA}	V
SFI	baseband sine channel input voltage	–0.3	V_{CCA}	V
CFO	demodulated cosine channel output voltage	–0.3	5.5	V
SFO	demodulated sine channel output voltage	–0.3	5.5	V
CAROSC	crystal input voltage for carrier oscillator	–0.3	5.5	V
CLKOSC	crystal input voltage for clock oscillator	–0.3	5.5	V
QMC,IMC	monostable output voltage	–0.3	V_{CCD}	V
DATA	data output voltage	–0.3	5.5	V
CLK	clock output voltage	–0.3	5.5	V
C5M	reference frequency output voltage	–0.3	5.5	V
CLKIN	bit-rate clock input voltage	–0.3	6	V
TEST	input voltage for test purpose	–0.3	6	V
CLKLPF	bit-rate loop output voltage	–0.3	5.5	V
CARLPF	carrier loop output voltage	–0.3	5.5	V
T_{amb}	operating ambient temperature	0	70	°C
T_{stg}	storage temperature	–40	+125	°C
T_j	maximum junction temperature	–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	80 K/W

CHARACTERISTICS

V_{CCA} = 5 V ± 10%; V_{CCD} = 5 V ± 10%; –0.5 V < V_{CCA} – V_{CCD} < 0.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5	5.5	V
V_{CCD}	digital supply voltage		4.5	5	5.5	V
V_{CCA}–V_{CCD}	differential supply voltage		–0.5	–	0.5	V
I_{CCA}	analog supply current		–	13	17	mA
I_{CCD}	digital supply current		–	13	17	mA
P_{tot}	total power dissipation		–	130	187	mW
Inputs						
CLKIN						
V_{IH}	HIGH level input voltage		2	–	V_{CCD}	V
V_{IL}	LOW level input voltage		–	–	0.8	V
I_{IH}	HIGH level input current	V_I = 5 V	–	–	10	µA
I_{IL}	LOW level input current	V_I = 0 V	–400	–	–	µA
QPSKIN						
f_{QPSKIN}	input frequency		5	–	7	MHz
R_I	input resistance	f = 6 MHz	1.75	2.5	3.25	kΩ
C_I	input capacitance	f = 6 MHz	–	2	–	pF
SFI, CFI						
I_b	input bias current	V_{SFI} = 4.3 V; V_{CFI} = 4.3 V	–	–	5	µA
R_I	input resistance	f = 364 kHz	70	100	130	kΩ
C_I	input capacitance	f = 364 kHz	–	2	–	pF
CAROSC						
f_{car}	oscillator frequency		11.5	–	13.5	MHz
CARRIER OSCILLATOR CRYSTAL						
	holder			RW 43		
	nominal frequency with specified load	C_L = 15 pF				
$f_{PAL\ I}$	PAL I		–	13.104	–	MHz
$f_{PAL\ B,\ G}$	PAL B, G		–	11.7	–	MHz
	vibration mode	fundamental				
	circuit condition	series resonance				
	adjustment tolerance on frequency at 25 °C		–30	–	+30	10^{-6}
	temperature		0	–	70	°C
	frequency stability over temperature		–30	–	+30	10^{-6}
C_L	load capacitance		–	15	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_s	resonance resistance	note 1	15	–	40	Ω
C_m	motional capacitance		–	21	–	fF
C_p	parallel capacitance		–	–	5	pF
	drive power level		–	–	0.5	mW
CLKOSC						
f_{clk}	oscillator frequency	C_l = 15 pF	–	11.648	–	MHz
BIT-RATE OSCILLATOR CRYSTAL						
	holder			RW 43		
	nominal frequency with specified load	C_L = 15 pF				
$f_{PAL\ I}$	PAL I		–	11.648	–	MHz
$f_{PAL\ B,\ G}$	PAL B, G		–	11.648	–	MHz
	vibration mode	fundamental				
	circuit condition	series resonance				
	adjustment tolerance on frequency at 25 °C		–30	–	+30	10^{-6}
	temperature		0	–	70	°C
	frequency stability over temperature		–30	–	+30	10^{-6}
C_L	load capacitance		–	15	–	pF
R_s	resonance resistance	note 1	15	–	40	kΩ
C_m	motional capacitance		–	21	–	fF
C_p	parallel capacitance		–	–	5	pF
	drive level		–	–	0.5	mW
Outputs						
CFO, SFO						
R_O	output impedance	f = 364 kHz	–	110	200	Ω
V_{amp}	signal amplitude (peak-to-peak value)		0.8	1	–	V
CARLPF						
V_{OL}	LOW level output voltage	I_{OL} = 100 µA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –100 µA	V_{CCD}–1 V	–	–	V
gm ϕ1	phase comparator transconductance gain	V_O = 0.4 V to V_{CCD} – 1 V	100	125	–	µA/rd
I_{LO}	output leakage current for π/4 phase shift		–5	–	5	µA
CLKLPF						
V_{OL}	LOW level output voltage	I_{OL} = 100 µA	–	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level output voltage	I_{OH} = −100 μA	V_{CCD}−1 V	–	–	V
gm ϕ2	phase comparator transconductance gain	V_O = 0.4 V to V_{CCD}−1 V	50	65	–	μA/rd
I_{LO}	off-state output leakage current		−5	–	5	μA
IMC, QMC (TYPICAL RC NETWORK; R = 22 kΩ; C = 150 pF)						
t_{REC}	monostable recovery time		–	–	600	ns
t_{on}	monostable time		–	1.37	–	μs
CLK, C5M						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −100 μA	2.4	–	V_{CCD}	V
t_r	rise time	C_L = 15 pF; see Fig.3	–	20	–	ns
t_f	fall time	C_L = 15 pF; see Fig.3	–	20	–	ns
f_{C5M}	C5M reference frequency		–	5.824	–	MHz
DATA						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −100 μA	2.4	–	V_{CCD}	V
t_r	rise time	C_L = 15 pF; see Fig.3	–	30	–	ns
t_f	fall time	C_L = 15 pF; see Fig.3	–	30	–	ns
CLOCK TIMING						
t_d	CLK to C5M delay (pin 17 to 18)		–	15	–	ns
t_d	CLKIN to DATA delay (pin 16 to 15)	V_{CCD} = 4.5 V	–	520	585	ns

Note

1. Only the maximum value is relevant with a 15 Ω resistor in series with the crystal (due to the application requirements).

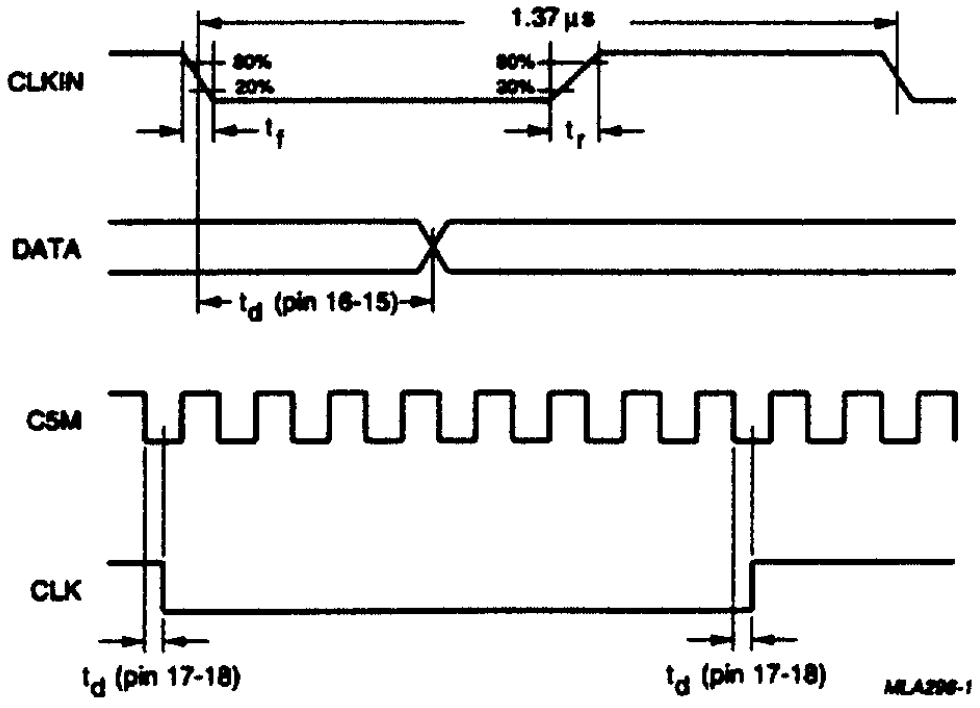
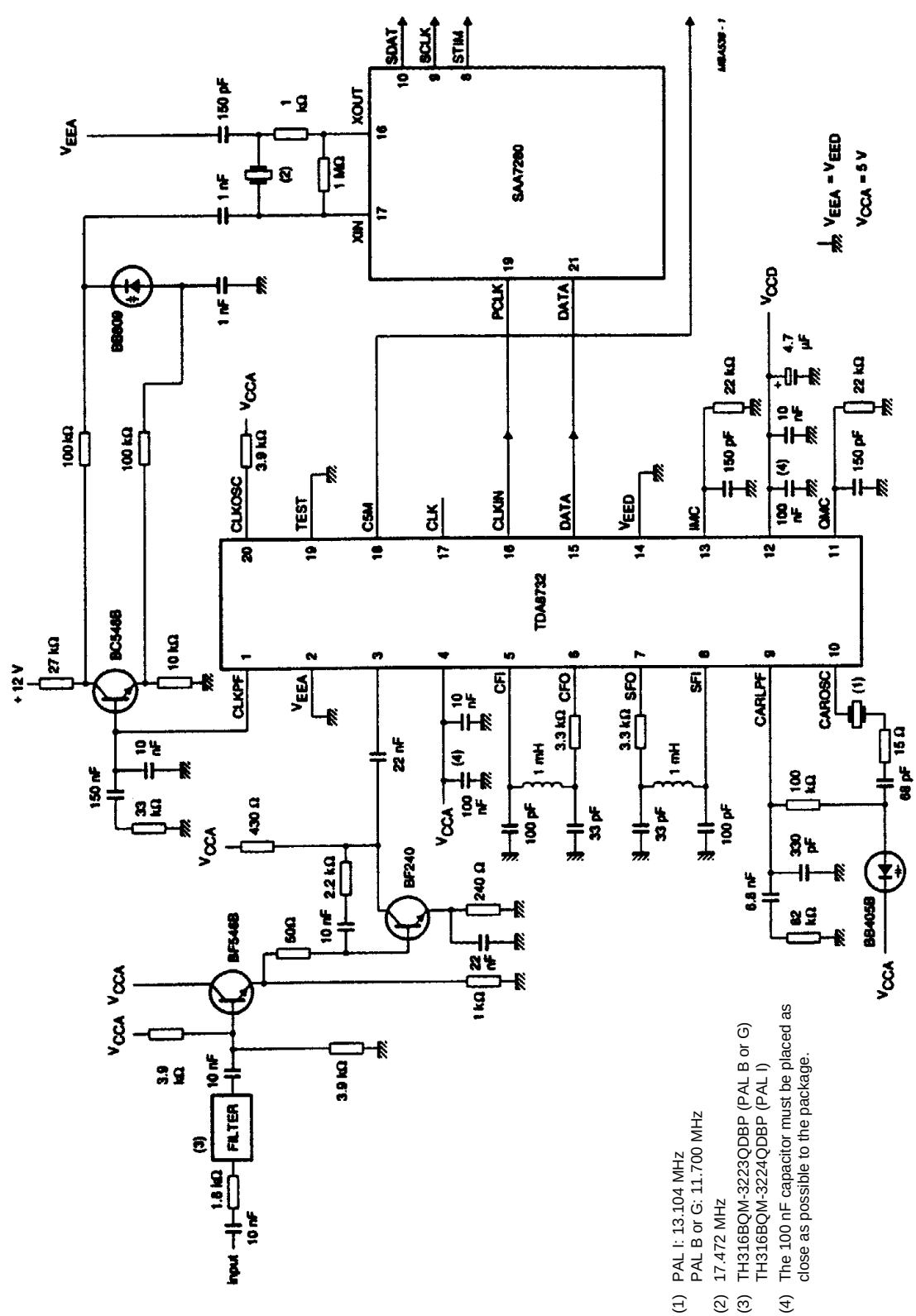


Fig.3 Data timing diagram.



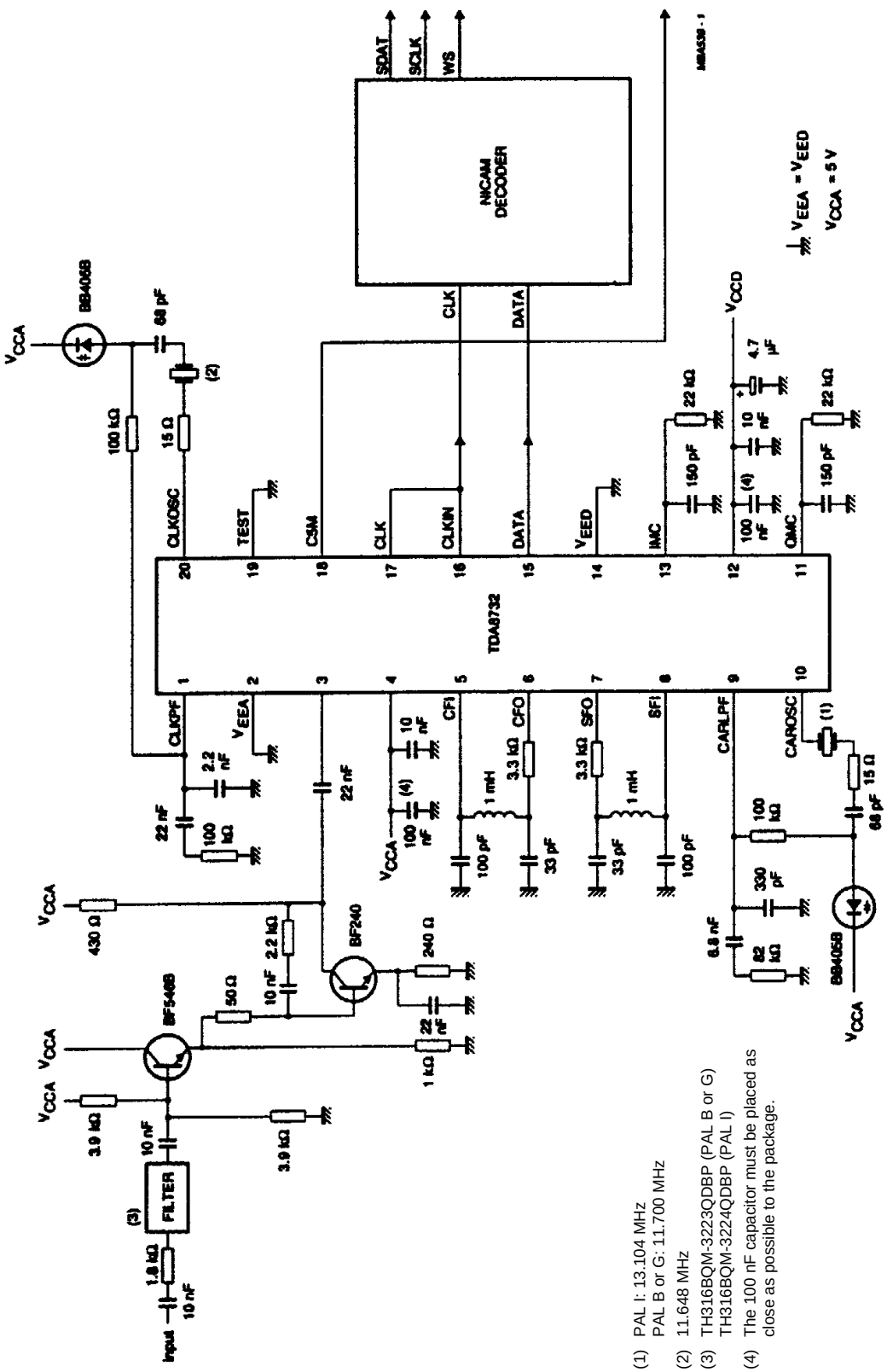
(1) PAL I: 13.104 MHz
PAL B or G: 11.700 MHz

(2) 17.472 MHz

(3) TH316BQM-3223QDBP (PAL B or G)
TH316BQM-3224QDBP (PAL I)

(4) The 100 nF capacitor must be placed as close as possible to the package.

Fig.4 Typical application diagram with the SAA7280.



(1) PAL I: 13.104 MHz
PAL B or G: 11.700 MHz

(2) 11.648 MHz

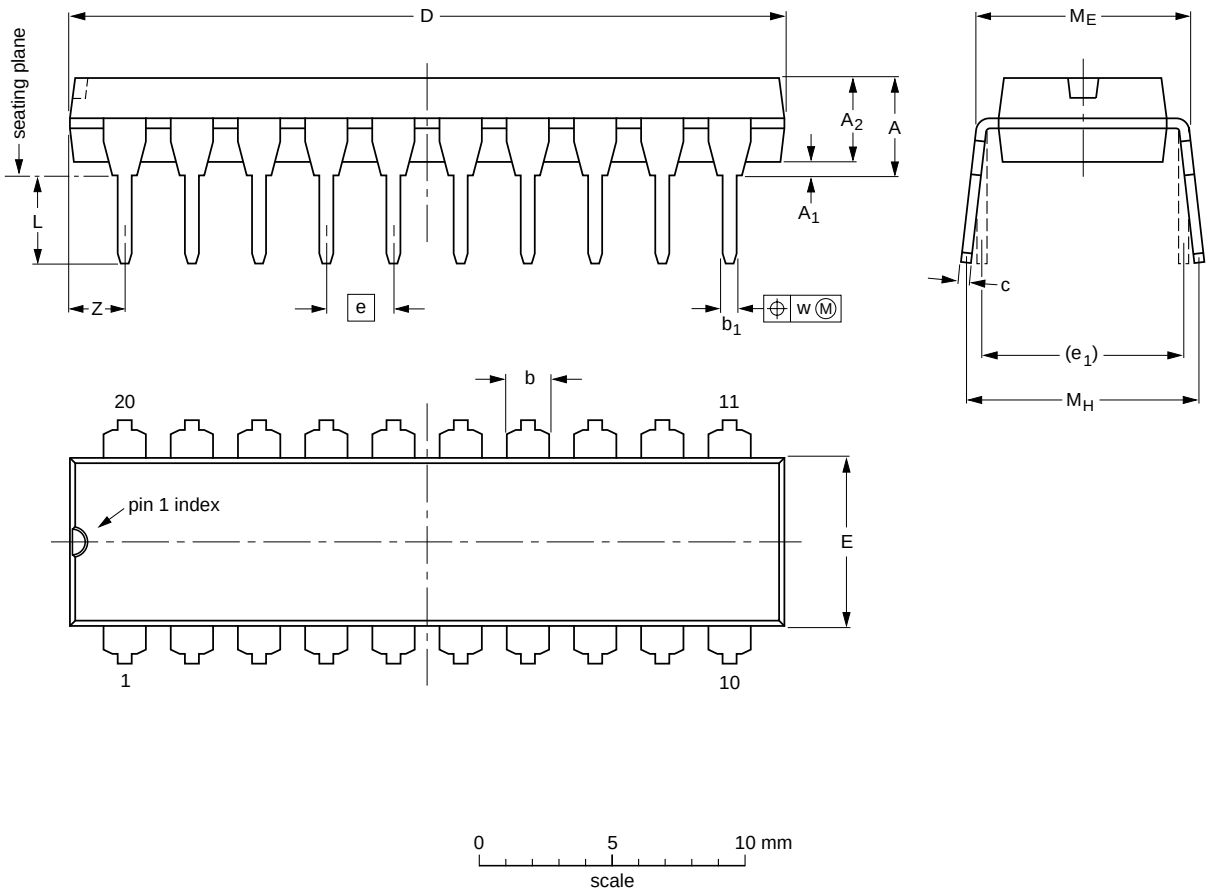
(3) TH316BQM-3223QDBP (PAL B or G)
TH316BQM-3224QDBP (PAL I)

(4) The 100 nF capacitor must be placed as close as possible to the package.

Fig.5 Typical application diagram with a NICAM decoder.

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.